

Some Aspects of a DSP Based Coprocessor Module , Applied in a System for Brain Activity Investigation

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Abstract

This paper describes design aspects of a system specialized in the acquisition and processing of brain potentials (EEG- signals).The system is composed from a PC-host computer equipped with an DSP based coprocessor for accelerating certain computing-intensive operations (FFT) and an acquisition unit (Head-box) serially coupled with the stand unit.

Keywords: EEG,data acquisition,DSP

1.Introduction

In the last few years, neurophysiology environments have experienced a significant evolution in the supporting technology which, based on computers, are taking a major role in A/D conversion, storage, display, signal processing and data base management including EEG. As a consequence of this fully digital computer take over, most of today's so called EEG machines are paper less.

Complex medical devices , and EEG also, request in the processing stage a high computing power.Modern implementations are based mostly on high-performance PC's.This paper describes a solution based on a less performant PC in combination with a DSP based coprocessor board, who takes many of the intensive computing tasks.

2.System structure

The system (fig.1.) consist mainly from two units:

- 1.Acquisition unit (Head-Box)
- 2.Processing unit (PC and DSP coprocessor)

The acquisition of brain potentials is done by an independent,isolated unit, serially linked with the DSP coprocessor. The unit accepts up to 24 input channels, amplifies the potentials (with a level of 10-150 μ V) , converts them in a digital form (max.12 bit resolution) and transmit those values to the DSP unit. Sampling frequency is 128 Hz, which allows evaluation of frequencies up to 45-50Hz.The unit is built using a 6809 microcontroller , who performs all the major tasks involved: local keyboard reading,management of the local LCD graphical display, data acquisition and communication with the host.

The DSP unit [1] is based on a fixed point DSP (TMS320C25 or TMS320C50) hosted in a PC compatible computer.The DSPxx25 board is equipped with TMS320C25 fixed point DSP.With a special adapter a TMS320C50 DSP can be used.

The block diagram of the board is presented in figure2. The structure has several particularities.

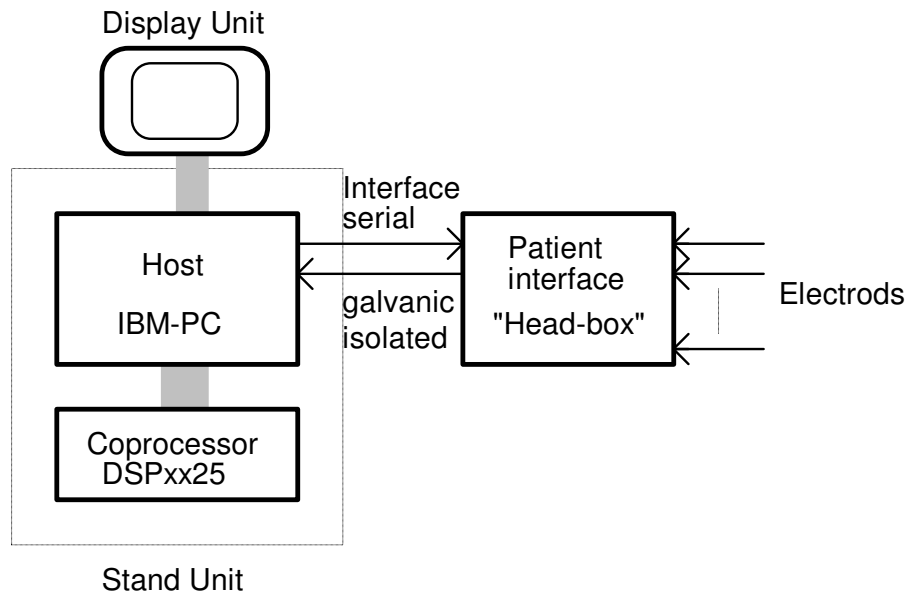


Fig.1. Block diagram of EEG system

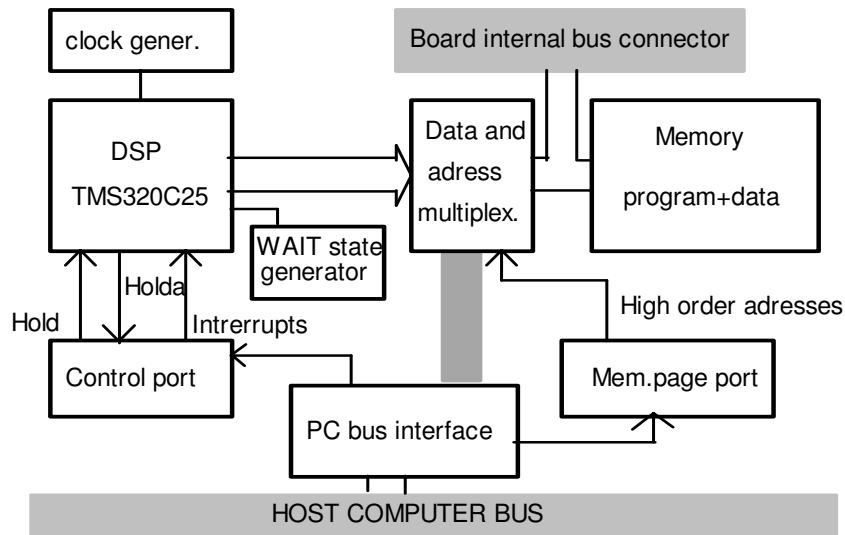


Fig.2. Block diagram of the coprocessor board

The memory(data and program) is shared, by multiplexing, between DSP and the host(PC). This feature allows direct access of the host to memory, accelerating the loading of programs and data and extraction of results. Therefore, the transfer speed is close to a memory/memory transfer in PC host, considerably higher than in similar development systems interfaced serial or parallel with the host.

To reduce interference with PC resources, memory from the host side is divided in 'slices' of 8kbytes each. The high order addresses are delivered from an internal special port (page port).

An other port manipulates the control signals of DSP (reset,hold,interrupt request).

For a higher efficiency the board can use one of the interrupt levels of the host .In the application described in this facility is not used.

The performances of the DSP board are the following [2]:

-DSP type	TMS320C25 or TMS320C50
-data format	fixed point
-maximum clock frequency	40MHz
-Wait states	maximum 2
-memory	64KWords program/data
-extensions	local DSP bus DSP serial
-physical format	AT type board

3.Software

The DSP unit has the following functions:

- communication with the acquisition unit
- prefiltering of input samples to eliminate the action of noise (especially the industrial frequency-50Hz).Filtering is done by a selectable set of non recursive filters (up to 40 cells)
- computing of FFT (256 points) for each channel
- computing of cross-corelation and autocorelation functions (as an option)

The host computer is dedicated especially for operator interface:

- recognizes and eliminates some artifacts in input signals
- displays waveforms of signals for the desired channels
- compute the power spectrum for the different domains of the input signal (delta,teta1,teta2,alfa,beta)

The software interface between host and coprocessor is done through a library , written in C , with the following functions:

- coprocessor detection and initialisation,loading of processing programs-INITDSP function
- input samples filtering -FILTERDSP function
- FFT computing -FFTDSP function

Object program occupies less than 1Kword in DSP coprocessor memory.

An unusual facility (certainly not encountered in classical - paper based - EEG machines) is the intuitive display of brain activity. The result is a schematic image representing the brain and his activity by means of pseudochromatisation according to the potentials measured in different zones.

Computing performances are illustrated in the following diagram (fig.3.)

This image presents the execution time for the different functions of the program (in milliseconds) - 256 samples filtering and respectively for FFT -three different implementations [3].

The duration is about 0.3 ms for nonrecursive filtering (3 cells) and between 12ms and 2.5 ms for various FFT implementations (Radix2,Radix 4 , for 8 and 16 bits respectively).

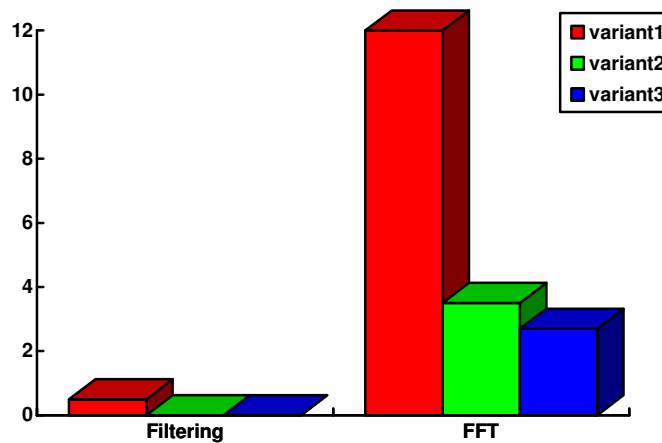


Fig.3.Coprocessor unit performances

4.Conclusion

Here are some conclusions revealed in the process of development ,especially the processing speed and the possibility of using low cost PC's.

The system has been designed to provide a high quality display of biological signals, with particular emphasis in neurophysiology environments and EEG signals. Anti-aliased reconstruction based on direct sample values, simulation of paper scrolling, pre-scaling, near-optimum reproduction of real EEG paper tracing and window and color keying for high versatility of screen space usage, are some of the concerns addressed in the current prototype solution. It allows fast page redraw, forward and backward page scrolling and annotation marks on an overlay plane.

The use of DSP coprocessor offer the possibility to implement a quasi-parallel system and to achieve a better separation of design tasks between the graphical interface , acquisition and signal processing with a gain in effectiveness.

The system can be further enhanced with additional signal processing functions,by simply upgrading the DSP coprocessor initialization program.

5.References

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