SUB-1V BANDGAP VOLTAGE REFERENCE OPTIMIZATION WITH GENETIC ALGORITHMS

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Abstract: This paper proposes an evolutionary approach to Bandgap Voltage Reference (BVR) design. The efficiency and feasibility of this method for solving the circuit design task are investigated. For demonstration purpose, two sub-1V BVR circuits are chosen. Circuit optimization is performed for various algorithm options. We have compared the design results obtained for purely random and deterministic initial conditions.

Keywords: *Sub-1V bandgap voltage reference, evolutionary circuit design, genetic algorithm (GA), GA parameters.*

I. INTRODUCTION

Analog and mixed-signal systems-on-a-chip, such as dynamic random memories, flash memories, analog-to-digital and digital-to analog converters, oscillators, PLLs, etc. [1,3], need stable reference voltages for circuit biasing. Thus, proper circuit operation strongly depends on the process, power supply voltage and temperature invariance of the reference voltage [2].

A widely employed solution is to have internal voltage reference blocks that generate the required temperature invariant voltage levels. The solution was found in Bandgap voltage references (BVR). The functioning principle of a BVR is depicted in figure 1. A voltage that is proportional to absolute temperature (PTAT) is used to compensate the negative temperature coefficient (TC) of a complementary to absolute temperature (CTAT) voltage. The result is an output voltage with low sensitivity to temperature.

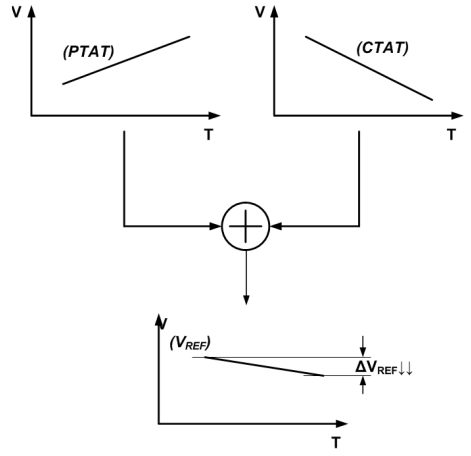

Figure 1. Bandgap voltage reference principle

The most appealing choice for a CTAT voltage is a bipolar transistor's (BT) base-emitter drop (v_{BE}) [3], due to its low-voltage potential. The v_{BE} negative temperature variance is compensated by a PTAT voltage, usually proportional to the thermal voltage V_T. Such BVRs provide the only real voltage references as they are directly derived from the bandgap of silicon [2], which is approximately 1.2V. Recent trends in analog and mixed-signal system developments however target low-power applications, such as medical implantable electronics, mobile electronics, etc. Consequently, sub 1V reference voltage levels are required [1]. In nowadays MOS technologies, sub-1V BVRs can use other CTAT voltages, such as *Vth*, that is the MOST threshold voltage.

The performance of BVRs can be estimated considering a set of measures, such as: initial accuracy, temperature insensitivity, power consumption, immunity to power supply noise, robustness to process variations, reliability, long term drift and temperature hysteresis [1], the first four being the most important for characterizing a BVR circuit. BVR performance however depends on the type of circuit, tolerances of the component parameters and their variation with temperature.

The design of BVRs translates to determining the circuit parameters of a chosen BVR topology, in order to satisfy a set of design specifications and circuit performance. Yet, the BVR needs to perform as specified even in the presence of errors. This leads to circuit redesign and parameter optimization until the design specifications are fully met and the optimal parameter set is determined [5].

Under these circumstances, the BVR design can be seen as a multi-objective and multi-constrained optimization problem. The multi-objective feature results from the multiple specifications which need to be simultaneously satisfied. The multi-constrained feature results directly from the physical constraints and operating regions in integrated circuits. As such, automatic circuit design tools become an attractive approach to solve the complex BVR design task.

This paper presents a genetic algorithm (GA)-based automatic design approach for the design of sub-1V BVRs.

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The paper is organized as follows. For proving the validity of the proposed method, two design examples are given. Section 2 gives the description of the designed circuits [6] [7]: a BiCMOS and a threshold voltage based MOS voltage reference, with an accent on the design parameters and their variation range. Section 3 explains the choice for GA for solving the circuit design problem and gives a description of the GA implementation. Particular attention is paid to the implementation of the objective function. Section 4 presents the simulation results for the design of both BVRs, for multiple algorithm parameters. Finally, conclusions are drawn in Section 5.

II. BANDGAP VOLTAGE REFERENCE CIRCUITS

In semiconductor technology, there are numerous ways to realize BVRs in both bipolar and CMOS technologies [2]. The goal is to have a constant reference voltage, invariant with temperature, power supply voltage and process.

The most straightforward way to generate a CTAT voltage is the base-emitter voltage (V_{BE}) of a diode-connected bipolar junction transistor (BJT) [2]. Other approaches use transistor's threshold voltage (V_{Th}) for the same purpose [5]. We took for example two such BVRs proposed in literature to demonstrate the validity of our design method

The first circuit to be designed, proposed by Malcovati et al. [6], is a BiCMOS BVR which achieves the sub-1V reference voltage by means of resistive division. The circuit schematic is given in figure 2. Malcovati et al. [6] have also proposed a possible implementation of the start-up circuit and the OpAMP, not presented in this figure.

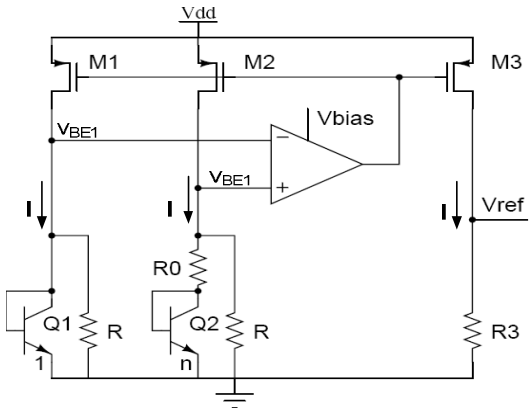

Figure 2. BiCMOS BVR [6].

The functioning principle is briefly described as follows [2]. The negative feedback equalizes the OpAMP input voltages, thus

$$v_{BE_1} = v_{BE_2} + R_0 I_0 \tag{1}$$

which results in

$$V_T \ln\frac{I_1}{I_{s1}} = V_T \ln\frac{I_0}{n \cdot I_{S1}} + R_0 I_0 \tag{2}$$

On the other hand

$$\begin{cases} I = I_0 + \dfrac{v_{BE_1}}{R} \\ I_1 = I - \dfrac{v_{BE_1}}{R} \end{cases} \tag{3}$$

Thus, $I_1 = I_0$ and

$$V_T \ln n = R_0 I_0 \Rightarrow I = V_T \frac{\ln n}{R_0} + \frac{v_{BE}}{R} \tag{4}$$

which gives

$$V_{ref} = \frac{R_3}{R}\left(\frac{R}{R_0} V_T \ln n + V_{BE}\right) \tag{5}$$

Consequently, if term $\frac{R}{R_0}\ln n$ is properly chosen [2], ideally V_{ref} will not depend on temperature and $\frac{R}{R_0} V_T \ln n + V_{BE} \cong 1.2V$. Thus, we may set V_{ref} to sub 1V values, by choosing ratio $\frac{R_3}{R}$.

Equation (5) shows that the reference voltage is actually determined by the value of resistors R_0, R and R_3 and by the BTs geometry ratio n. On the other hand, as proposed by Malcovati et al. [6], the OpAMP has a pseudo-differential input stage loaded by two transistors biased with V_{bias}. Thus, we consider that V_{bias} also counts for a design parameter.

Considering the design for a specific reference voltage, we have reduced the BVR design problem to the optimization of a set of 5 parameters:

$$[R, R_0, R_3, V_{bias}, n] \tag{6}$$

For proper circuit operation, parameter variation is bound to

$$\begin{cases} R_1 = R_2 \in 15k...35k \\ R_3 \in 10k...100k \\ R_0 \in 1k...2k \\ V_{bias} \in 540mV...700mV \\ n \in 5...17 \end{cases} \tag{7}$$

An additional constraint must be added for a proper transistor operation, that is, transistor M_3 must be biased in saturation. This means that

$$V_{SD_3} > V_{SG_3} - |V_{th}| \tag{8}$$

which is to be rewritten as

$$V_{D_3} - V_{G_3} = V_{ref} - V_{out\_AO} < V_{th} \tag{9}$$

where $|V_{th}|$=165mV is a process parameter. Equation (10) is the expression of the constraint imposed for transistor M_3 to operate in the saturation region.

The second circuit to be designed, proposed by Pletersek [7], is a CMOS BVR which achieves the sub-1V reference voltage based on the threshold voltage difference across an n-well resistor. The circuit schematic is given in figure 3.

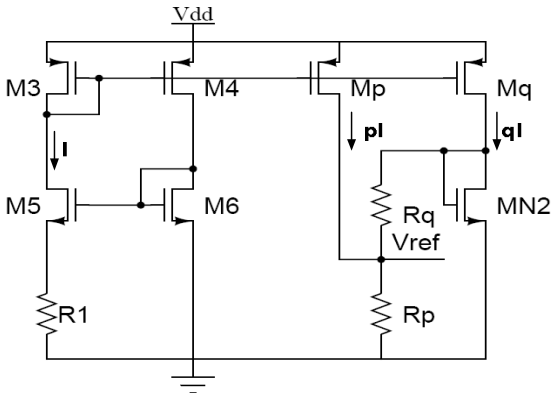

Figure 3. MOS BVR based on threshold voltage difference [7].

The operation principle of the MOS BVR biased in weak inversion is described as follows.

$$V_{GS} \cong V_{Th} \tag{10}$$

The diode connected transistor *M6* gives:

$$V_{GS6} = V_{GS5} + R_1 I \tag{11}$$

Since both transistors *M6* and *M5* are biased in weak inversion, i.e. $V_{GS} \approx V_{Th}$, the current *I* is written:

$$I = \frac{\Delta V_{Th}}{R_1} \tag{12}$$

The reference voltage is determined by the current through resistor R_p, thus:

$$v_{ref} = \left(\frac{v_{GS_2} - v_{ref}}{R_q} + p \cdot I \right) \cdot R_p \tag{13}$$

Finally, the desired reference voltage is expressed as:

$$V_{ref} = \frac{R_p}{R_p + R_q} \left(V_{th} + p \cdot \Delta V_{th} \cdot \frac{R_q}{R_1} \right) \tag{14}$$

which for the proper choice of pR_q/R_1 can become nearly constant vs. temperature variations. The values of V_{ref} are set by Rp/Rq.

The MOS transistor threshold voltage and its temperature dependency are process parameters. As such, eq. (14) shows that the reference voltage can be set by means of R_q, R_P and R_1. On the other hand, the drain current of *MN2* also has an influence on the reference voltage, and the transistor aspect ratio becomes a design parameter. Thus, we have reduced the BVR design for a specific reference voltage optimization of a set of 6 parameters:

$$\left[p, q, R_q, R_p, R_1, (W/L)_{MN2} \right] \tag{16}$$

where *p* and *q* are the current gain factors of mirrors M_3-M_P and M_3-M_q respectively.

For proper operation of the BVR circuit, transistors M_p and M_q must be in saturation. It is shown in [7] that p>q is mandatory. This translates to design constraints and must be handled accordingly. For a proper circuit operation, parameter variation is bound to

$$\begin{cases} p \in 3...15 \\ q \in 3...15 \\ R_q \in 1k...50k \\ R_p \in 100k...250k \\ R_1 \in 10k...100k \\ (W/L)_{MN2} \in (10\mu...100\mu)/10\mu \end{cases} \tag{17}$$

Compared to the BiCMOS BVR, it is unnecessary to translate the MOS transistor operating region constraints to equations. The parameter variation domains implicitly satisfy these constraints.

These examples are representative for proving our procedure, because in a similar manner, the design of almost all BVR circuits, presented in literature, a large number of such examples of schematics given in [1] and [2], can be designed optimizing a set of circuit parameters.

III. IMPLEMENTATION OF THE GENETIC ALGORITHM FOR BVR DESIGN

In this work, genetic algorithms (GA) are implemented for BVR circuit optimization. Before describing the implemented procedure, the choice for GA as an optimization method is explained.

As shown in the previous section, the design of a BVR circuit reduces to the optimization of a set of parameters under a set of constraints, in order to meet the design specifications. Thus, the design task presented in this paper can be seen as a parameter-level design problem, which is suitable for solving with computational intelligence techniques [8, 9]. The result is a procedure for automatic BVR design.

First of all, the choice for optimization methods, rather than knowledge-based methods, is obvious due to their capacity to generalize the circuit design procedure. The cost for this is however a longer design time. Further on, stochastic optimization [8, 9] is chosen over deterministic optimization [10, 11], due to its capacity to escape from local optima.

Evolutionary algorithms (EA) are in the category of stochastic optimization algorithms. Out of the EA family, it is shown in [12] that genetic algorithms (GA) are the most useful in search and optimization problems, due to their capacity to handle large and complex search spaces. As such, GAs are the best choice for the BVR circuit automatic design, which is a complex, multi-objective and multi-constrained optimization problem.

A simulation-based optimization is chosen for implementation, because simulator device models are more accurate than simplified model equations suitable for hand calculus. As such, circuit simulation will be performed within the optimization engine. Consequently, it is expected that the optimization results, i.e. the fully designed circuit, be better suited to satisfy the design specifications.

The block diagram of the implemented GA is shown in figure 4.

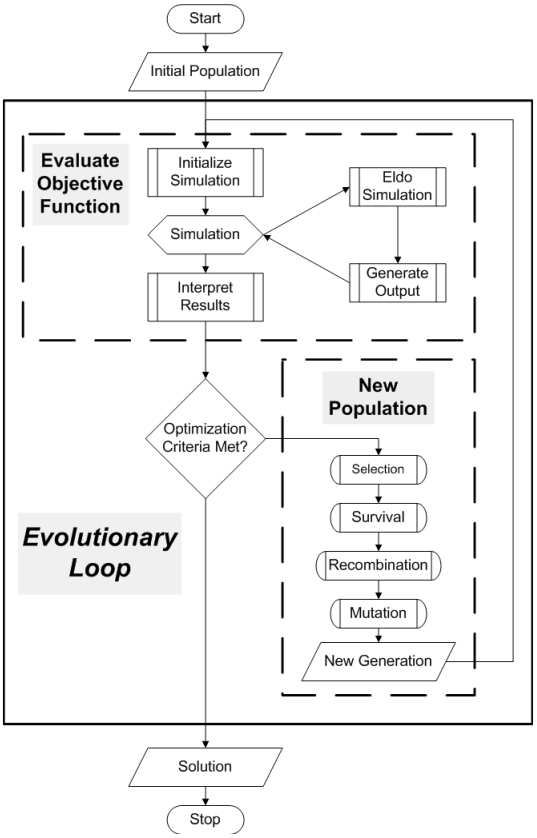

Figure 4. Block Diagram of the GA for BVR BVR optimization.

The implementation of the genetic operators is as follows. Fitness scaling is done with rank-based ordering. Selection is done with a stochastic universal sampling scheme. The creation of new population implements elitism, a scattered crossover operator and a Gaussian probability mutation. The elitist count, cross-over rate and mutation-rate are algorithm parameters which can be varied in order to gain algorithm performance. The parameter choices will be discussed in the next section. The stopping criterion is a number of 10 consecutive generations with a variance of the objective function less than 10^{-6}.

Further on, the definition of the objective function is presented. The GA considered in this work aims towards minimizing a cost function. The simulation-based optimization procedure enables simulation results to be used directly to compute the fitness of each individual.

As stated before, the BVR performance can be expressed by a multitude of measures. In the present work however, we only intend to optimize the BVR temperature performance. Consequently, only two BVR measures are targeted: the initial accuracy term and the temperature insensitivity.

The targeted BVR measures were defined in [5] as follows. The initial accuracy term refers to the difference between the BVR output and the reference voltage specification at the reference temperature, e.g. 25^0C. The temperature insensitivity term refers to the difference between the BVR output at the reference temperature and the BVR output at the edges of the temperature variation range, e.g. 0^0C and 100^0C for a rage of 0^0C – 100^0C. In the current work however, the temperature insensitivity term is computed by means of a temperature sweep over the variation range 0^0C – 100^0C, with an increment of 1^0C.

To be noticed is the multi-objective nature of the optimization task. Thus, a multi-objective optimization scheme [13] was employed. In the present work, the two distinct objectives are combined to one single goal by means of weighting. The GA objective function is expressed as in eq. (18), where t^0 is the temperature parameter, V_{ref} is the design specification for the output reference voltage, $V_{ref}@t^0C$ is the BVR output at temperature t^0 and a_1 and a_2 are the weights of the 2 terms.

$$OF = a_1 \cdot \left| V_{ref} - V_{ref}@25^\circ \right| + \\ + a_2 \cdot \sum_{t^\circ=0^\circ C}^{100^\circ C} \left| V_{ref}@25^\circ - V_{ref}@t^\circ \right| \quad (18)$$

To be noted is that the second term in eq. (18) is two orders of magnitude higher than the first, as it is the sum of 100 temperature differences. As such, the weighting factor a_1 must be chosen to compensate for this difference. The choice of the weighting factors is however subject to "trial and error".

As stated in the previous section, BVR operation is subject to transistors operating in the proper region. In [5], this problem was handled by adding another term to the weighted objective function, which is an active voltage constraint term. In the present work, proper transistor biasing has been imposed as evolutionary constraint, and was handled accordingly in the evolutionary loop.

IV. SIMULATION RESULTS

The GA for BVR circuit design was implemented in MATLAB (www.mathworks.com) using the Genetic Algorithm and Direct Search toolbox. Simulation-based optimization was achieved by using Eldo available from Mentor Graphics (www.mentor.com).

The simulation-based optimization engine was formerly proposed by the authors in [14]. It basically performs three steps: simulator initialization, simulator call and importation of the simulation output data. Thus, on-line circuit evolution is achieved.

Several tests for circuit evolution have been run, for various algorithm parameters, i.e. genetic operator parameters and weight factors a_1 and a_2. However, only the relevant trials are reported.

For the BVR circuit design, consider as design specification a BVR output voltage V_{ref} at the reference temperature 25^0C. The objective function expressed in eq. (18) is subject to minimization.

The first matter of concern is the choice of the weight factors. Throughout all GA runs, factor a_2 is kept fixed at a_2=1. Factor a_1 is varied to determine its value for satisfactory

evolution results.

For the first GA implementation, algorithm parameters have been chosen as follows: an elite count of 2 and a mutation rate of 20% which leaves an 80% cross-over rate. The reason was to have the majority of offspring produced via crossover, while still maintaining population diversity. The immediate effect is that, over generations, the evolution gets polarized towards a limited region in the search space. The GA solution is strongly dependent on the search direction at the beginning of the evolutionary process. Consequently, BVR performance will vary from one simulation to the other. The best results are reported as follows.

First, the BiCMOS voltage reference from figure 2 was designed for $V_{ref}=490mV$. The chromosome used for the BVR representation is the parameter set from eq. (7). Equations (8) and (10) give the constraints for the circuit evolution.

In a first design attempt, the initial accuracy term was considered of more significance than temperature insensitivity. This translates to a choice for a_1=3000. The V_{ref}=490mV@25^{0}C specification is fully met, and a reference voltage variance of 14.7% over 100^{0}C is obtained. This value is however considerably high. In the second design attempt, the constraint to satisfy V_{ref}=490mV@25^{0}C was relaxed in favor of minimizing the reference voltage variation. Thus, weight a_1 was set to 1000. The V_{ref}=490mV@25^{0}C specification is still met. Yet, the reference voltage variance was reduced to 7.6% over 100^{0}C. The V_{ref} vs. temperature characteristics obtained after circuit evolution in the two attempts are plotted in figure 5. The parameter values, as well as the BVR temperature coefficient, are listed in table 1.

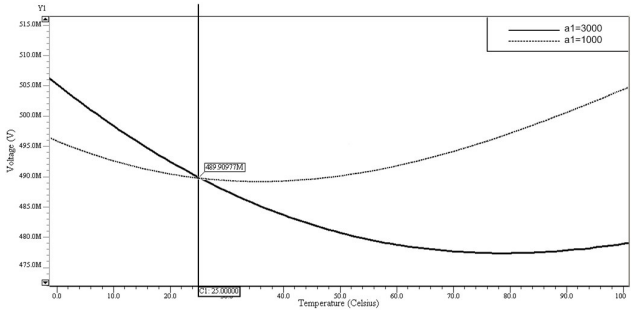

Figure 5. Temperature sweep characteristic of the BiCMOS BVR

Table 1. Parameters of the BiCMOS BVR after design.

a_1	R [kΩ]	R_0 [kΩ]	R_3 [kΩ]	V_{bias} [mV]	n	Temp. coeff. [ppm/^{0}C]
3000	16.3	1.07	10.5	661	17	591
1000	17.6	1.05	10.1	619	10	306

The reduction of factor a_1, leads to a slight improvement of the BVR temperature performance. Simulation of the BVR was done using a digital fabrication process. Thus, BTs are very poor concerning factor β. Therefore, results achieved in this work are lower than some formerly reported in literature, e.g. [6]. The proposed method was proven to be valid and suggests improving technological parameters, by using for example a BiCMOS technology, or may be continuing search for other population and initial conditions.

In the given circumstances, an alternative to the BiCMOS BVR is to have the currents generated by sub-threshold MOS transistors instead of BJTs. This led to our choice of the MOS BVR based on threshold voltage difference, shown in figure 3.

The BVR from figure 3 was subject to design for $V_{ref}=420mV$. The chromosome used for the BVR representation is the parameter set from eq. (16). Equation (17) gives the bounds for constrained circuit evolution.

Out of similar reasons as before, weight factor a_1 was set to 500 in the first design attempt. The V_{ref}=420mV@25^{0}C specification is fully met. The reference voltage variance is 17.8% over 100^{0}C. For a second GA run, factor a_1 was set to 100. The V_{ref}=420mV@25^{0}C specification is again fully met. Yet, the reference voltage variance has decreased to 9.5% over 100^{0}C. The V_{ref} vs. temperature characteristic obtained after the GA run in the two design attempts are plotted in figure 6. The parameter values, as well as the BVR temperature coefficient are listed in table 2.

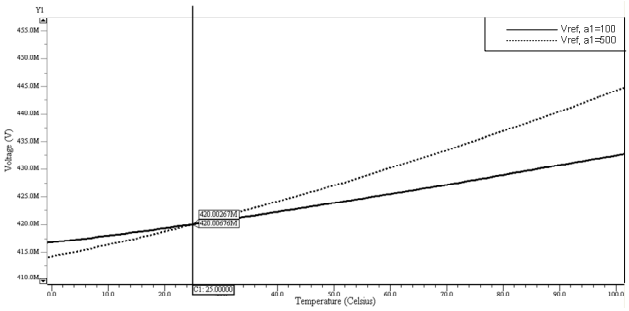

Figure 6. Reference voltage temperature sweep characteristic of the V_{th} based MOS BVR.

Table 2. Parameter values for the CMOS BVR after design.

a_1	p	q	R_O [kΩ]	R_P [kΩ]	R_1 [kΩ]	W_{MN2} [μ]	T. Coeff. [ppm]
500	9	3	33.3	226.1	61	74	714.2
100	11	7	4	223.3	75	49.5	381

To compensate for the phenomenon of polarized evolution, the authors adopted the following strategy. The mutation rate was also increased to 40%. The elite count has been increased to 4 so that promising individuals are not lost and survive to the next generation. The reason was that having a higher number of offspring produced via mutation increases the probability to search outside the proximity area of the parents. This broadens the actual search area and consequently increases the chances of finding the optimal solution.

The design of the V_{th}-based CMOS BVR has been repeated for these algorithm parameters. The design specification V_{ref}=420mV@25^{0}C has again been fully met. The variance of the reference voltage variation has been improved to 1.7% for a_1=100. The V_{ref} vs. temperature characteristics obtained after the GA run are plotted in figure 7, for two values of a_1. The parameter values, as well as the BVR performance are listed in table 3.

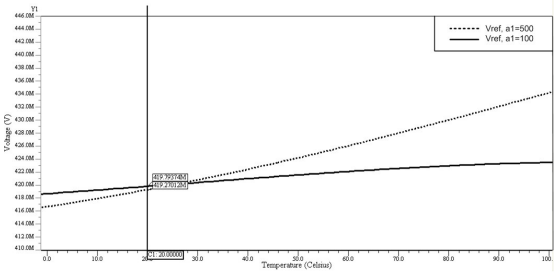

Figure 7. Reference voltage temperature sweep characteristic of the V_{th} based MOS BVR.

Table 3. Parameter values for the CMOS BVR after design.

a_1	p	q	R_O [kΩ]	R_P [kΩ]	R_1 [kΩ]	W_{MN2} [μ]	T. Coeff. [ppm]
500	6	8	1.9	219.3	13.3	67.7	404.7
100	4	4	18.8	231.8	21.2	90	71.4

The average distance between individuals vs. generations is plotted in figure 8. The dotted line, corresponding to the GA with an elite count of 2 and mutation rate of 20%, clearly shows the polarized nature of the evolution. The solid line, corresponding to the GA with an elite count of 4 and mutation rate of 40%, proves that the search diversity is indeed maintained over generations.

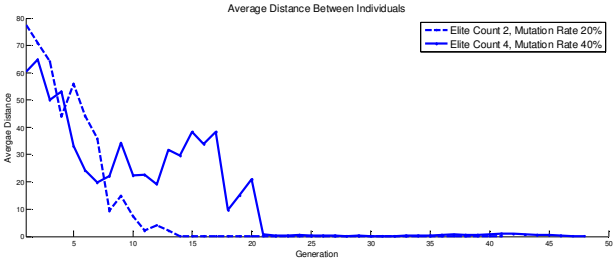

Figure 8. Evolution of the distance vs. generations.

One of the main drawbacks of this search method is the extremely large search-space. With no knowledge whatsoever regarding the targeted solution, the GA initial conditions are purely random. Long evolution times are recorded. It is then sensible to consider initializing the GA with a pre-designed circuit that partially meets the design specifications and restrict the parameter variation ranges even further.

To investigate this matter, the circuit design task was split into two layers. The first layer implements a GA, with an elite count of 4 and a mutation rate of 40%, to perform raw circuit design. The solutions of the first layer are then fed as initial conditions to the second layer. Simulations have shown that a GA on the second layer doesn't improve the design solutions. Alternatively, a gradient deterministic optimization function is implemented, resulting in a hybrid GA. For a_1=100, the BVR temperature coefficient reaches 76.2 ppm. The design gain also lies in the considerably shorter design time due to the deterministic second layer.

CONCLUSIONS

This paper presents an approach to automatic circuit design by employment of GAs. Two sub-1V BVRs were subject to design with the proposed method. An analysis of the BVRs was made in order to determine the chromosome and evolutionary constraints. Simulation results proves that BVR design is indeed feasible by means of the proposed design method. It is also shown that a proper choice of algorithm parameters leads to improved evolution results.

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