EFFICIENT STRATEGIES TO OPTIMIZE A POWER DISTRIBUTION NETWORK

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Abstract: One of the biggest design challenges for today is to properly design, manufacture, simulate and validate a power distribution network (PDN) in systems with increasing speed, power dissipation and density. Power distribution networks are typically comprised of capacitors networks that have several types of capacitors and values to obtain target impedance over the required frequency range for the power/ground planes on PCBs. Capacitors provide a temporary source of localized energy for instantaneous current demands from an IC, and a low-impedance return path for high frequency noise.

Keywords: *Power distribution network, target impedance, decoupling capacitor, dielectric constant, plane separation.*

I. INTRODUCTION

The power distribution is a major challenge in present-day systems. This challenge is expected to increase in the next decade as systems become smaller and new materials are introduced into packages and boards.

The power distribution network (PDN) consists of all interconnects from the voltage regulator module to the pads of the chip that locally distribute power and return current.

The main concern is to keep a constant supply voltage on the pads of the chips, and keep it within a narrow tolerance band, typically on the order of 5%. The voltage has to be stable, within the voltage limits, from DC up to the corner frequency.

Second, in most designs, the same power distribution network interconnects that are used to transport the power supply are also used to carry the return currents for signal lines. The interconnects must provide low impedance return path for the signals. The easiest way of doing this is by making the interconnects wide, so the return currents can spread out as much as they want, and by keeping the signal traces physically separated so that the return currents do not overlap. If these conditions are not met, the return current is constricted and the return currents from different signals overlap. The result is ground bounce, also called simultaneous switching noise.

Finally, since the power distribution network interconnects are usually the largest conducting structures in a board, carrying the highest currents, and sometimes the high frequency noise, they have the potential of creating the most radiated emissions and causing failure of an EMC certification test. When done correctly, the power distribution network interconnects can mitigate many potential EMI problems and help prevent EMC certification test failures.

The consequence of not designing the PDN correctly is that there will be excessive noise on the voltage rails of the chips. This can cause a bit failure directly, or it can mean that the clock frequency of the chip can't be met resulting in timing errors.

To conclude the introduction, we can say that the purpose of the power distribution network in a board is a threefold: ***keep the voltage across the board constant, minimize ground bounce***, and ***minimize EMI problems***.

II. THEORETICAL DISCUSSIONS

A. Board Planes

Planes play a very important role at high frequencies by acting as high-frequency capacitors, serving as conduit for the transportation of the current, and supporting the return currents of the signal lines referenced to it. Planes are large metal structures separated by a thin dielectric and are invariably used in all high-frequencies boards for power distribution [1].

Voltage and ground planes transport the current from the capacitors to the switching circuits, therefore control the inductance and delay from the capacitor to the switching circuits. At high frequencies much beyond the resonant frequency of the capacitor, the plane inductance dominates the impedance of the power distribution network [1].

The capacitance formed between the voltage and ground planes can be used to decouple the power supply at high frequencies and hence becomes a useful contributor [1].

Planes carry the return current of the signal lines, and hence the voltage fluctuations between the voltage and ground planes across the board are dictated by the plane behavior [1].

The voltage distribution on the plane for a board of size $a \times b$ depends on the resonance mode, while the resonance frequency is determined by the mode number, the dielectric constant of the insulator, and the physical size of the planes. The resonance frequency of the planes

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is given by [1]:

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (1)$$

where the first mode, assuming $b>a$, correspond to a resonant frequency of:

$$f_{01} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\frac{\pi}{b} = \frac{1}{2b\sqrt{\mu\varepsilon}} \quad (2)$$

In equations (1) and (2), μ and ε correspond to the permeability and permittivity of the material between the planes.

Since planes are passive structures, they can be represented using transfer functions. The parameter that is often used to understand plane characteristics is the impedance. The impedance of any two-port circuit can be defined as:

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \quad (3)$$
$$V_2 = Z_{12}I_1 + Z_{22}I_2 \quad (4)$$

where V and I are the voltage and current at the two ports, and Z is the impedance [3]. Impedances Z_{11} and Z_{22} are called as the self-impedances, while Z_{12} and Z_{21} are called as the transfer impedances. These impedances can be modeled and measured, and can be used to represent the behavior of the planes. With a few exceptions, the power distribution network interconnects and components are electrically reciprocal, therefore $Z_{12} = Z_{21} = Z_{transfer}$. However, in general, Z_{11} is not equal to Z_{22} [2][3].

Z parameters or impedance parameters are a type of frequency domain electromagnetic model. They are very similar to the S parameters, which are used a lot in signal integrity analysis, and there are also Y parameters, or admittance. Z parameters give us a pretty good picture of the effectiveness of the power distribution network and allow to characterize different design changes such as using different values capacitors, mounting the capacitors differently or putting the capacitors on different location on the board [1][2][3].

B. Influence of Plane Parameters on Self-Impedance and Transfer Impedance

For a better optimization of the power distribution network, it must be examined how the plane parameters affect the plane impedance and resonances. Specifically, it must be analyzed the impact of the dielectric thickness, plane thickness and dielectric constant on the plane impedance.

a) Impact of dielectric thickness

Resonances of planes can contribute to increase simultaneous switching noise and ground bounce. Thin dielectric materials by themselves can effectively help to suppress plane resonances of boards. It is known that the series conductor losses of a transmission plane increase the attenuation, which under matched conditions can be expressed as [3]:

$$A(f)^{dB} = 4.35\left(\frac{R_s}{Z_0} + G_d Z_0\right) \quad (5)$$

R_s, the total series resistance of the conductor, determined by the cross section of the conductor, is also known as the AC resistance that accounts the skin effect on both conductors, and is calculated with next equation [1][3]:

$$R_s = 2\sqrt{\frac{\pi f \mu_0}{\sigma_c}} \quad (6)$$

In the equation above, μ_0 is the permeability of free space, and σ_c is the metal conductivity.

At higher frequencies, the resistance of conductor increases, because current tends to flow on the surface, leaving for current conduction only an effective channel of depth, which is proportional to the inverse square root of frequency. This effective depth is called skin depth, and at a first approximation is expressed as [3]:

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \sigma_c}} \quad (7)$$

G_d, parallel conductance of the dielectrics, is also known as the shunt conductance and represents the dielectric loss in the material between the planes [1][3]:

$$G_d = \omega C tan\delta \quad (8)$$

In the equation above, C is the capacitance of the plane, and $tan\delta$ is the loss tangent of dielectric.

$$C_{plane} = \frac{A \cdot \varepsilon}{d} \quad (9)$$

Z_0 is the characteristic impedance of the transmission plane. As the dielectric thickness decreases, skin effect losses remain constant, but the characteristic impedance, that is $Z_0 = \sqrt{L/C}$, decreases proportionally with the dielectric thickness. This happens because inductance and capacitance are proportional and respectively, inversely proportional to the dielectric thickness.

With decreasing dielectric thickness, the dielectric loss term eventually decreases, thus leaving the skin loss responsible for the suppression of the plane resonances. This simple approximation shows how thin dielectrics between power and ground planes have advantages for power distribution networks at high frequencies [3].

The above expressions, (5), (6), (7), (8), suggest that the same resistance produces higher attenuation if the characteristic impedance is lower. This also suggest that in case of parallel conductive planes, if the planes are put sufficiently close, without any change in the material properties, the series ac resistance eventually may provide enough attenuation to suppress plane resonances.

b) Impact of dielectric constant

The granularity of the power-ground plane models is important: each transmission line segment in the model should represent a small fraction of the wavelength of the highest frequency of interest. With a 15.24 cm square plane with 8 x 8 grid and $\varepsilon_r=4$ dielectric constant, the accuracy of the model significantly deteriorates above 2GHz. Since the propagation delay goes linearly with $\sqrt{\varepsilon_r}$, the same grid model is limited to about 1GHz and 0.5GHz. The typical PCB materials have been optimized for low-loss signal transmission; as a result, they do not provide sufficient suppression of plane resonances. If used only between the power/ground planes, intentionally high dielectric losses may be utilized [3].

C. A Basic Decoupling Methodology

Decoupling methods reduce the ripple noise in the power distribution network. Using decoupling capacitors is one of the most common, efficient and relatively inexpensive ways to achieve power integrity. This method involves choosing the number of capacitors of each value such that the parallel combination of capacitors approximates a flat line at the target impedance. Assuming that only a small percentage of the power supply voltage is allowed as ripple voltage and there is a maximum switching current, target impedance for the power distribution network is calculated as [1][2]:

$$Z_{target} = \frac{allowed\ ripple\ \cdot voltage}{I_{switching\ current}} \qquad (10)$$

Trying to achieve the target impedance calls for a flat impedance profile from DC up to a certain corner frequency, beyond which frequency the impedance may rise linearly, following the reactance of the PDN inductance. The corner frequency is the maximum frequency of interest determined by the rise time of the load and limited by the package or by the PCB inductance. Target impedance and the frequency corner are useful to calculate the optimal number of parallel capacitors, *n*, that are needed to achieve the flat profile from DC up to the frequency of the interest [3]:

$$n = 2\pi \frac{f_c \cdot \left(L_{cap} + L_{mount}\right)}{Z_{target}} \qquad (11)$$

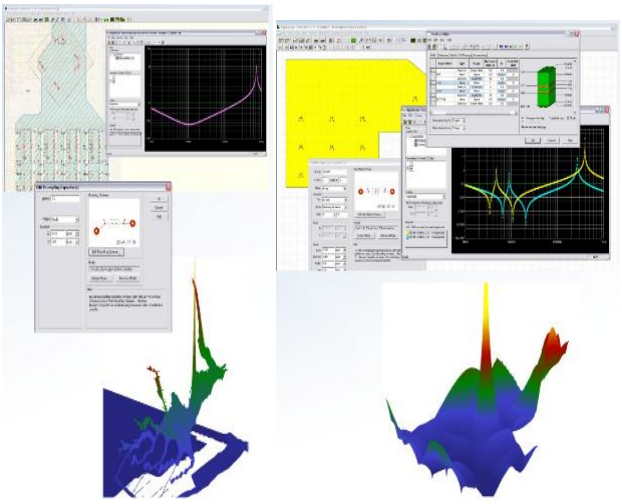
In the expression above, L_{cap} is the internal capacitor inductance or the equivalent series inductance and L_{mount} is the mounting inductance, and f_c is the corner frequency. The approximate number of capacitors for each value can be calculated by dividing the target impedance into the ESR of that capacitor.

A power distribution network that meets the target impedance across the entire frequency has sufficient stored charge to supply clean power at all frequencies. On the other hand, a power distribution network that is higher than the target impedance in any frequency band will usually fail to meet the specified voltage tolerance under some load condition. If the measured impedance is substantially below target impedance in any frequency range, the cost of the power distribution network can usually be reduced while still meeting the power specifications. It is referred to as "target" because it gives the best cost and performance solution for the power distribution network [1][2][3].

III. SOFTWARE PRESENTATION

With the growing number of power problems on modern PCB designs, HyperLynx PI from Mentor Graphics is an indispensable tool, allowing an insight of this problems and allowing generating solutions quickly. Hyperlynx PI allows to the user to identify power distribution problems very early into design even prior to layout with a very powerful what-if analysis environment, it identifies problems early and possible solutions to this problems.

Hyperlynx PI offers an easy way to perform an AC analysis for the power distribution network. Once the board data are read by Hyperlynx BoardSim, it can be analyzed the impedance profile of the power distribution network. If it accounts any problems, the design can be exported from BoardSim to LineSim and can be made what-if analysis such as adding and removing decoupling capacitors, changing the capacitors values, changing the way the decoupling capacitors are mounted on the board, changed the board stack-up to see if they solve any issues they might accounted in the power distribution network impedance. It can be also performed a noise analysis to visualize that the decoupling strategy is actually working and get a more intuitive feeling of the effectiveness of the decoupling. It can create board's outlines, put voids into the plans, change planes, shapes, and/or add copper, also, the decoupling can be moved around the board or add others with different models.



IV. SIMULATIONS RESULTS

To illustrate the concept presented chapter II, let's plug in some numbers from a real example. For the sake of simplicity, we assume that we have a *40x10inch* board,

with a 5V supply plane with two ICs attached to it, located at the coordinates from the figure 1.

We suppose that those ICs need 2A of switching current; these ICs also have a maximum voltage ripple requirement of 5%. So by using the equation (10), we see where our max PDN impedance can be and it comes out to be 125mΩ. So we want to synthesize 125mΩ of impedance supposing that the corner frequency is about 400MHz.

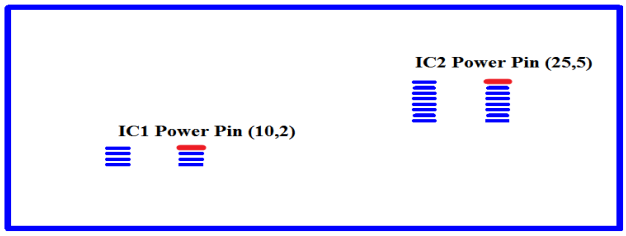


Figure 1. ICs location on a *40" x 10"* board.

An ideal current source, with infinite resistance and zero capacitance, is usually an acceptable AC model for an IC power pin. The stimulus for every IC was modeled as in figure 2.

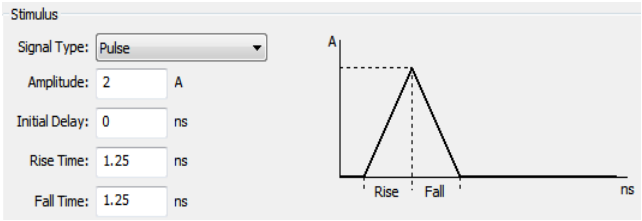


Figure 2. The shape and magnitude of the maximum switching current.

To figure out what that impedance is on our real board, we can look at the impedance as a combination in parallel of all the different capacitors and of course their parasitic and whatever the *Cplane* may have on the board. So we are trying to visualize the Z parameter profile of the PDN [4][5][6][7][8].

Noise analysis allows for inspection of maximum voltages. These voltages are based upon real expected loads in the system and they give a pretty good indication where the noise is going to be located on the board. Hyperlynx PI offers a visual representation of the analysis data that is coming out from decoupling. We can actually visualize the decoupling working and see areas of the board that might need more decoupling [7].

The noise that propagates on the planes gets shaped by a number of things: plane shapes, the stack-up, and plane capacitance as well, capacitors, all of those will shape how the noise propagates around the plane. Another thing that is important is the actually current waveform that is being induced under the plane [7][8][10][11].

An item that is very important to the power distribution network is the embedded capacitance or the plane's capacitance and this is going to be highly dependent to the stack-up of the board, mainly the plane separation and the constant of the dielectric separating those planes. The size of the planes is the other determinant, but is typically determinate by the size of the board and the capacitance of this embedded plane pair is very simple to calculate, is just a simple parallel plate capacitor and that is equal to the dielectric constant time by area divided by the distance between the plates. The embedded capacitance is very important because is really the only effective capacitance at higher frequencies. Because of its very low inductance, it has a dominant capacitance at higher frequencies that the regular capacitor can't provide.

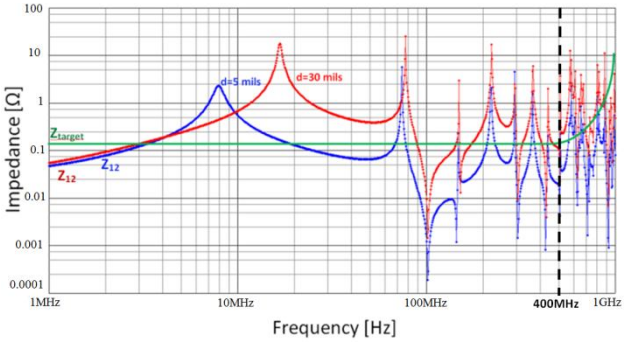


Figure 3. The transfer impedance without decoupling capacitor, for two cases: d=30mils, and d=5mils.

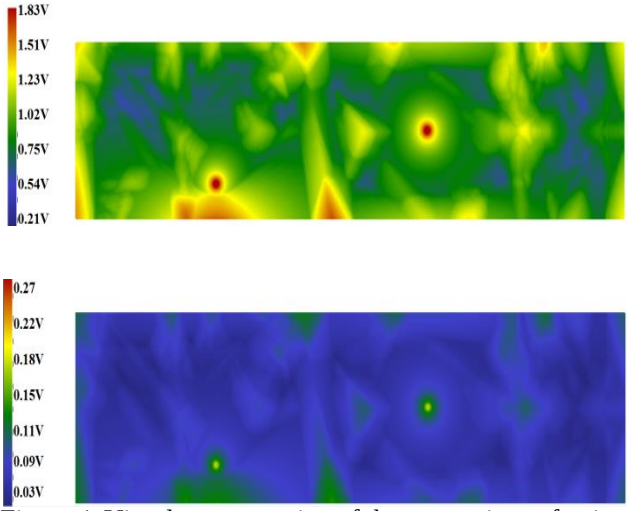


Figure 4. Visual representation of the comparison of noise propagation in those two cases: d=30mils (top), d=5mils (bottom).

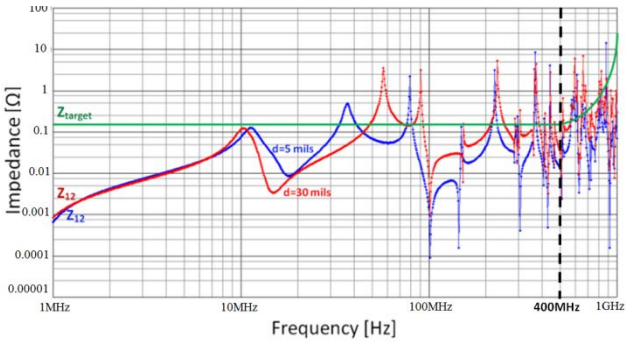


Figure 5. Transfer impedance of the plane with 100nF and 33uF decoupling capacitors.

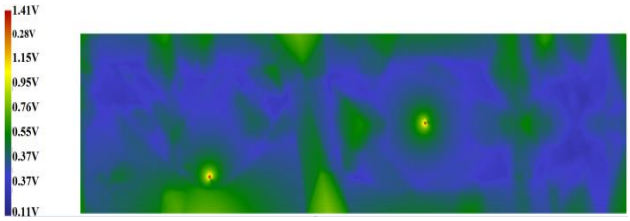


Figure 6a. Visual representation of the propagation of noise on the plane: without decoupling capacitors (top); with decoupling capacitor (bottom).

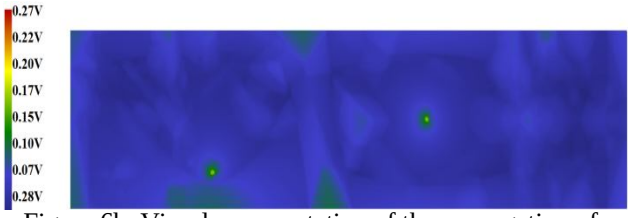


Figure 6b. Visual representation of the propagation of noise on the plane: without decoupling capacitors (top); with decoupling capacitor (bottom).

The plane cavities provide nearly all the decoupling to the design for frequencies above about 100MHz. So if we look at the example below, we have two cases that are shown: one is for a loosely coupled plane pair where we have about 30 mils separation between the VCC and the GND plane, and a case where we have a tightly coupled plane pair, the VCC and GND planes are exactly 5 mils apart.

In figure 3, with red line is represented the 30mils case and with blue line the tightly coupled case. It can be seen that for the tightly coupled plane pair, we are able to achieve about 6x performance benefits in the target impedance compared to the loosely coupled plane pair, so by coupling this plane pairs tightly together, it can be obtain a significant benefit.

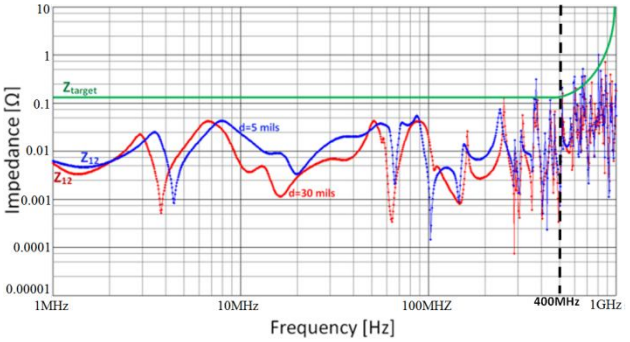


Figure 7. Transfer impedance of the plane with the decoupling capacitor from *Table 1*.

Figure 8. Visual representation of the propagation of the noise after using the capacitors from *Table 1* for d=30mils(top) d=5mils (bottom).

Table 1. Capacitors needed to decouple the plane.

Package	*C*	*ESR [Ω]*	*ESL [pH]*	*Freq [MHz]*	*Quantity*
0603	330pF	1.34796	525	300.5	11
0603	820pF	0.83572	525	190.6	7
0805	2.2nF	0.43923	710	105.5	4
0805	10nF	0.19169	710	49.5	2
0805	100nF	0.05432	710	15.6	1
0805	1µF	0.01539	710	4.9	1

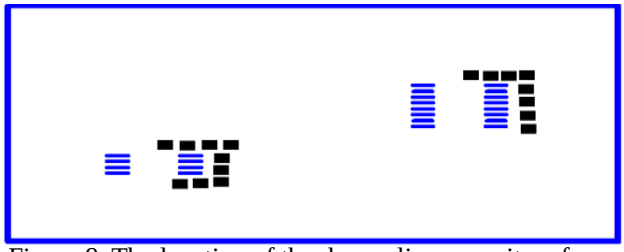


Figure 9. The location of the decoupling capacitors from *Table* 1 near the ICs.

The decoupling capacitors are the primary components of any power distribution network [8][9][10][11]. Ideally, we can use a bunch of capacitor and they would combine in parallel and suffice all decoupling and bypass needs, but unfortunately real capacitor have some inherit parasitic to them, and how the capacitors is mounted on the board add to those parasitic as well. For the next simulation, we used 100nF and 33uF decoupling capacitors attached to the power pins of the ICs. If we take in the consideration the fact that the local voltage regulator module can typically provide enough energy up to around 100MHz, at which point their inductance limits their energy deliver capabilities, we can see that using those two types of capacitors only creates a higher dip in the impedance profile around the their self resonance frequencies (Figure 5).

We can see this effect in the visual representation of noise created after the capacitors were added (Figure 6). The response of this problem is by using different capacitors with different resonances frequencies, and the number of capacitors used for decoupling is calculated by dividing the ESR to the target impedance. After using the capacitors from table 1, the power distribution network can provide enough energy up to around corner frequency, as is shown in figure 7 [4].

IV. CONCLUSIONS

The purpose of this paper is to determine how many capacitors we need, where the capacitors should be placed, how we should mount those capacitors and once were done all those things, we are trying to see whatever we'll meet the noise voltage requirements of the power and ground planes. To begin with, the things are focused in the frequency domain. For digital designers, they are mostly comfortable with time domain, but it is important to look at the frequency domain behavior of the power distribution network. When designing a power distribution network, we are trying to specify a target impedance that we want to achieve for our networks. So, in this case, we want to specify the voltage of this power net, the ripple tolerance and the maximum switching current and with these information, we are able to target a specific impedance for that power pin on the IC. Once we target impedance is settled, than it can be identified whatever the power distribution design is going to meet the impedance goals. We take a look at impedance versus frequency plot and it can be seen several resonances that occur in the design, some of them are from decoupling capacitors, the once that are very far in the frequency range, are resonances that are occurring because of the plane structure. Those are the high frequency resonances, self resonances of the actual plane from the PCB design. We want to be sure that for a given frequency range, those impedance goals are met, cause if we exceed those goals, it's the simple math of taking voltage, resistance and current and determine how much voltage is created based on the impedance and the current at that particularly frequency point. Once the impedance design goals in the frequency domain are established, we can see how much noise voltage is occurring on the power plane structure in the PCB. Taking the example analyzed in the paper, a plane structure that had two ICs, we ended up with slightly high noise voltage. So we can see spikes, which represent where that noise voltage is going to be significantly higher because it doesn't have high frequency decoupling (figure 4). But if we are looking at this from the overall noise voltage perspective, we see about 1800mV of noise on this power net.

Inductance is the number one thing that we want to look for when we are doing a power distribution. Inductance is what will cause the design to meet or fail the design performance goals. In order to optimize the power distribution for a target impedance, we are going to need to be able to manage the inductance. There are three mainly contributors of inductance within power distribution network: *the capacitor surface mounting*, *stack-up* and *via separation.*

To optimize the performance for a power distribution design, we also need to be able to properly select capacitors in order to achieve the impedance goals in the frequency domain. For a capacitor, the first thing we should know is that a capacitor is more than a capacitor, it also have an equivalent series resistance, as well as an equivalent series inductance. Those two parameters impact the self resonance frequency of the capacitor, as well the impedance we are able to target with that capacitor.

In addition to the decoupling capacitors on the design, the stack-up and plane design can have a significantly impact on overall decoupling strategy. The stack-up can play a key part in the decoupling process by decoupling at much higher frequencies then the decoupling capacitors are able to achieve. The plane cavities provide nearly all the decoupling to the design for frequencies above about 100MHz. If we look at our example, we got two cases that are shown: one is for a loosely coupled plane pair where we have about 30mils separation between the VCC and the GND plane, and a case where we have a tightly coupled plane pair which is the VCC and GND and they are only at 5mils apart. If we look at the simulation results, for the 30mils case and for the tightly coupled plane pair, we see that for a tightly coupled plane pair, we are able to achieve about 6x performance benefits in the target impedance compare to the loosely coupled plane pair. So is a significant benefit by coupling this plane pairs together.

If we take the example with no decoupling capacitors placed on the plane structure, we can see some interesting results and correlate the voltage ripple to that impedance. If we look at the voltage ripple plots, we see that the resonances of the plane look very similar, the reason is because the current load didn't change, the only thing that changed, is the actual coupling between the plane cavity, so we just reduced the size between plane cavities and for the case were we have 30mils versus the 5mils doesn't look that are a lot of differences in our resonances, but if we do a comparison between those two wave forms and look at them in rolled tip to each other, we can see that for the case were we had a wide plane pair that it wasn't coupled together, we had 1800mV of noise that was generated within that plane cavity, but for the case were we did have a tightly coupled plane pair together, we only have about 300mV of noise which correlates pretty well with what we saw in the impedance plots as well. After using the decoupling capacitors from table 1, we only have around 120mV of noise that maybe adequate enough for this particularly design.

In this case maybe we don't need to change the decoupling behavior or maybe we can choose to remove some high frequency decoupling capacitors or move them around in this plane shape in order to lower the overall effective noise on that power plane structure and reduces any resonances that are occurring with the voltage ripple on our power plane design.

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