RELIABLE POWER INTEGRITY ANALYSIS USING MATLAB

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Abstract: In Power Distribution Network (PDN) design of high-speed systems appears to be contradictory design philosophies, component selection and layout rules. A not properly designed power distribution increases the supply rail noise, but this impacts the system's performance in statistical manners, convoluted with many other variables. For this reason, the analysis and the design of a PDN is crucial in the real world of high-speed board systems. For a good reliability, the PDN should meet the target impedance ([2][5][9][10][13][16]) across the frequency range, up to the highest frequency of interest. Primarily, we need to characterize the high-frequency resonance peaks. Several commercial tools are available to analyze a PDN, [2][14][16][18], but the goal of this paper is to analyze a PDN using a tool developed in MATLAB that calculates and plots the self-impedance of an integrated circuit and the transfer impedance between two integrated circuits of a PCB consisting of a power-ground planes pair. The MATLAB tool gives the possibility to analyze the effects of the planes' parameters on the noise and to find a tested decoupling strategy to optimize the PDN.

Keywords: *power integrity, decoupling capacitors, target impedance, self-impedance, MATLAB tool.*

I. INTRODUCTION

In a PDN design, a major challenge is to supply a clean power to the switching circuits. One of the problems that appear in a PDN is the simultaneous switching noise (SSN) which is induced by the inductance of the power and ground planes. It has been recognized that power supply noise induced by a large number of simultaneously switching-circuits can limit the performance of the system, [2][10][13][14][16]. As the signal's rise time and supply voltages decrease, the power supply's noise appears as undesired voltage fluctuation on the power/ground planes. This is caused by the fast transient currents which excite cavity modes between planes during the switching activity of the digital circuits. This leads to unwanted effects in the PDN such as ground bounce, [2][10][16]. For an ideal PDN, the desired characteristics are zero self-impedance and zero transfer impedance between ports at all frequencies. Therefore, the goal in designing the PDN is to provide a low impedance power/ground connection to the devices, to reduce coupling between devices, and to decrease the resonant frequencies over the entire bandwidth of the signal. The first step in designing the PDN is to establish the target impedance based on the highest impedance that will create a voltage drop still below the acceptable ripple specification, [13][15][16]:

$$Z_{target} = \frac{V_{dd} \cdot ripple\%}{I_{transient}} \qquad (1)$$

where V_{dd} is the supply voltage for a specific integrated circuit, $I_{transient}$ is the worst case transient current, Z_{target} is the target impedance and *ripple%* is the ripple allowed. The optimum PDN impedance should be below the target impedance, but if it is much below the target impedance, it means that the PDN was over-designed and costs more than it needs to, [2][10][14][16].

According to [2][16], the Power Distribution Network can be partitioned in the frequency domain into simple regions: at the lowest frequency, from DC up to about 10KHz the VRM dominates the impedance seen by the integrated circuit. The next higher frequency range, in the 10kHz to 100kHz is dominated by the bulk decoupling capacitors, which are typically electrolytic and tantalum capacitors that provide a low impedance beyond the range of the VRM. The next region is influenced by the high frequency ceramic capacitors, from about 1MHz up to around 400MHz. The frequency region that the board planes can influence is up to about 500MHz.

Several software tools can simulate and predict the response of power distribution components and networks based on three major types of tools:

1) Analytical expressions;
2) Circuit simulators;
3) Electromagnetic field simulators.

Closed-form analytical solutions exist in a very small subset of structures, for example, waveguides or coaxial cables, [1][2][3][7][9][10][16]. Consequently, their utility in solving real-world problems is limited. Semi-analytic solutions can be obtained for several useful structures, including, for example, the self and transfer impedance profiles of parallel planes, [2][10][16]. Often, these types of solutions involve infinite series approximations or complicated integrals. Circuit simulators translate conductors and dielectrics into equivalent circuit elements, such as resistance, capacitances, inductances, and their coupling, [2][6][8][16].Then, frequency-domain simulations

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can be done on the entire circuit network to capture the device behavior. On the other hand, electromagnetic field solvers can solve a range of problems where are no expressions. Unlike circuit simulators, do not require an estimation of the equivalent circuit elements or parasitic coupling between the elements. The electromagnetic field solvers can include all electromagnetic effects from first principles leading to a deeper understanding of how devices or networks operate, [2][16][18].

A method to analyze a two plane pair is by using analytical expressions that describe the self and transfer impedance between rectangular ports, for simple plane shapes, [1][2][3][8][10][16].

II. CHARACTERIZATION OF A POWER DISTRIBUTION NETWORK (PDN)

According to [2][16], the PDN consists of all the interconnects from the voltage regulator module (VRM) to the pads on the chip and the metallization on the die that locally deliver power and return current. This includes the VRM itself, the bulk decoupling capacitors, the vias, the traces, the planes on the circuit board, the additional capacitors added to the board, the interconnects in the packages and the interconnects on the chips.

The power and ground plane pair is acting as high-frequency capacitors, serving as a conduit for the transportation of current, and supporting the return currents of the signal lines referenced to it, [2][16]. They are large metal structures separated by a thin dielectric and are invariably used in all high-frequency boards for power delivery, [2][16]. Power and ground planes transport the current from the SMD capacitors to the switching circuits. Therefore, the power and ground plane pair controls the inductance and the delay from the capacitor to the switching circuit, [2][10][16].

According to [2][10][16], at high frequencies much beyond the resonant frequency of the capacitor, the plane inductance dominates the impedance of the power distribution network. The capacitance formed between the power and ground planes can be used to decouple the power supply at high frequencies and hence becomes an useful contributor. A major problem with power and ground planes is their behavior as electromagnetic resonant cavities, where the dielectric constant of the insulator and the dimensions of the cavity determine the resonance frequency. When excited at the resonant frequency, the planes can become a significant source of noise in the board.

The voltage distribution across the planes depends on the resonance mode, while the resonance frequency is determined by the mode number, dielectric constant of the insulator, and the size of the planes. The resonance frequency of the planes is given by, [2][10][16]:

$$f_{kl} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{k\pi}{a}\right)^2 + \left(\frac{k\pi}{b}\right)^2} \qquad (2)$$

where k and l are given by the resonance mode and a and b are the lateral dimensions of the board. The distribution of the voltage across the planes depends on the source location. At the resonant frequencies, the voltage distribution is maximum and minimum at certain points on the planes. This variation in the voltage fluctuation across the plane is called plane bounce, [2][16].

III. ANALYTICAL MODEL OF A LOW-LOSS POWER-GROUND PLANE IMPEDANCE

In contrast to signal traces where the signal travels along the axis of the signal conductor, the wave generated by an injected signal between the planes launches a radial expanding wave. The self and transfer impedance of transmission planes with rectangular shapes can be analytically calculated. Impedances of square-shaped parallel planes are widely analyzed in the literature for planar microwave circuits and printed antennas, [1][2][3][8][10][16]. Assuming infinitesimally small port sizes, open boundaries at the edges and a pair of parallel, rectangular planes with side dimensions a and b along x and y axes, with plane separation d along the z axis, based on the losses of the materials that compose the power and ground planes ,[10],the generalized impedance between ports i and j can be written as:

$$Z_{st} = j\omega\mu d\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{\chi_{mn}^2}{ab\left(k_{xm}^2 + k_{yn}^2 - k^2\right)} f(x_s y_s x_t y_t) \qquad (3)$$

Where:

$$f(x_s y_s x_t y_t) = \cos\left(\frac{2m\pi x_s}{2a}\right)\cos\left(\frac{2m\pi y_s}{2b}\right)\cdot \cdot\cos\left(\frac{2m\pi xt}{2a}\right)\cos\left(\frac{2m\pi yt}{2b}\right) \qquad (4)$$

In this relation m represents the mth mode associated with the x-dimensions, n represents the nth mode associated with the y-dimensions, k represents the complex wave number for low-loss case. The constant χ_{mn}^2 can be defined as:

$$\begin{cases} \chi_{mn}^2 = 1 & \text{, for m=n=0} \\ \chi_{mn}^2 = 2, & \text{, for m=0 or n=0} \\ \chi_{mn}^2 = 4 & \end{cases} \qquad (5)$$

and $k_{xm} = \frac{m\pi}{a}$, $k_{yn} = \frac{n\pi}{b}$,

$$k = k' - k''$$

$$k' = \omega\sqrt{\varepsilon\mu} = \omega\sqrt{\varepsilon_r\varepsilon_0\mu_0} = \sqrt{\varepsilon_r}\,\frac{\omega}{c} \qquad (6)$$

$$k'' = \omega\sqrt{\varepsilon_r\varepsilon_0\mu_0}\left(\frac{tg\delta_d}{2} + \frac{\delta}{2d}\right)$$

where $tg\delta_d$ is the loss tangent of the dielectric, ω is the angular frequency, μ is the permeability of the dielectric and c is the speed of light. δ is the skin depth at the frequency of interest determined by:

$$\delta = \sqrt{\frac{1}{\pi f\sigma_c\mu}} \qquad (7)$$

where σ_c is the conductivity of the metal associated to the power and ground planes.

As it can be seen, the analytical expression has a double infinite series, which for practicable calculations must be truncated, so instead of using *k* and *l* to be infinite, we have to equalize *k* and *l* with a finite number. If the summation limits are changed, at low frequency, the impedance minima converge very slowly and at high frequency, after the last impedance peak in the summation, the impedance drops monotonically, as opposed to a rising function that we should expect from the inductive behavior. To ensure sufficient frequency coverage for the peaks, the summation limits have to be chosen such that the highest included modal peak is safely above the highest frequency of interest. In [8] was introduced a MATLAB tool to analyze a power and ground plane pair, based on the analytical expressions. To correlate MATLAB and SPICE impedances, a power and ground plane pair with lateral dimensions of *32cmx16cm*, with a dielectric with *254μm* and a dielectric constant of 4.7 was selected. Figure 1 shows a 3D view of this power and ground plane pair.

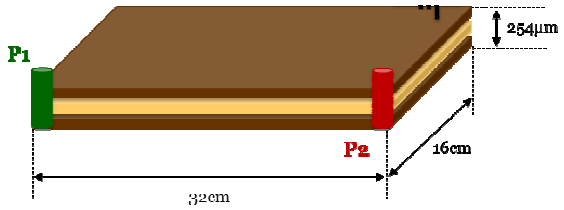

Figure 1. 3D view of a power and ground plane pair.

Self-impedances and transfer impedances were simulated in the 1MHz – 1GHz range at the edge of the test board. Figure 2 shows the self-impedances and the transfer impedance profiles.

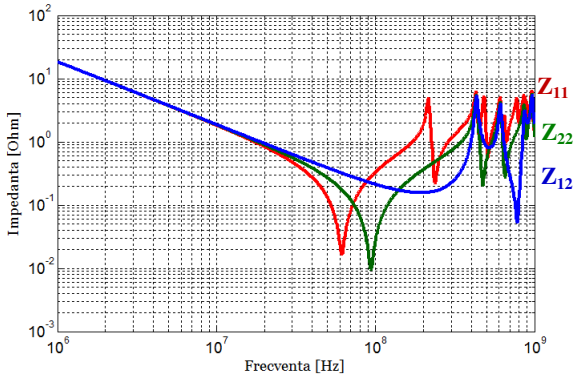

Figure 2. The self-impedances, Z_{11} and Z_{22}, and the transfer impedance, Z_{12}, of the PDN.

Based on those profiles, the voltage distribution across the planes was determined. The response can be shown in two different ways: as a 2D plot and as a 3D plot. Figure 3 and Figure 4 show an example of a 2D and 3D voltage distribution across the planes at a resonance frequency of 483MHz.

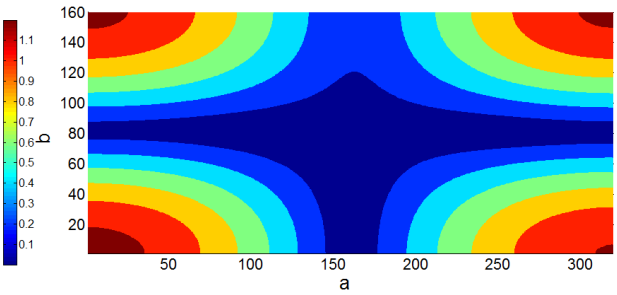

Figure 3. 2D voltage distribution across the planes at 483MHz. The dimensions of the planes are in mm.

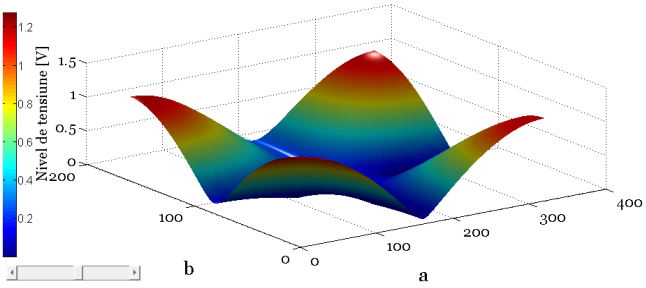

Figure 4. 3D voltage distribution across the planes at 483MHz. The dimensions of the planes are in mm.

IV. THE FREQUENCY DOMAIN BEHAVIOR OF A PDN WITHOUT DECOUPLING CAPACITORS

According to [2][16], the low frequency impedance is set by the voltage regulator module (VRM). Regardless of the type of regulator, all VRMs have an output impedance profile. Figure 5 shows a typical equivalent circuit model of the VRM and Figure 6 shows the impedance profile of a VRM with L_{slew}=70nH, L_{out}=5nH, R_{flat}=30mΩ and R_{out}=1mΩ.

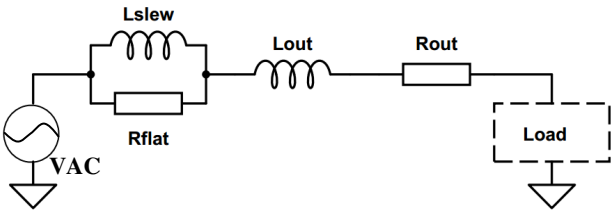

Figure 5. Typical equivalent circuit model of the VRM.

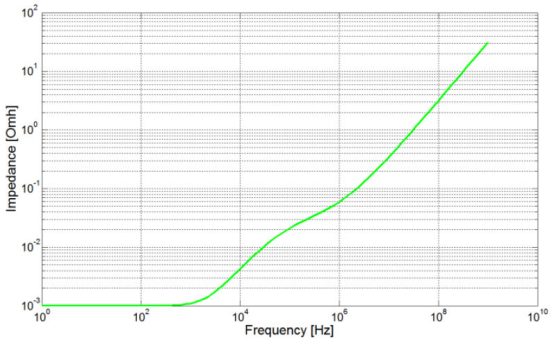

Figure 6. The impedance profile of the VRM with Lslew=70nH, Lout=5nH, Rflat=30mΩ, and Rout=1mΩ.

When it comes to establish the actual target value of the capacitance, the interactions of the VRM's effective

inductance and capacitor's capacitance must be taken into account with a SPICE or MATLAB simulation. Figure 7 shows the impedance of the PDN without decoupling capacitors.

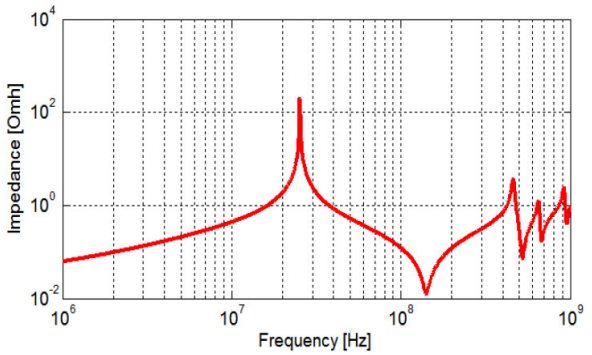

Figure 7. The impedance of the PDN without decoupling capacitors.

At lowest frequency, the VRM dominates the impedance the chip sees looking into the PDN. The VRM performance dominates from DC up to about 100kHz. Above 1kHz, the impedance seems to increase, until it matches the impedance of the power and ground planes.

V. DECOUPLING STRATEGIES BASED ON PLANES' PARAMETERS AND DECOUPLING CAPACITORS

Next, a maximum impedance of *Ztarget=1Ω (the blue transparent plane from Figure 8)* was selected. For a good performance, the impedance of the PDN must be maintained below this maximum impedance ($Z_{PDN}<Z_{target}$).

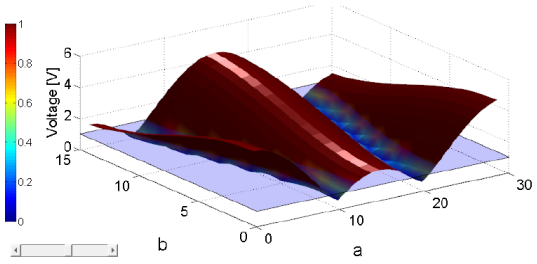

Figure 8. Voltage distribution across the planes at 461MHz.

As it's shown in Figure 7, the first resonance peak occurs near 461MHz, determining large voltage fluctuations (Figure 8). Here, it is recommended to avoid placing ICs which draw large currents near the resonant voltage peaks/dips because it is easier to excite the resonant modes.

To suppress the noise, a basic decoupling strategy is needed. According to [2][4][10][16], a method to reduce the noise, is by decreasing the distance between the planes and a lower dielectric constant. The simulations were repeated for a 50.8µm separation between the planes and 4.3 dielectric constant's value. Figure 9 shows the voltage distribution for 50.8µm separation between the planes and 4.3 dielectric constant's value.

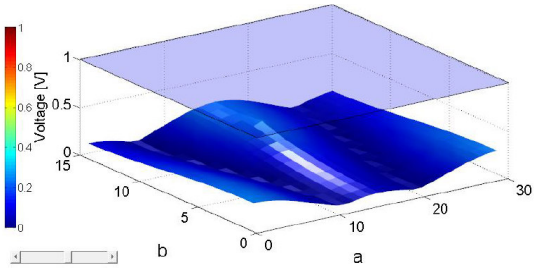

Figure 9. Voltage distribution across the planes at 461MHz for 50.8µm separation between the planes and 4.3 dielectric constant's value.

The results show that the noise was suppressed and the PDN designed is meeting the target impedance.

The simulations were repeated to see if the PDN meets 100mΩ target impedance. Figure 10 shows the voltage distribution across the planes when the PDN must meet a 100mΩ target impedance.

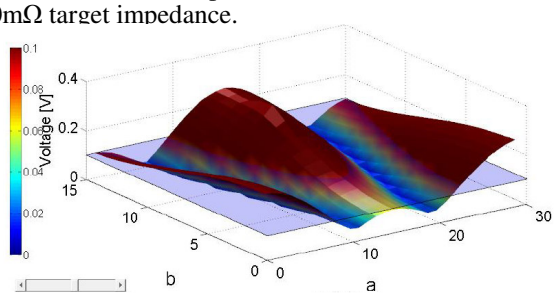

Figure 10. Voltage distribution across the planes at 461MHz for 50.8µm separation between the planes and 4.3 dielectric constant's value and a 100mΩ targe impedance.

Here, the resonance peak determines large voltage fluctuations, above 100mV.

Another strategy to engineer the PDN impedance profile must be applied. This strategy is to select the right number and value of capacitors to keep the peak impedance below the target value from where the VRM no longer provides low impedance, up to about 200MHz.

Using target impedance for PDN design involves choosing the number of decoupling capacitors of each value such that the parallel combination approximates the target impedance, by dividing the target impedance into the ESR of the capacitor. The equivalent R, L, and C of n capacitors in parallel are, [2][9][13][15][17]:

$$C_n = nC \tag{8}$$

$$ESR_n = \frac{1}{n} ESR \tag{9}$$

$$ESL_n = \frac{1}{n} ESL \tag{10}$$

Decoupling capacitors with different values connected between power and ground planes may exhibit resonances between different capacitors or between capacitors and planes. If the inductance connecting the parts is minimized, the resonance peaks are also reduced. Using SMD capacitors, it can be approached a several hundred pH inductance, but sometimes, the dimensions of the capacitors

and of the PCB do not allow us to lower it below 100pH, and in some applications this value is still too high to reduce the resonance peaks. Also, the ESR of the decoupling capacitors could be used to obtain a flat frequency impedance response, but the designer is constrained by the fact that the ESR parameter for today's capacitors is not user definable, [2][9][13][15][17]. The precise number and optimized values of decoupling capacitors needed, will depend on the bulk capacitors, the capacitance in the board, the target impedance, the maximum frequency and the ESL of each capacitor, [2][16]. The combination of these terms varies dramatically from product to product so it is not possible to give one capacitor distribution that will always work. However the methodology can be applied to many designs. This methodology was pioneered by Larry Smith and has been named "Frequency Domain Target Impedance (*FDTI*) method"[14]. The process leverages the simulated impedance profile of a collection of capacitors including their ESL and ESR, including the capacitance in the planes at high frequency and bulk capacitors and VRM at low frequency.

We suppose that the ESL of each capacitor is the same and equals 1nH, and the maximum frequency of interest is 500MHz. The theoretical minimum number of capacitors required to meet the target impedance value for the above condition is, [2][14][16]:

$$n > 2\pi F_{\max}\left(\frac{ESL}{Z_{target}}\right) \qquad (11)$$

$$n = 2\pi \cdot 0{,}5\left(\frac{1}{0.1}\right) = 32 \qquad (12)$$

In the first example, we add 32 decoupling capacitors with a capacitance of 1μF. Figure 11 shows the impedance of the PDN after the decoupling capacitors were added to the PDN.

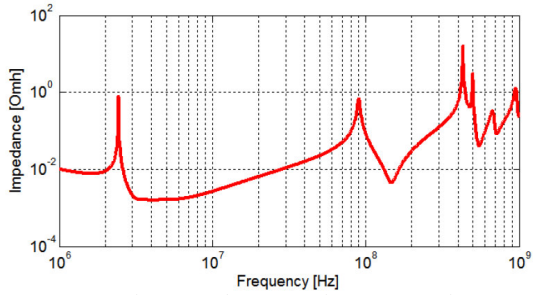

Figure 11. The impedance of the PDN with 32 1μF decoupling capacitors.

After attaching the decoupling capacitors, the impedance of the PDN is maintained below target impedance (*target impedance*) up to around 450MHz. Above this frequency, the impedance of the PDN starts to increase determining a voltage fluctuation across the planes (See Figure 12).

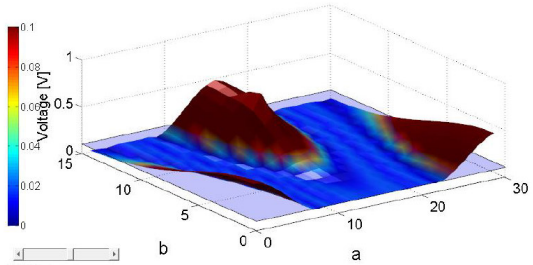

Figure 12. Voltage distribution across the planes at 461MHz for 50.8μm separation between the planes and 4.3 dielectric constant's value, with 32 1μF decoupling capacitors.

To optimize the impedance of the PDN it is necessary to add the best combination of minimum 32 decoupling capacitors. Starting at the low frequency end, a decoupling capacitor value is selected and simulated, and for each value enough capacitors are added to bring the impedance peak below the impedance that we want to achieve. The best combination of decoupling capacitors was calculated according to [14]. Figure 13 shows the impedance profile of the combination with 32 different decoupling capacitors.

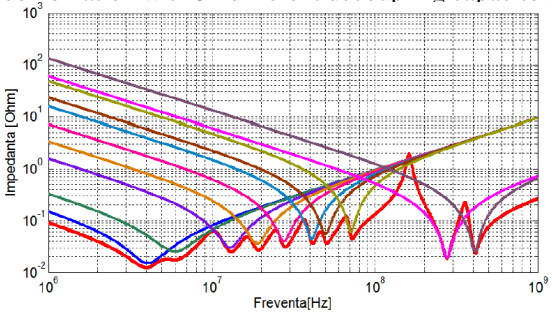

Figure 13. Impedance profile of the decoupling capacitors used to decouple the PDN.

The decoupling capacitors were attached to the PDN. Figure 13 shows the 3D view of the new PDN with the VRM, the ports P1 and P2, the power and ground planes and a total of 32 decoupling capacitors placed near port P1.

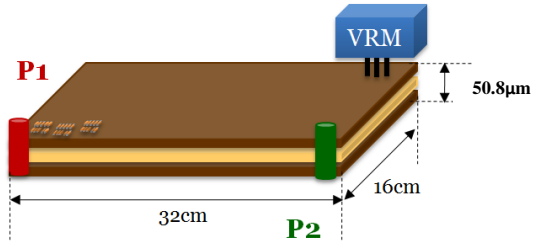

Figure 14. 3D view of the new PDN with the VRM, the ports P1 and P2, the power and ground planes and a total of 35 decoupling capacitors placed near port P1.

Figure 15 shows the impedance profile of the new PD and Figure 16 shows the voltage distribution across the planes 461MHz, after the decoupling capacitors were attached to the PDN.

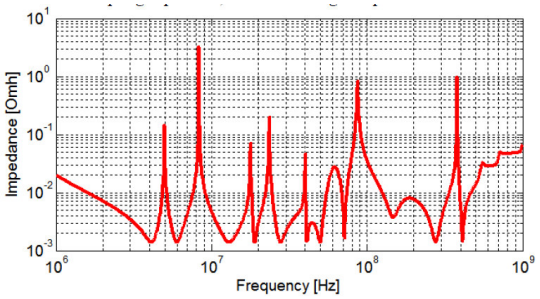

Figure 15. Impedance profile of the new PDN.

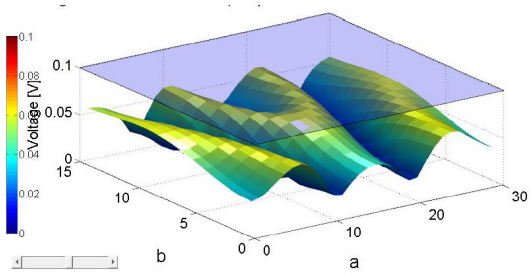

Figure 16. Voltage distribution across the planes at 461MHz for 50.8µm separation between the planes and 4.3 dielectric constant's value, with an optimum combination of decoupling capacitors.

Using an optimum combination of decoupling capacitors (according to [2][5][9][14][16]), was obtained an impedance profile that meets the target impedance up to 500MHz (See Figure 15). Also, the voltage noise was reduced below 100mV across all the surfaces of the planes. The capacitance formed between the power and ground planes and by the decoupling capacitors, up to 500MHz, and hence becomes an useful contributor.

VI. CONCLUSIONS

This paper introduces a new software tool for simulating a Power Distribution Network. This MATLAB tool is based on an analytical method that calculates the self-impedance and transfer impedance for lossy power and ground planes. The MATLAB results obtain in the frequency domain were compared with SPICE results. Also, using the impedance profile was presented a MATLAB example on how to select an optimum combination of decoupling capacitors to best design a PDN. The location of the decoupling capacitor was determined from the voltage distribution across the planes.

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