AN OPERATIONAL TRANSCONDUCTANCE AMPLIFIER SIZING METHODOLOGY WITH GENETIC ALGORITHM-BASED OPTIMIZATION

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Abstract: This paper proposes a methodology for the parametric design of operational transconductance amplifiers. In the proposed methodology, amplifier sizing is performed in two stages: an equation-based design scheme performs an approximate design, followed by optimization of the design results with genetic algorithms. The feasibility of this method was investigated with extensive simulation. For demonstration purpose, a folded-cascode operational transconductance amplifier was subject to design.

Keywords: *Folded-cascode operational transconductance amplifier, evolutionary circuit design, genetic algorithms.*

I. INTRODUCTION

Development of modern mixed-signal systems-on-a-chip (MS-SOC) is a continuous race to achieve higher processing capabilities. It is a natural consequence that the integrated circuits (IC) become ever more complex. With the growth in IC complexity comes a growth in designer effort, design time, and implicitly design costs. IC development must however be carried out under short design times and small development costs. Therefore, the International Technology Roadmap for Semiconductor (ITRS) report on Design [1] states the need for electronic design automation all along the IC development flow.

Signal processing is nowadays mostly digital, and digital synthesis is almost fully automated. Yet, the analog processing part, which only takes up a small fraction of the modern ICs, is indispensable in MS-SOCs and cannot be neglected. Specific examples of processing functions which are analog by nature are biasing, interfacing, signal-conditioning, signal-conversion, etc [2].

The process of analog circuit design consists of topology synthesis followed by topology sizing. Considering the nature of the analog circuitry, analog IC design translates to a complex multi-objective highly constrained design problem [3, 4]. To facilitate the task of the analog designer, automatic analog synthesis has been a matter for research in the past few decades.

The operational transconductance amplifier (OTA) is the center element in any analog processing chain, as for example analog intermediate frequency filters for wireless communications [5]. Thus, it is the starting point in any analog design [2, 6]. Systematic OTA design plans are formulated based on simplified first-order transistor models, and don't account for parasitic effects which limit the circuit performance. Thus, it is not surprising to see that the design doesn't perform as expected and it doesn't fully satisfy the design specifications. Circuit designers usually proceed to over-sizing the IC, i.e. designing the OTA for a higher DC gain, SR and GBW, such that it meets the design specifications even in the presence of transistor parasitics. Over-sizing however comes with the cost of higher chip area and increased power consumption.

Automatic amplifier design has been a matter of research for the last few decades and consistent contributions have been reported [7]. Yet, a solution hasn't been fully adopted so far, in either academia or industry, for the automatic design of the analog amplifier. Thus, the problem is far from being solved.

This paper deals with the parameter level design of the analog amplifier and presents a novel automatic OTA sizing algorithm. For validation of the proposed algorithm, the automatic sizing of a folded-cascode OTA (FC-OTA) is illustrated.

This paper is organized as follows. Section 2 presents a review of automatic parameter-level OTA design algorithms in literature. Section 3 presents the FC-OTA modeling equations which are used for determining a systematic design plan. Section 4 describes the proposed design algorithm. Finally, the simulation results which validate the proposed design algorithm are presented in Section 5.

II. RELATED WORK

A review of automatic parameter level design algorithms is presented in this section. Considering the implementation of the automatic parameter level design algorithm, a first classification distinguishes between knowledge-based and optimization-based design schemes respectively [7].

Knowledge-based automatic design schemes implement the knowledge of the analog designer into a design plan. The design algorithm then executes the design plan in order to provide a fully designed circuit. A conclusive example for knowledge-based OTA design is IDAC [8] developed by the Centre Suisse d'Electronique et de Microelectronique, which employs manually derived design plans. The formulation of the design plan however implied several simplifications to the circuit analysis equations, and therefore the provided result needed further optimization.

A similar application for automatic OTA design is OASYS [9], which implements manually derived design plans for basic analog building blocks, e.g. current mirror, current source, simple differential pair, etc. Then, the sizing

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of the analog circuit is performed hierarchically starting from the individual building blocks. Fine-tuning the provided result for complying with the design specifications is again a matter of further optimization.

A knowledge-based automatic OTA design methodology implemented around design heuristics was proposed by Haubeneder et al in [10], in the shape of a batch-file driven design application. The OTA is designed in multiple iterations by optimizing one performance parameter at a time.

An alternative to knowledge-based design is the employment of optimization algorithms in the automatic design methodology. The optimization-based design methods can further be classified considering the nature of the optimization algorithm into deterministic and stochastic optimization.

The automatic design methodology which employs deterministic optimization consists in applying some gradient-based optimization schemes, e.g. steepest descent, downhill, etc., to determine the circuit parameters which optimally approximate the desired design specifications. For example, Delight.Spice [11] uses the method of feasible directions to fine-tune a predesigned analog circuit. As another example, OAC [12] uses non-linear optimization for operational amplifier sizing.

The main disadvantage of deterministic optimization is the issue with sensitivity vs. initial conditions. A proper choice of the initial conditions is mandatory for the optimization process to perform satisfactorily. OPASYN [13] for example applies steepest descent optimization to multiple randomly generated starting points.

Random initialization of the optimization process is however not a solution. Therefore, deterministic optimization is rather used in multi-layer design procedures as a secondary design stage to a knowledge-based deterministic design scheme for fine-tuning the results provided by the design plan. A further disadvantage of deterministic optimization schemes is that they tend to get stuck in points of local optima. Means to escape local optima can be defined, however, they add to the complexity of the design algorithm even further.

The automatic design methodology which employs stochastic optimization, e.g. simulated annealing, swarm optimization, evolutionary algorithm, etc. introduces a random component to the optimization process, thus, the issue with getting stuck in points of local optima is inherently solved.

For example, FRIDGE [14] and AMGIE [15] both apply simulated annealing to solve the circuit sizing formulated as a global optimization problem. Liu et al applied a differential evolution optimization scheme for the sizing of an operational amplifier [16]. Another significant example for the use of genetic computation is Darwin [17] for sizing of OTAs.

III. FOLDED-CASCODE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER MODELLING EQUATIONS

The circuit schematic of the FC-OTA is illustrated in figure 1.

A set of OTA design specifications, expressed simultaneously in different domains, is listed as follows [6]:

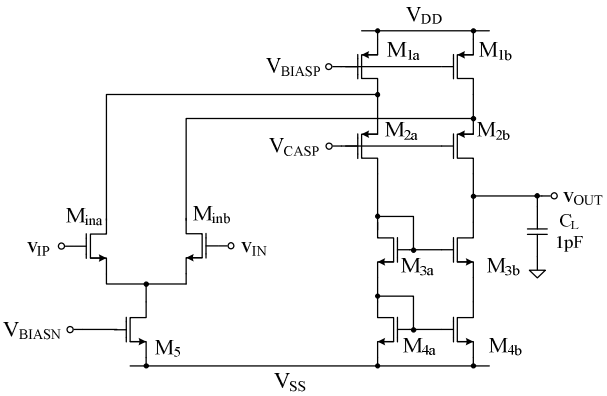

Figure 1. Schematic of the folded-cascode operational transconductance amplifier.

- DC domain: DC gain (A_0), input common-mode voltage, input dynamic range, output dynamic
- range, maximum output current,
- AC domain: dominant pole frequency – bandwidth (BW), gain-bandwidth product (GBW), AC node resistance and node capacitance,
- Transient domain: slew rate (SR), pulse response settling time, stability,
- Offset and noise specifications,
- Maximum power consumption,
- etc.

For simplicity in illustrating the proposed design algorithm, we will only consider A_0, GBW and SR as design specifications.

The FC-OTA performance measures are expressed using the amplifier small signal parameters, as expressed in equations (1 – 4) [6],

$$A_0 = G_{m,in} \cdot R_{out} \tag{1}$$

$$BW = \frac{1}{2\pi R_{out} C_L} \tag{2}$$

$$GBW = \frac{G_{m,in}}{2\pi C_L} \tag{3}$$

$$SR = \frac{I_{D5}}{C_L} \tag{4}$$

where $G_{m,in}$ is the transconductance of the input differential stage, R_{out} is the FC-OTA output resistance, C_L is the load capacitance connected to the FC-OTA output and I_{D5} is the bias current of the differential stage. The amplifier small signal parameters are expressed using the transistor small signal parameters, as expressed in equations (5) and (6) [6],

$$G_{m,in} = g_{m,in} \tag{5}$$

$$R_{out} = g_{m3} r_{DS3} r_{DS4} \,\|\, g_{m2} r_{DS2} r_{DS1} \tag{6}$$

where g_m is the transconductance and r_{DS} is the drain-source resistance of the transistor respectively, and the indices indicate the transistor index numbers. The transistor small-signal parameters are in their turn expressed using circuit parameters, namely transistor aspect ratios, bias voltages and DC currents [6]

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} \quad (7)$$

$$r_{DS} = \frac{V_A}{I_D} \quad (8)$$

$$I_D = \frac{K}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (9)$$

where I_D is the drain current, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, W/L is the geometry, K is factor kappa which consists of the charge mobility and oxide capacitance and V_A is the Early voltage of the MOS transistor respectively. To be noted is that K, V_{th} and V_A are process parameters, while I_D and V_{GS} are the design parameters.

According to equations (1 – 9), the FC-OTA circuit performance measures can easily be estimated knowing the circuit parameter values. Reversely, an FC-OTA design plan can be formulated for a given set of design specifications.

For proper operation, the OTA must satisfy the multiple design specifications which are interdependent, and even conflicting. The interdependence of the design specifications is expressed in equations (10 – 12) and is explained as follows. The ratio between SR and GBW is stated by the overdrive voltage V_{GS}-V_{th}, and therefore is fixed for a given transistor bias point. Similarly, the ratio between $G_{m,in}$ and SR is stated by the $C_L/(V_{GS}-V_{th})$ ratio, and therefore is fixed for a given transistor bias point and OTA load capacitance. Then, increasing the bias current $I_{D,in}$ to increase either $G_{m,in}$, GBW or SR, as stated in equations (3 – 5), will affect all three performance parameters simultaneously.

$$\frac{SR}{GBW} = 2\pi(V_{GS} - V_{th}) \quad (10)$$

$$\frac{G_{m.in}}{SR} = \frac{C_L}{V_{GS} - V_{th}} \quad (11)$$

$$\frac{SR}{GBW} = 4\pi\frac{I_{D,in}}{G_{m,in}} \quad (12)$$

IV. PROPOSED AUTOMATIC AMPLIFIER DESIGN ALGORITHM

A systematic FC-OTA design plan, formulated starting from equations (1-12), is based on simplified first-order transistor modeling equations, and doesn't account for parasitic effects which limit the circuit performance. Thus, it is not surprising to see that the design doesn't perform as expected and it doesn't fully satisfy the design specifications.

Circuit designers usually proceed to over-sizing the IC, i.e. designing the amplifier for a higher DC gain, SR and GBW, such that it meets the design specifications even in the presence of transistor parasitics. Over-sizing however comes with the cost of higher chip area and increased power consumption, as expressed in equations (10 – 11). Under such circumstances, alternative design techniques based on computational intelligence are worth investigating.

Most automatic OTA design algorithms reviewed in Section II implement two design levels: first a raw design of the analog circuit is performed, followed by a secondary level for fine-tuning the raw design. In this article we have proposed a novel approach to handle the two design levels, while keeping the same double-layer hierarchy. The block diagram of the proposed design approach is illustrated in figure 2.

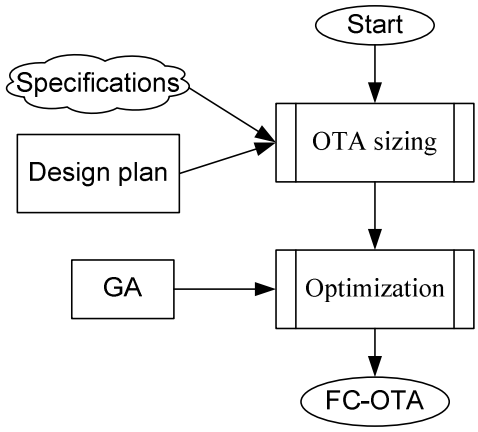

Figure 2. Block diagram of the proposed automatic OTA design algorithm.

In the proposed design approach, we have implemented a two-layer design algorithm which performs a knowledge-based design of the FC-OTA in the first design level, followed by an optimization stage in the second design layer.

We have chosen an equation-based systematic sizing methodology for the first design stage because systematic OTA sizing schemes are proven for the validity of the provided results. Naturally, the results provided by the design plan need further fine-tuning. Therefore, the results of equation-based OTA sizing are fed as initial conditions to the optimization design layer.

At this stage, a choice between deterministic and stochastic optimization had to be drawn. It is sensible to assume that the feasibility region of the design solution is found around the initial conditions supplied by the sizing stage. Thus, a deterministic optimization scheme would seem suitable. In contrast, a stochastic optimization scheme might easily leave the feasibility region as a result of the random component in the optimization process. The fitness landscape for the OTA design problem however exhibits numerous points of local minima, creating the danger for a deterministic optimization scheme to get stuck in points of local optima, and strategies to escape local optima would further complicate the design algorithm. Therefore, we have chosen evolutionary optimization to ensure the design algorithm's capacity to escape from local optima.

From the family of evolutionary algorithms we have chosen genetic algorithms (GA). Genetic algorithm (GA) is an iterative optimization scheme which applies operators inspired form natural evolution in order to minimize the value of an objective function. The block diagram of a GA is illustrated in figure 3.

GA operates on a population of solution candidates rather than on single solutions. A randomly created initial population is iteratively evolved by application of genetic operators: selection, cross-over, mutation and optionally survival. The evolutionary process aims to produce individuals better and batter fitted to solve the optimization problem.

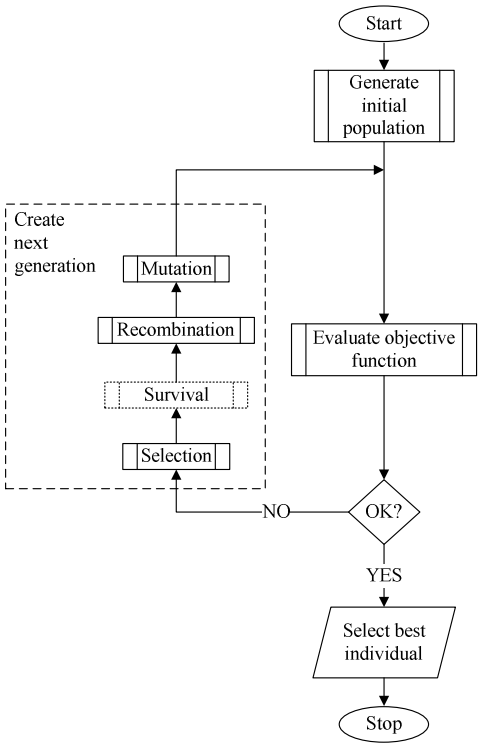

Figure 3. Block diagram of the Genetic Algorithm [18].

Our main reason for choosing GA was that, provided a sufficiently long runtime, they are statistically proven to find the global optimum. The employment of GA to solve the optimization problem is further motivated by its capacity to operate over large, complex, and highly constrained search spaces. Moreover, GAs have high capacity to escape points of local optima and exhibit good insensitivity vs. initial conditions [18].

Regarding the implementation of the GA evaluation engine, we have chosen a simulation –based evaluation. The performance measures of the circuit under design (CUD) are computed using the Eldo circuit simulator available form Mentor Graphics, rather than a set of circuit-analysis equations as is the case for equation-based evaluation.

The main issue with employing GAs in the second design level is that it might easily leave the feasibility area during the evolutionary process. To handle this issue, the novelty of our optimization approach with GA is that we deviate the design parameters around the value supplied by the sizing design stage, rather than compute the design parameters as is the case with classical evolutionary computation. Deviation of the transistor geometry around the initially supplied $(W/L)^*$ value is expressed in equation:

$$\frac{W}{L}=\left(\frac{W}{L}\right)^{*}+(-1)^{b_1}\cdot\sum_{i=2}^{n}\left(\frac{W}{L}\right)^{*}\cdot\frac{b_i}{2^i} \tag{13}$$

where b_k, $k=1\ldots n$ are bits which encode the addition or subtraction of transistor geometry fractions. The geometry deviation process around the initial $(W/L)^*$ value is illustrated in figure 4.

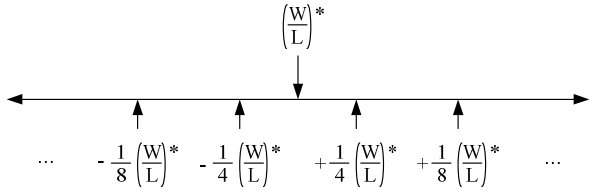

Figure 4. Illustration of the transistor geometry deviation.

Transistor geometry deviation is encoded as an n-bit long binary string

$$[b1\ b2\ b3\ \ldots\ bn] \tag{14}$$

where b_1 is the sign bit and states the direction of the deviation, towards either higher or lower values, and $b_2 \ldots b_n$ indicate the appearance of the $(1/2^i)^{th}$ geometry fraction in the final value. The length of the binary vector n gives the resolution for geometry deviation. Therefore, a fine resolution is then achieved for a high value of n. A high value of n however accounts for an increased GA computational burden and consequently longer design time. Our tests show that $n=6$ is a good compromise for both GA speed and solution accuracy.

The GA chromosome encodes the deviation data for all transistors in the FC-OTA structure. To shorten the chromosome length, we have represented the matching transistors, i.e. the differential pair, and the transistors building the folded-cascode load, with one single deviation vector. Therefore, the GA chromosome is a binary vector of $6n$ bits, and encodes the deviation data for 6 transistors:

$$[Min\ M5\ M1\ M2\ M3\ M4] \tag{15}$$

The error in meeting the individual designs specifications is expressed according to equation (16).

$$\begin{cases} errA_0 = \left|A_0{}^{spec} - A_0\right| \\ errGBW = \left|GBW^{spec} - GBW\right| \\ errSR = \left|SR^{spec} - SR\right| \end{cases} \tag{16}$$

The GA objective function is expressed as a weighted sum of the individual error values

$$err = a_1 \cdot errA_0 + a_2 \cdot errGBW + a_3 \cdot errSR \tag{17}$$

where a_1, a_2 and a_3 are the weights of the DC gain, gain bandwidth product and the slew rate errors respectively.

Minimizing the objective function (17) operates towards equating A_0, GBW and SR to $A_0{}^{spec}$, GBW^{spec} and SR^{spec} respectively. This expression is suitable for an "equality" type definition of the OTA specifications. However, OTA design specifications are usually expressed with "greater than" type definitions. Allowing the GA to operate towards optimizing the "greater than" design specifications would result in an over-sized OTA with an unacceptably high power consumption and chip area. Rather than introducing power and size as two additional optimization objectives to

restrict OTA over-sizing, we have translated the OTA specifications to "equality" type requirements. Weight factors a_1, a_2 and a_3 then state the precedence of each individual objective, and inherently allow a certain degree of over-sizing to satisfactorily meet all design specifications. The used approach provides good results in most optimization problems, exhibiting the character of generality.

V. SIMULATION RESULTS

The FC-OTA was implemented in Mentor Graphics, using the 3V analog extension of a 90 nm digital process. The equation-based design plan and the GA to build the automatic design algorithm were implemented in Matlab.

The interface of the automatic design application is illustrated in figure 5.

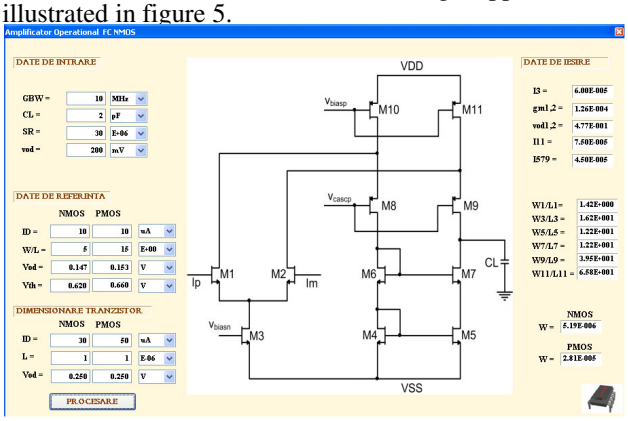

Figure 5. The interface of the automatic design application.

We have validated the proposed design algorithm with extensive simulation. Some conclusive results are presented as follows.

For the first design run we have considered the set of design specifications:

- A0 > 60 dB
- GBW > 10 MHz
- SR > 30 V/µs

Table 1 lists the transistor geometries obtained after the equation-based design stage and after the GA-based optimization stage. The FC-OTA performance measures are listed in Table 2.

To be noted is that power consumption (PWR) and estimated chip area were not included in the expression of the objective function, and therefore they were not subject for optimization. We have only listed these values for comparison. We have estimated the FC-OTA area as the sum of the transistor geometries, since it is sensible to assume that wiring would occupy approximately the same area. For comparison, we have also listed the transistor geometries and performance measures achieved via OTA over-sizing.

The performance parameters listed in table 2 clearly indicate that the proposed design algorithm satisfies the design specifications, but for a smaller power consumption and smaller estimated chip area in comparison to OTA over-sizing.

The GA evolution lasted for 18 generations. The evolution of the fitness value vs. generations is plotted in figure 6. Design algorithm convergence is illustrated by the decrease in the average distance between individuals, plotted vs. generations in figure 7.

Table 1. FC-OTA transistors geometries in the first design run.

	Equation-based design	Over-sizing	GA-optimized design
M_{in}	1.42µ/1µ	1.92µ/1µ	1.52µ/1µ
M_1	65.8µ/1µ	70.2µ/1µ	65.6µ/1µ
M_2	39.5µ/1µ	42.1µ/1µ	52.6µ/1µ
M_3	12.2µ/1µ	13µ/1µ	13.6µ/1µ
M_4	12.2µ/1µ	13µ/1µ	13.4µ/1µ
M_5	16.2µ/1µ	17.3µ/1µ	19.8µ/1µ

Table 2. FC-OTA performance parameters in the first design run.

	Equation-based design	Over-sizing	GA-optimized design
A_0	65 dB	66.4 dB	73 dB
f_p / BW	5.1 kHz	5.5 kHz	2.5 kHz
GBW	8.9 MHz	11.2 MHz	10 MHz
SR	26.6 V/µs	32.8 V/µs	30 V/µs
PWR	926 µW	977.9 µW	956.6 µW
Area	278.4 μ^2	297.7 μ^2	280.2 μ^2

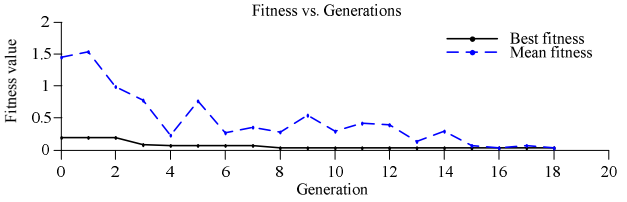

Figure 6. Evolution of the fitness value vs. generations for the first design run.

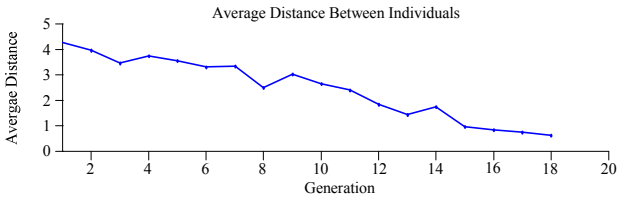

Figure 7. Evolution of the average distance between individuals vs. generations for the first design run.

In the second design run, we have considered a slew-rate:

- SR > 40 V/µs

in the GA-based optimization stage. The GA initial conditions were the same as in the first design run, thus, our target was to see how far can the GA improve an equation-based design. Table 3 lists transistor geometries obtained after the equation-based design stage and after the GA-based optimization stage. The FC-OTA performance measures are listed in Table 4. Again, we have listed the transistor geometries and performance measures achieved via OTA over-sizing for comparison purposes.

The performance parameters listed in table 4 clearly indicate that the proposed design algorithm satisfies the design specifications. Again, the power consumption and the estimated chip area are smaller in comparison to over-sizing.

Table 3. FC-OTA transistors geometries in the second design run.

	Equation-based design	Over-sizing	GA-optimized design
M_{in}	1.42µ/1µ	1.46µ/1µ	1.91µ/1µ
M_1	65.8µ/1µ	92.2µ/1µ	65.8µ/1µ
M_2	39.5µ/1µ	55.3µ/1µ	42.9µ/1µ
M_3	12.2µ/1µ	17µ/1µ	9.6µ/1µ
M_4	12.2µ/1µ	17µ/1µ	4.9µ/1µ
M_5	16.2µ/1µ	22.7µ/1µ	30µ/1µ

The GA evolution lasted for 30 generations. The evolution of the fitness value vs. generations is plotted in figure 8. Design algorithm convergence is illustrated by the decrease in the average distance between individuals, plotted vs. generations in figure 9.

Table 4. FC-OTA performance parameters in the second design run.

	Equation-based design	Over-sizing	GA-optimized design
A_0	65 dB	62.9 dB	73.3 dB
f_p / BW	5.1 kHz	7.2 kHz	3.2 kHz
GBW	8.9 MHz	10 MHz	13.5 MHz
SR	26.6 V/µs	39.4 V/µs	40 V/µs
PWR	926 µW	1.23 mW	930.6 µW
Area	278.4 μ^2	388.6 μ^2	280.2 μ^2

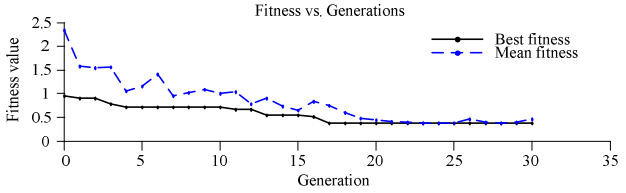

Figure 8. Evolution of the fitness value vs. generations for the first design run.

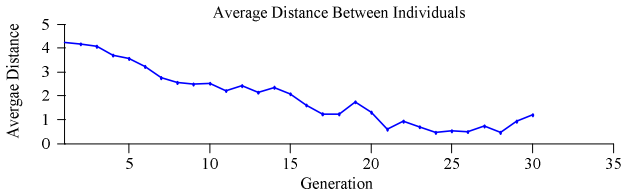

Figure 9. Evolution of the average distance between individuals vs. generations for the first design run.

CONCLUSIONS

This paper presents a two stage design methodology to automate the design of operational transconductance amplifiers. The first design stage employs an equation-based scheme for sizing the OTA. The second designs stage employs GA to optimize the OTA parameters. A FC-OTA was subject to design with the proposed methodology. Simulation results prove that the proposed methodology is indeed valid. The designed FC-OTA performs better in terms of chip area and power consumption, in comparison to the design results obtained with over-design, for the same design specifications.

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