FULLY DIFFERENTIAL CURRENT MODE LOW-PASS BIQUAD WITH INDEPENDENT PARAMETER TUNING

Robert GROZA , Claudia FARAGO
Technical University of Cluj-Napoca, Faculty of Electronics, Cluj-Napoca, Romania
G. Bariţiu street, no. 26-28, Tel. +40-264-401227, Fax +40-264-591340, Robert.Groza@bel.utcluj.ro

Abstract: The paper presents a fully differential log-domain low-pass second order filter. The topology was derived, using a LIN-ELIN transformation, from a standard state-variable biquad. The filter allow for orthogonal parameter tuning. Its low-frequency gain (H_0), natural pulsation (ω_0) and quality factor (Q) can be tuned continuously by varying only DC bias currents. The filter was implemented in a generic BiCMOS 0.18µm process and the simulation results demonstrate the validity of the design.

Keywords: *ELIN, current mode circuits, parameter tuning.*

I. INTRODUCTION

Nowadays there are growing strong demands for low power consumption and low supply voltage systems. This is especially true for battery operated medical devices, wireless sensors and also for compatibility with today's low supply voltages used for digital applications. Multi-standard integrated radio receivers for mobile communication devices, beside the low-voltage low-power requirements, need programmable and reconfigurable continuous-time analog filters, with bandwidths tunable over a wide range, as well as the possibility of changing the type of the filter transfer function. This trend has forced designers to look for alternative approaches, more amenable to low-voltage and low power integrated circuits.

One solution is current mode operation which offers larger dynamic range than the voltage mode operation, provided that the inherent nonlinear characteristic of the active device is compensated such that the operation remains linear outside the small signal region.

An effective way to accomplish this is to combine blocks with known nonlinear transfer functions. These structures are usually called Externally Linear Internally Nonlinear (ELIN). A well-known example of this approach is the log-domain filter [1], where one uses the logarithmic and exponential functions so that the resulting circuits present linear input-output characteristics, even if the internal building blocks are nonlinear. One of the main features of these types of circuit is how easily the parameters (H_0, ω_0, Q) can be tuned. The tuning of parameters is achieved by varying the bias currents from inside the log-domain schematic.

Another advantage of the current mode operation is the ease with which it can implement mathematical operations such as adding and subtracting signals, both for topology (a circuit node) and for circuit implementation (a current switch). This is a useful feature for reconfigurable filters, able to realize multiple frequency characteristics.

Section II presents briefly the prototype from which the log-domain biquad was derived and the dependence between the filter parameters and the building block parameters. Section III presents the log-domain building blocks used to implement the filter; the log-domain biquad is described in Section IV. The tunability of the proposed biquad is demonstrated by simulations presented in Section V; conclusions are drawn in the last Section.

II. SECOND ORDER LOW-PASS PROTOTYPE

The standard state-variable topology for a second order low-pass filter is shown in Figure 1 with the transfer function described in (1).

$$H(s) = H_0 \cdot \frac{\frac{1}{\tau_1 \cdot \tau_2}}{s^2 + \frac{k}{\tau_2} \cdot s + \frac{1}{\tau_1 \cdot \tau_2}} \qquad (1)$$

After comparing (1) with the general form of a low-pass second order filter:

$$H(s) = H_0 \cdot \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} \cdot s + \omega_0^2} \qquad (2)$$

results the dependency between the filter parameters and the building block parameters:

$$\omega_0 = \sqrt{\frac{1}{\tau_1 \cdot \tau_2}}; \qquad Q = \frac{1}{k} \cdot \sqrt{\frac{\tau_2}{\tau_1}} \qquad (3)$$

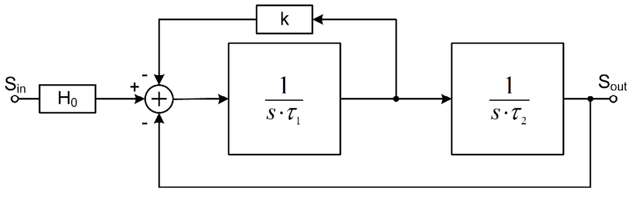

Figure 1. General block diagram of a low-pass biquad

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If $\tau_1 = \tau_2 = \tau$, one can see that the quality factor (Q) can be adjusted using the **k** parameter and the natural pulsation (ω_0) can be adjusted independently from the other parameters by tuning the factor τ.

III. LOG-DOMAIN BUILDING BLOCKS

A. Basic log-domain building blocks

The basic building blocks (logarithmical cell and two exponential cells) used for our application are the ones based on the voltage controlled current mirrors [1]. Using these cells the differential logarithmic and exponential cells were implemented. The differential logarithmic cell and its symbol are presented in Figure 2 while Figure 3 shows the differential exponential cell and its symbol. We need two types of exponential cells because the usual implementation of the log-domain integrator requires exponential current source (Q_1-Q_4 and Q_9-Q_{12}) and exponential current sink (Q_5-Q_8 and Q_{13}-Q_{16}).

Equation (4) presents the expression of the output voltages of the circuit shown in Figure 2. One can see the non-linear (logarithmic) dependence of the output voltages (v+ and v-) on the input currents (i+ and i-), but also the fact that it also depends on the thermal voltage, V_T, and the bias current I_L.

$$\begin{cases} v^+ = 2 \cdot V_T \cdot \ln \dfrac{i^+}{I_L} \\ v^- = 2 \cdot V_T \cdot \ln \dfrac{i^-}{I_L} \end{cases} \tag{4}$$

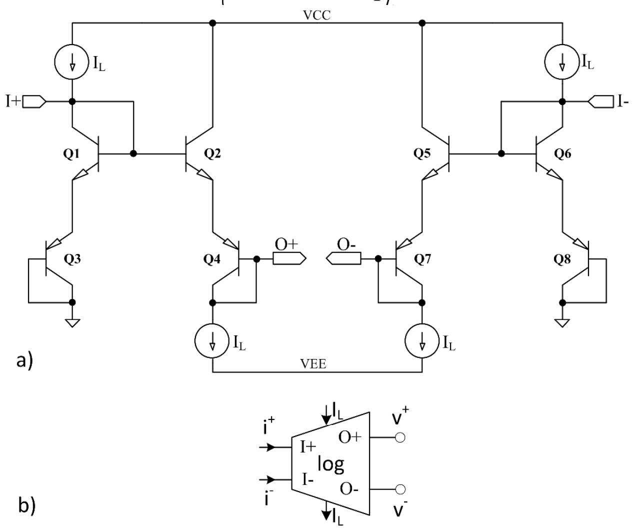

Figure 2. Differential logarithmic cell: a) schematic view, b) symbol

The expressions of the output currents of the circuit shown in Figure 3 is given in (5); note that, beside the exponential dependency on the differential input voltage, it also depends on the bias current, I_E, and on the thermal voltage, V_T.

$$\begin{cases} i^+ = I_E \cdot \exp\left(\dfrac{v_1^+ - v_1^-}{2 \cdot V_T}\right) \\ i^- = I_E \cdot \exp\left(\dfrac{v_2^+ - v_2^-}{2 \cdot V_T}\right) \end{cases} \tag{5}$$

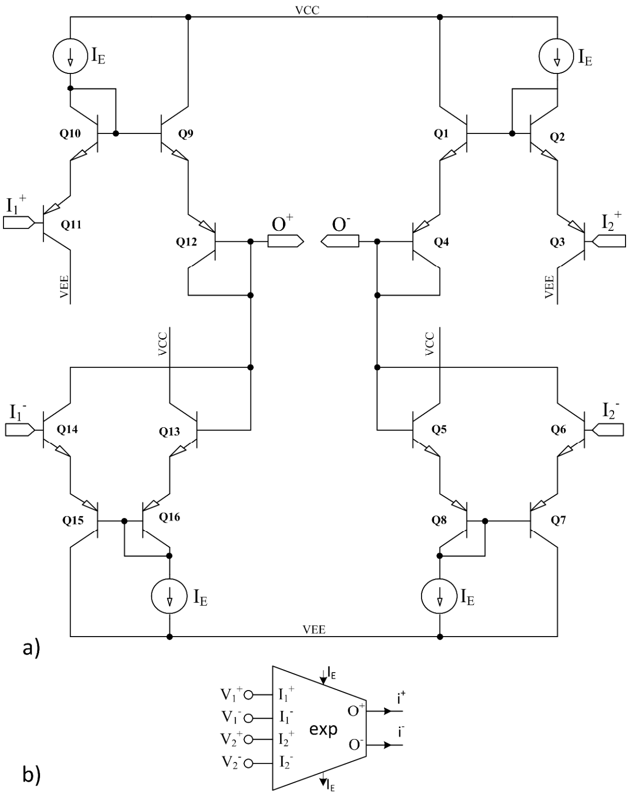

Figure 3. Differential exponential cell: a) schematic view, b) symbol

B. Fully differential log-domain voltage amplifier

In Figure 4 is presented a fully differential log-domain voltage amplifier. The gain of the amplifier is the ratio between the bias currents of the log-domain building blocks:

$$k = \frac{I_E}{I_L} \tag{6}$$

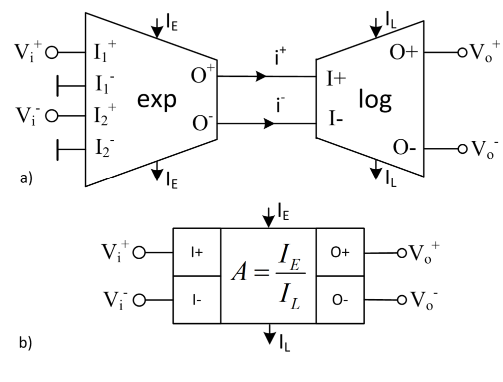

Figure 4. Fully differential log-domain voltage amplifier: a) schematic view, b) proposed symbol

C. Fully differential log-domain lossless integrator

In Figure 5 one can see the block level implementation of a fully differential lossless log-domain implementation where the input and output signal is voltage. Its transfer function can be written:

$$\frac{v_o^+ - v_o^-}{v_i^+ - v_i^-} = \frac{1}{s\cdot\tau} = \frac{1}{s\cdot\frac{2\cdot V_T\cdot C}{I}} \qquad (7)$$

From (7) one can see that the natural pulsation can be tuned using the bias current, I, of the exponential cells.

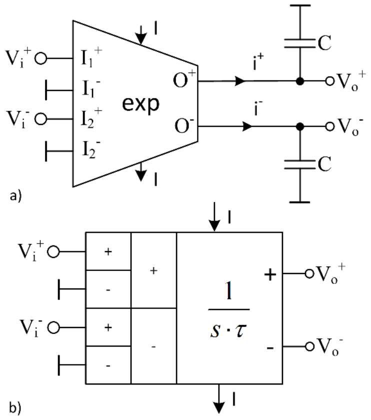

Figure 5. Fully differential log-domain lossless integrator: a) schematic view, b) proposed symbol

IV. TUNABLE LOG_DOMAIN FULLY DIFFERENTIAL LOW-PASS BIQUAD

Figure 6 shows the topology and circuit implementation of a fully differential low-pass biquad implemented with the log-domain building blocks described in Section III. It was derived from the general structure shown in Figure 1 by using the LIN-ELIN transformation method developed in [2].

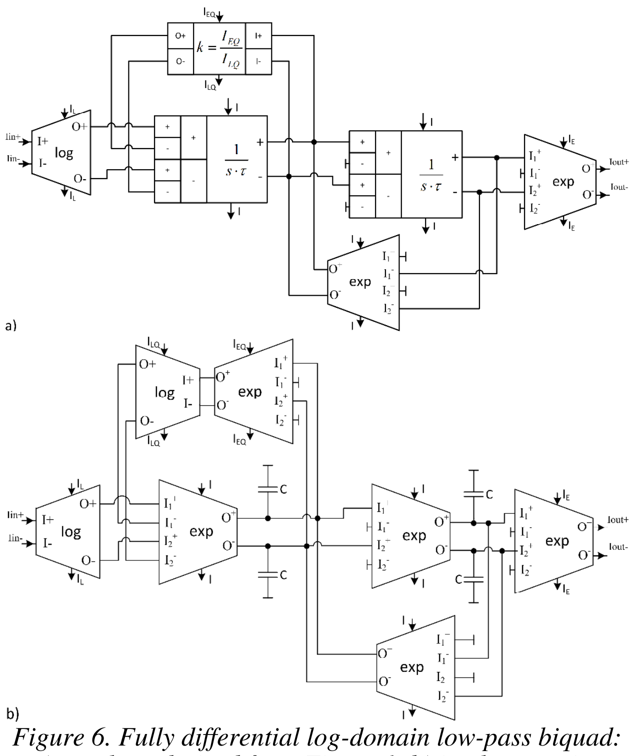

Figure 6. Fully differential log-domain low-pass biquad: a) topology derived from Figure 1, b) implementation with log-domain blocks

It implements the transfer function described by (2), where:

$$\omega_0 = \frac{1}{2\cdot V_T}\cdot\frac{I}{C}; Q = \frac{I_{LQ}}{I_{EQ}}; H_0 = \frac{I_E}{I_L} \qquad (8)$$

V. SIMULATION RESULTS

In order to demonstrate the functionality of the proposed fully differential log domain low-pass filter topology, the structure from Figure 6 was implemented using a generic 0.18µm BiCMOS process. The following requirements were targeted: Butterworth transfer function with 10MHz corner frequency and unitary gain. It was considered the capacitance values (C) equal to 1pF and the thermal voltage (V_T) equal to 25.8mV. These yields (equation 8) I=3.25 µA, I_{LQ}=7 µA, I_{EQ}=10uA and I_E=I_L=10 µA. Figure 7 shows the frequency characteristics and Figure 8 the group delay.

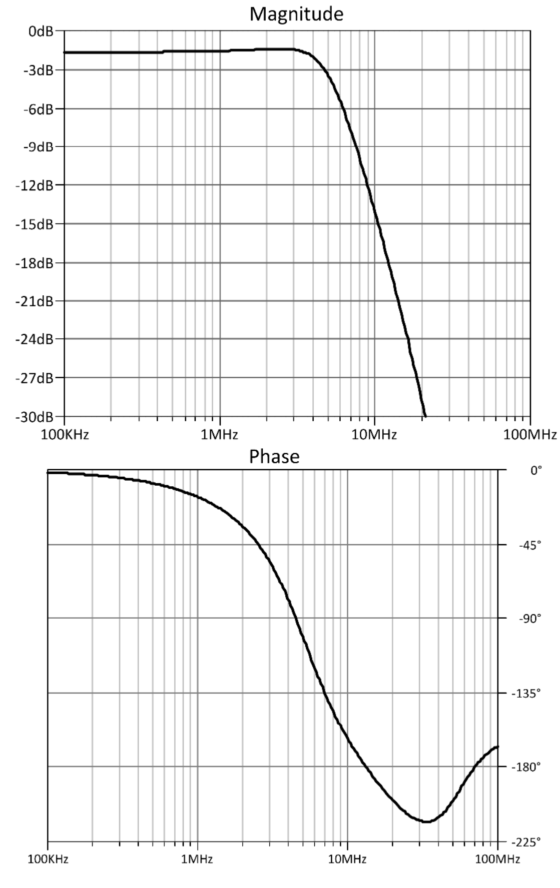

Figure 7. Magnitude and phase response of the biquad for I=3.25µA, C=1pF, I_E=I_L=I_{EQ}=10µA, I_{LQ}=0.7I_{EQ}

Starting from this filter, the tuning capabilities of the proposed filter was demonstrated:

- In Figure 9 the -3dB corner frequency was varied between 2.5MHz and 78MHz by changing the bias current I, between 1µA and 50µA. One can see that the low frequency gain remains relatively constant and there is no gain peaking so the quality factor has not changed. The small gain variation is due to transistor non-idealities [3].
- Figure 10 shows that the low-frequency gains can be varied using the input logarithmic cell and the output

exponential cell bias current. The gain takes values within a 36dB range when the bias current I_E is modified between 2μA and 200μA. Bias current I_L is kept at 20μA.

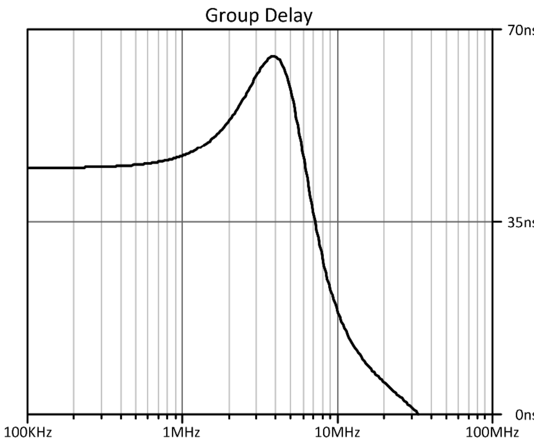

Figure 8. Group delay response for I=3.25uA, C=1pF, I_E=I_L=I_{EQ}=10uA, I_{LQ}=0.7I_{EQ}

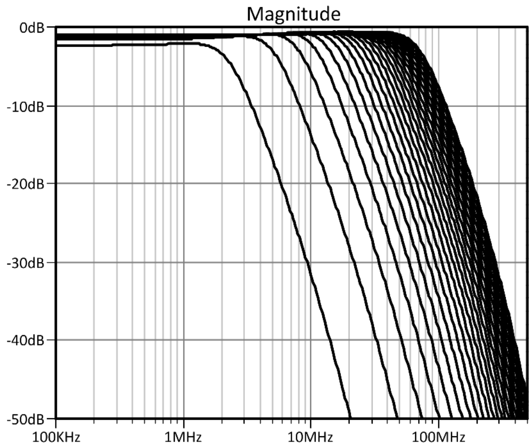

*Figure 9. Orthogonal corner frequency tuning for C=1pF, I_E=I_L=I_{EQ}=10μA, I_{LQ}=0.7*$I_{EQ,}$ I= [1μA…50μA]*

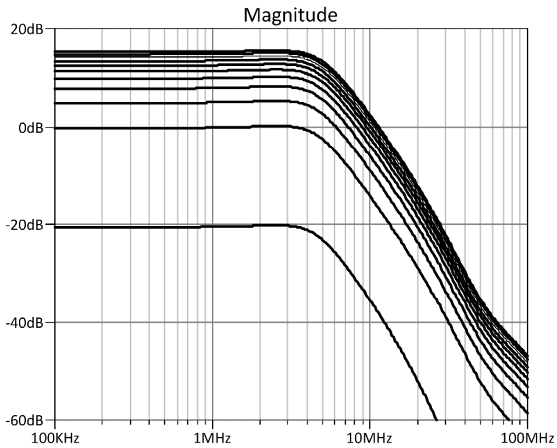

*Figure 10. Orthogonal gain tuning for C=1pF, I=3.25μA, I_L=20μA, I_{EQ}=10uA, I_{LQ}=0.7*I_{EQ} and I_E= [2μA…200μA]*

- Figure 11 shows that the gain peaking (hence the quality factor) can be varied over a wide range by varying the biasing current I_{EQ} between 10μA and 100μA. The natural pulsation remains constant - the frequency characteristics have a common point at the critical phase value of -90°. The low-frequency gain has a slight variation like in the case of the corner frequency tuning. This is also due to transistor non-idealities.

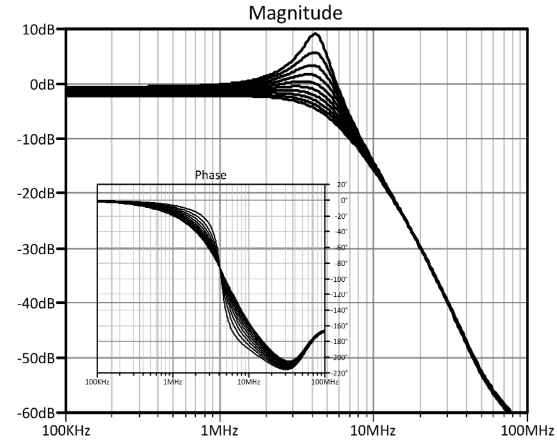

Figure 11. Orthogonal Q tuning for C=1pF, I=3.25μA, I_L=I_E=10μA, I_{LQ}=50μA and I_{EQ}= [10μA…100μA]

VI. CONCLUSIONS

In this paper, a novel topology for a fully differential log-domain second order low-pass filter is presented. The structure was implemented using differential input – differential output logarithmic and exponential cells. The biquad permits an orthogonal tuning of its main parameters, low-frequency gain, natural pulsation and quality factor. This can be done continuously by simply changing DC bias currents. To validate the analytical analysis the proposed filter was implemented in a generic BiCMOS 0.18μm process. The simulations results shown here demonstrate the predicted tunability: the cut-off frequency can be varied by modifying the DC bias current of the lossless log-domain integrator, while the gain and quality factor remain unchanged; the low-frequency gain can be modified by varying the DC bias current of the output exponential cell; the quality factor can be set independently by the bias current of the exponential cell that implements the voltage-current feedback path mentioned above.

ACKNOWLEDGMENT

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