STABILITY OF SEVERAL TYPES OF HIGH FREQUENCY RING OSCILLATORS DEPENDING ON CIRCUIT CONFIGURATIONS AND PARAMETERS

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Abstract: This paper proposes studying the performance of the PLL loop depending on the configurations of the voltage-controlled oscillators used and on the types of ring oscillators. The oscillation frequency depends on the oscillator structure, the size of the CMOS transistors, the supply voltage, the control voltage, and the load capacity. In several configurations, ring oscillators and VCOs were used, with several gate types and several sizes of CMOS transistors. We also added an inverter to the output of the studied oscillators and demonstrated the increase of the robustness of a PLL loop in a larger frequency range. By measurements, we have shown that the oscillation frequency is no longer influenced by the variation of the load capacity. We measured the phase-locked time for the PLL loops and demonstrated that by using the inverter at the oscillator's output to the load, we obtain the shortest time. The implementation and simulation of the circuits used in this paper were performed in the LT Spice XVII simulator. The simulations were performed transiently, with the duration set in such a way that the results are interpreted properly.

Keywords: *ring oscillators, oscillation frequency, PLL loop, phase-locked time.*

I. INTRODUCTION

Oscillators are widely used in many electronic devices, from the simplest clock generators to digital instruments and complex computers. Common examples of oscillator signals include signals from radio and television stations, clock signals that adjust computers and quartz clocks, and the sounds produced by video games [1].

Voltage-controlled oscillators (VCOs) are commonly found in wireless and other communications systems that need to adjust a frequency band. These oscillators are available from a wide range of manufacturers in various package styles and performance levels. The development of modern VCOs began almost 100 years ago. VCO technology improvement has continued over time, obtaining smaller and smaller oscillation sources, with improved low phase noise and linearity of adjustment [2], [3].

The input voltage controls the frequency of the oscillator output signal. This oscillator can produce the output signal frequency over a wide range as a function of a given input voltage. A conventional construction for a VCO includes two parts:

- the first, which converts the input voltage into a control current;
- and second, which converts the control current into an output signal having a predetermined frequency based on the size of the control current;

This paper has studied high-frequency digital oscillators' performance for use in the remote transmission of frequency encoded information. The ring oscillator implemented in several structures was studied, and also, the current starved ring VCO and combined VCO. The ring oscillator is a circuit that switches itself from one state to another, depending on a time constant; namely, it is an astable circuit. The main components of which it is composed are the transistors because no passive components are used. CMOS transistors are used to easily integrate and occupy small areas on the chip, with low costs. The ring oscillator is built of an odd number of inverters connected in a ring [4], [5]. An odd number of gates is used because an inverter calculates the negation of its input, proving that having an odd number of gates, the whole chain's output is the negation of the first input, thus maintaining the periodicity of the generated signal. The oscillator's output is connected to its input, and thus, to produce the oscillation, the minimum number of gates that make up an oscillator is 3. The oscillation frequency obtained at the oscillators' output in the ring is inversely proportional to the number of use gates [6].

Ring oscillators consist of both inverters and NAND gates or NOR gates that have interconnected inputs. The oscillator's main diagrams implemented with these types of gates are illustrated in figures 1, 2, and 3, respectively.

A VCO is an electronic oscillator whose oscillation frequency is controlled by an input voltage; this applied voltage determines the instantaneous oscillation frequency.

A current starved ring VCO is a circuit that controls each element's delay by controlling the amount of current available for charging and discharging the load capacity of the inverter. The Figure 4 shows the schematic diagram of the current starved ring VCO circuit.

The combined VCO was designed because most oscillators cannot improve the stability of the oscillation frequency at supply voltage fluctuations [7]. Figure 5 shows the schematic diagram of the combined VCO.

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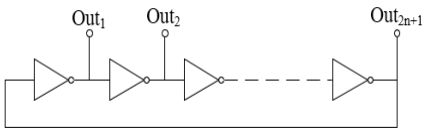

Figure 1. Ring oscillator implemented with inverters

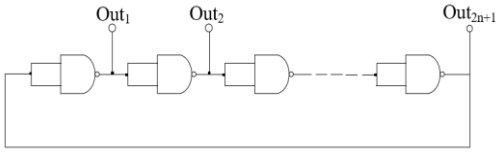

Figure 2. Ring oscillator implemented with NAND gates

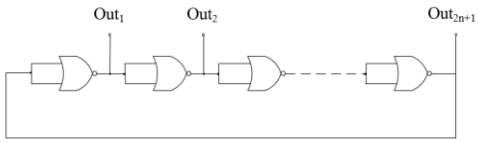

Figure 3. Ring oscillator implemented with NOR gates

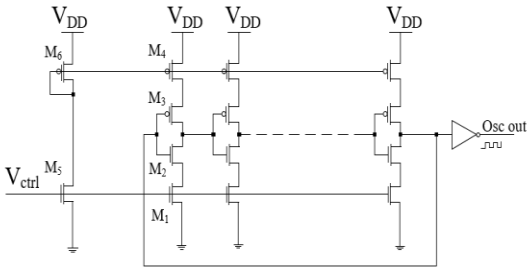

Figure 4. The current starved ring VCO

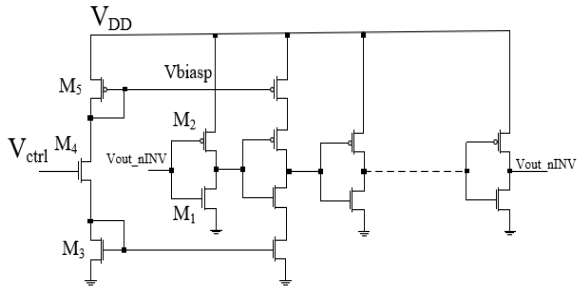

Figure 5. The combined VCO

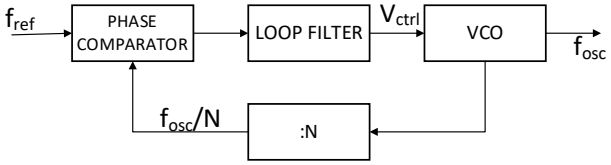

Figura 6. The Phase-Locked Loop

Several solutions drive the realization of VCO with central frequencies in the range of a few GHz. In wireless, good feature propagation and high bandwidth are available in the 1-2 GHz range, have allowed the stabilization and operation of digital mobile systems worldwide. The new 2.5-5 GHz wireless data applications have aroused interest in large markets. These applications are automation, wireless connections, etc.

In telecommunications, it is necessary to generate an exact and stable tactile signal and a carrier frequency for synchronous sequential digital circuits (microprocessors, memories, network interfaces, etc.). This is done using phase-synchronized frequency synthesizers known in the literature as Phase-Locked Loop (PLL). These synthesizers use in CMOS technology, with VCOs optimized for short synchronization time (phase-locked time).

The PLL loop's role is to ensure increased stability of the output oscillation frequency, using an input reference frequency [8]. The reference frequency (f_{ref}) is very accurate and comes from a quartz oscillator, whose frequency is suitably divided. The desired oscillation frequency (f_{osc}) is adjusted by controlling a VCO in the PLL. Figure 6 shows the block diagram of a PLL loop [9]. The output signal has an oscillation frequency that is an integer multiple of the reference frequency. To maintain a constant and accurate output frequency due to the feedback loop, the phase comparator causes the VCO to oscillate faster or slower, ensuring a Vctrl control voltage at the VCO input. The synchronization speed or phase-locked speed of the PLL loop on the desired frequency is quantified in the measurement of the synchronization time (t_s).

This paper aims to demonstrate the advantage of using the inverter at the VCO output. The inverter ensures better linearity of the oscillation frequency depending on the control voltage, and the independence from the load capacity, thus ensuring the increase of the robustness of the PLL loop.

This paper is structured in five sections. The first chapter describes the ring oscillators, the VCOs, and the PLLs. The second describes the configurations used and parameters, that change the signal frequency at the oscillator's output. Section three illustrates the results of the measurements, and in the fourth chapter, are shows interpretations of results. In the last one, conclusions are highlighted.

II. IMPLEMENTATION METHODS

The role of this paper is to monitor the oscillation frequency, which is influenced by different parameters of the circuit, and to measure the phase-locked time (synchronization) of the PLL loops implemented with VCOs. Following the implementation of the circuits in the simulator, we will identify the oscillators' performance in the transmission of signals at a distance and the linearity range of the variation of the oscillation frequency..

1. Ring oscillator

The ring oscillator was implemented using inverters, NAND gates, and NOR gates. The number of gates was chosen as 3, 5, 7, and 9 for each implementation.

Each gate contains both nMOS and pMOS transistors by 90 nm, which took three width/length (W/L) ratios in turn, these dimensions being: 2/1 and 1/1, 8/1 and 4/1,

respectively 8/4 and 4/4. For these ring oscillators, the variation of the oscillation frequency was analyzed depending on the supply voltage, load capacity, and transistors' size. The frequency of the oscillator output signal was calculated using the following formula [3],[10]:

$$f = \frac{1}{2 \cdot n \cdot (t_p + t_r)} \qquad (1)$$

where t_p is the propagation time through a gate, t_r is the rising time of the signal front, n the number of gates in the circuit, and f represents the oscillation frequency.

Since these oscillators must be connected either in load or to another circuit, the following two circuits' implementation was analyzed: the ring oscillator with 5 inverters with a load capacity to the output, respectively the ring oscillator with 5 inverters with an additional inverter at the output toward a load capacity. These circuits are illustrated in Figure 7 and Figure 8, respectively.

1. Voltage Controled Oscillator

The purpose of testing VCOs is to analyze the influence of the control voltage on the oscillation frequency at a constant supply voltage of 5V.

1.1. Current starved ring VCO

The current starved ring VCO was made in two configurations, both being implemented with 3, 5, and 7 inverters, and the size of the transistors in the circuit was chosen as 8/1 and 4/1, respectively. The application of the control voltage gives the difference between the two forms. In the first form, the control voltage is applied to one of the transistors that form the current mirror. In the second form, the control voltage is applied to a transistor located between the two transistors that make up the current mirror (intermediate transistor). This current mirror has the role of controlling the current through each stage. Figures 9 and 10 show the oscillators with 5 inverters on which we performed the measurements in the two configurations.

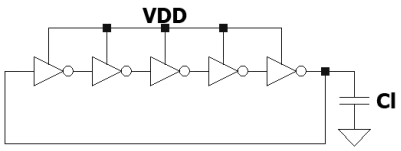

Figure 7. The ring oscillator with 5 inverters and a load capacity

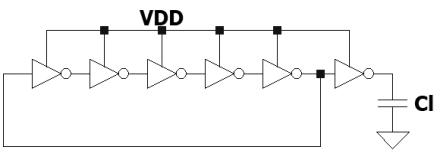

Figure 8. Ring oscillator with 5 inverters, a load capacity, and inverting gate at the output toward the load

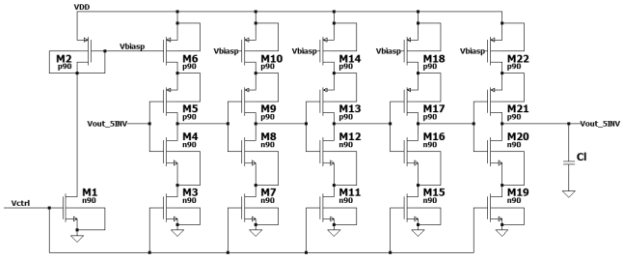

Figure 9. The VCO with 5 inverters

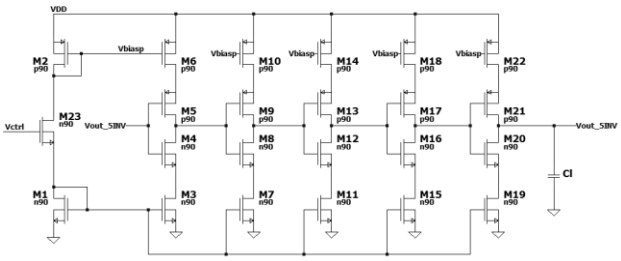

Figura 10. The VCO with 5 inverters and intermediate transistor

For the stability of the oscillation frequency from the output of the oscillator, regardless of the value of the load capacity, we implemented an inverter at the output of the oscillator toward the load.

1.2. The combined VCO

The combined VCO was implemented with 3, 5, and 7 reversing gates. The size of the transistors in the circuit was chosen as 8/1 and 4/1, respectively. Figure 11 shows the combined VCO, without inverter at the load exit, and in Figure 12, the combined VCO, with inverter toward the load exit.

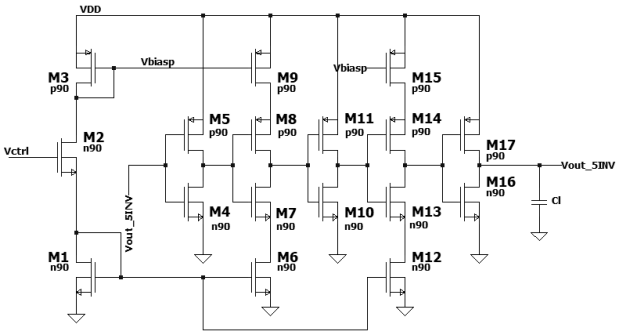

Figure 11. The combined VCO

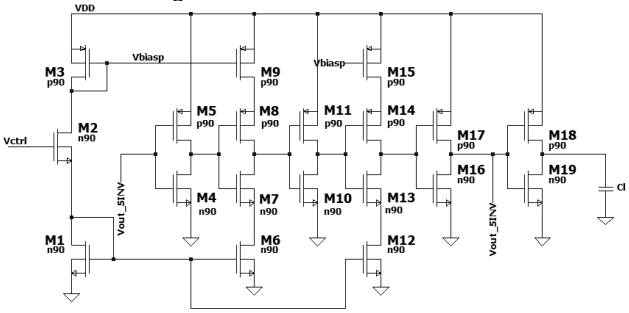

Figure 12. The combined VCO with inverter toward the load capacity

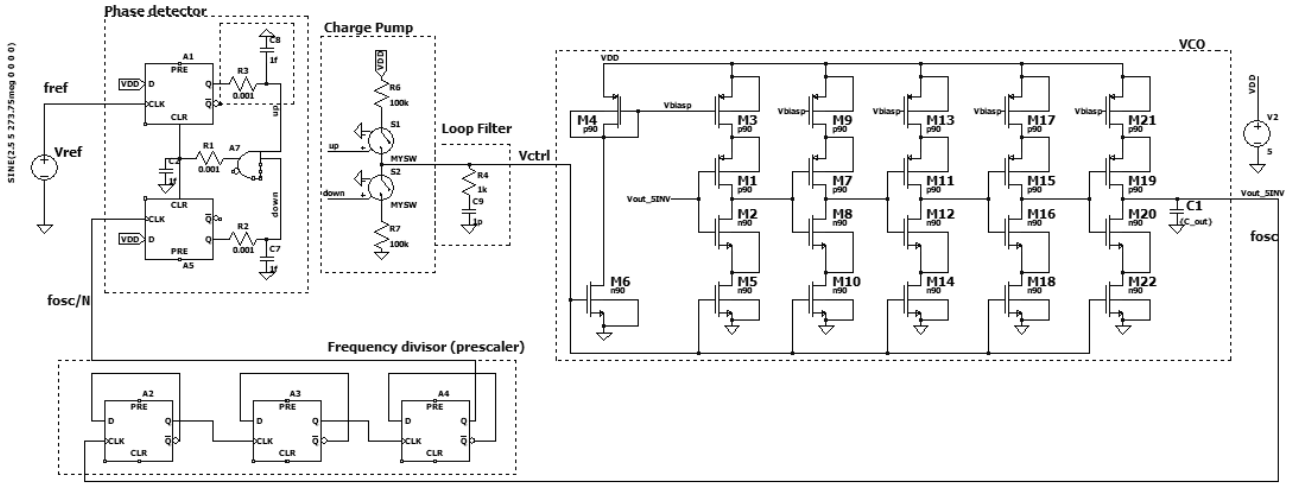

Figura 13. The Phase-Locked Loop

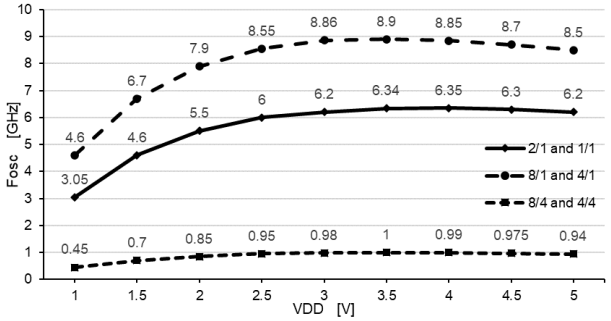

Figure 14. Variation of the oscillation frequency for the ring oscillator with 5 inverters depending on VDD

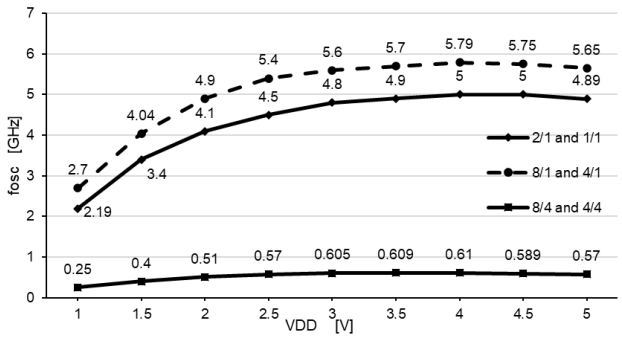

Figure 15. Variation of the oscillation frequency for the ring oscillator with 5 NAND gates depending on VDD

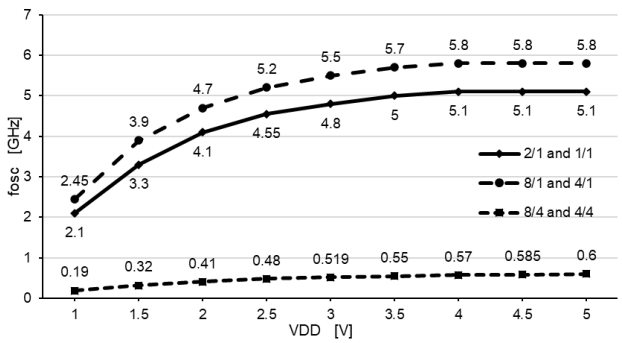

Figure 16. Variation of the oscillation frequency for the ring oscillator with 5 NOR gates depending on VDD

2. Phase-Locked Loop

The loop's role is to ensure the desire oscillation frequency at small variations of the input signal frequency through a feedback mechanism without the loop coming out of the synchronization. An important parameter considered and measured in this paper is the phase-locked time (synchronization time) of the loop on the desired frequency when the load capacity takes values between 10 and 200 fF, with a step of 10 fF.

The VCOs taken into account in the measurement operations are the ones in a simple configuration, with an intermediate transistor in the current mirror where Vctrl is applied, combined, and all these, with an inverter inserted at the output toward the load capacity. The PLL implemented with VCO with 5 inverters is represented in Figure 13.

III. RESULTS

1. Ring oscillator

Following the simulations performed on the ring oscillators, in those three configurations of dimensions (2/1 and 1/1, 8/1 and 4/1, 8/4 and 4/4), at the variation of the supply voltage (VDD), between 1 V and 5 V, with a step of 0.5 V, an increase of the oscillation frequency was observed with the increase of the voltage of power supply (Figure 14).

For the ring oscillators with 3, 7, and 9 inverters, respectively, the oscillation frequency dependence to the VDD has the same allure. For the 3 inverters ring oscillators, the obtained oscillation frequencies are higher than those illustrated in Figure 14, and for 7 and 9 inverters, respectively, the obtained oscillation frequencies are lower.

The results obtained by replacing the inverters with NOR gates and then with NAND gates are illustrated in Figures 15 and 16.

It is observed that the use of the NAND or NOR gates, respectively, decreases the frequency range of the output signal, the variation curve of the oscillation frequency keeping the same allure for all types of gates.

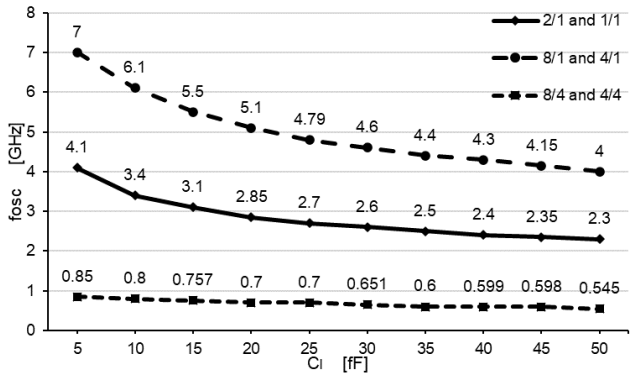

Figure 17. Variation of the oscillation frequency according to the load capacity (Cl) for the ring oscillator with 5 inverters

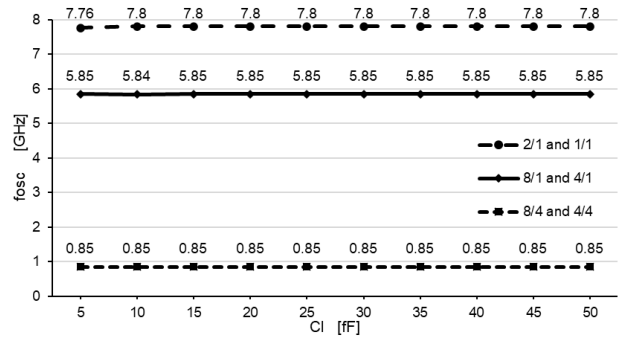

Figure 18. Variation of the oscillation frequency according to the load capacity (Cl) for the ring oscillator with 5 inverters and reversing gate toward the load capacity

The variation of the oscillation frequency depending on the load capacity is illustrated in Figure 17 and is built for the ring oscillator with 5 inverters. The results for the other types of gates are similar, being only at different oscillation frequencies.

For small load capacities, the oscillation frequency does not have a linear variation. Linearity is more evident for capacities above 25 fF.

The location of an inverting gate at the output of the oscillator ensures a constant value oscillation frequency, as illustrated in Figure 18.

2. Voltage controlled oscillator

We measured the oscillation frequencies from the simple VCO output and combined VCO, in the current mirror configurations, with and without an intermediate transistor. We considered the transistors' three size variants (2/1 and 1/1; 8/1 and 4/1; 8/4 and 4/4). The results of the measurements are shown in Figures 19, 20, and 21.

By introducing the inverter at the oscillators' output toward the load capacity, we obtained an increase in the linearity of the variation of the oscillation frequency. Figures 22, 23, and 24, respectively, show the measurement results for the three VCO variants.

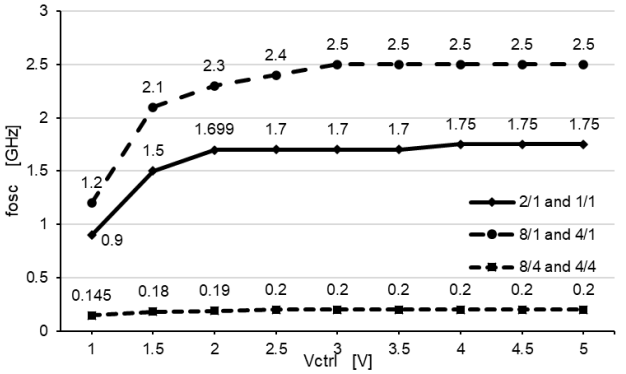

Figure 19. Variation of the oscillation frequency according to the control voltage (Vctrl) for simple VCO

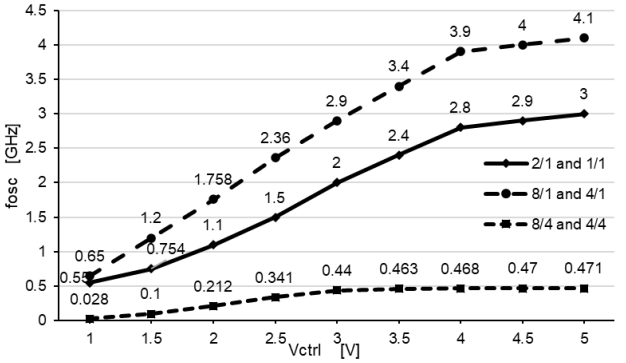

Figure 20. Variation of the oscillation frequency according to the control voltage (Vctrl) for VCO with an intermediate transistor in the current mirror

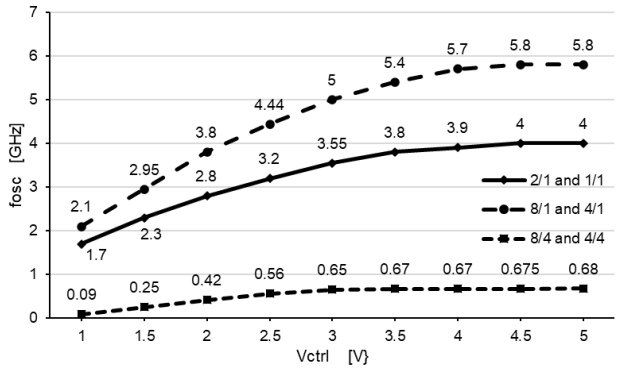

Figure 21. Variation of the oscillation frequency according to the control voltage (Vctrl) for combined VCO

3. *Phase-Locked Loop*

We built the PLL with VCOs composed of 5 inverters in the following configurations: simple VCO, VCO with an intermediate transistor in the current mirror, and combined VCO. The configurations were made with and without inverter at the VCO output toward the load capacity, resulting in six PLL schemes. The VDD supply voltage is 5 V, and the load capacity varies from 10 fF to 200 fF, with a step of 10 fF. Thus, we followed the variation of the phase-locked time according to the load capacity. Figures 25, 26, 27, 28, 29, and 30 show the results of the phase-locked time measurements for VCOs with gates whose transistors are the 8/1 and 4/1 ratios.

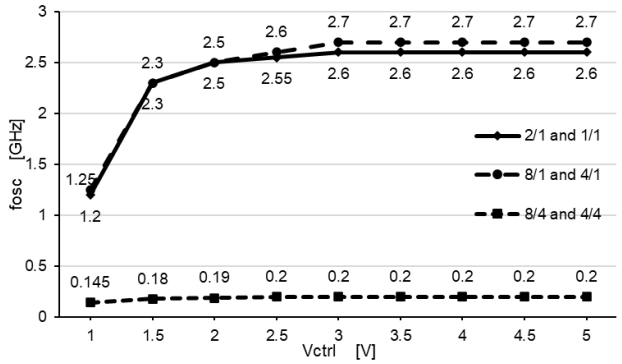

Figure 22. Variation of the oscillation frequency according to the control voltage (Vctrl) for simple VCO with an inverter to the output toward the load capacity

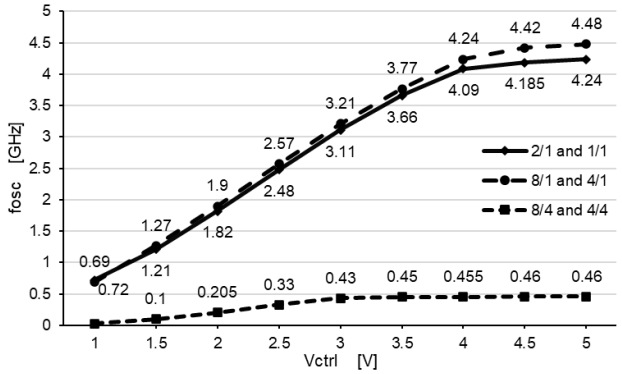

Figure 23. Variation of the oscillation frequency according to the control voltage (Vctrl) for simple VCO with an intermediate transistor in the current mirror, with an inverter to the output toward the load capacity

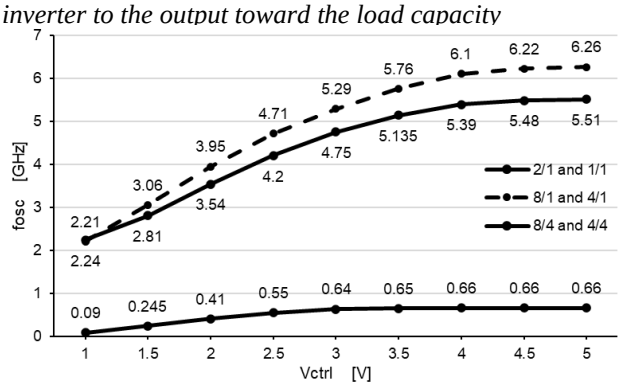

Figure 24. Variation of the oscillation frequency according to the control voltage (Vctrl) for combined VCO with an inverter to the output toward the load capacity

IV. INTERPRETATIONS OF RESULTS

All the values we obtained from the measurements, specified on the graphs in the figures

For the first measurements, the ring oscillators were used in three simple configurations built with reversing gates, NAND gates, and NOR gates. The transistors have, in turn, dimensions 2:1 and 1:1, 8:1 and 4:1 and 8:4 and 4:4, respectively.

The first measurements presented in the paper illustrate the variation of the oscillation frequency depending on VDD and on the type of gates. In Figures 14, 15, and 16, we can see that the highest oscillation frequency is obtained using inverters.

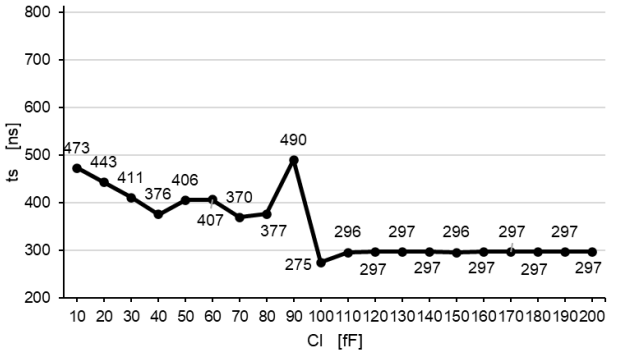

Figure 25. Variation of the phase-locked time according to the load capacity (Cl) for PLL with simple VCO

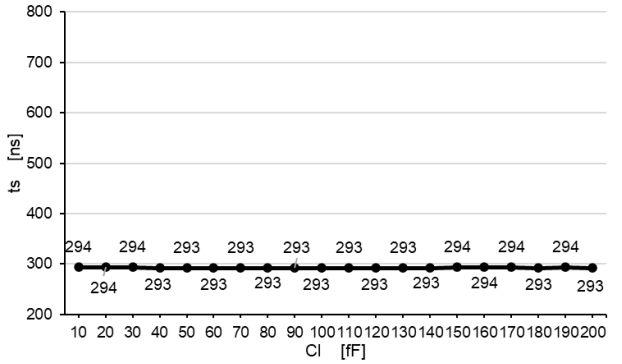

Figure 26. Variation of the phase-locked time according to the load capacity (Cl) for PLL with simple VCO, with an inverter to the output toward the load capacity

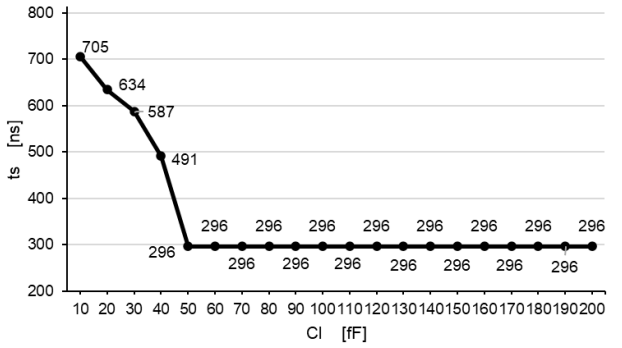

Figure 27. Variation of the phase-locked time according to the load capacity (Cl) for PLL with VCO with an intermediate transistor in the current mirror

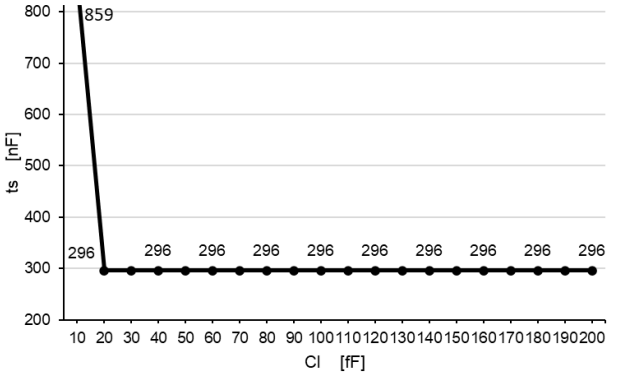

Figure 28. Variation of the phase-locked time according to the load capacity (Cl) for PLL with VCO with an intermediate transistor in the current mirror, and with an inverter to the output toward the load capacity

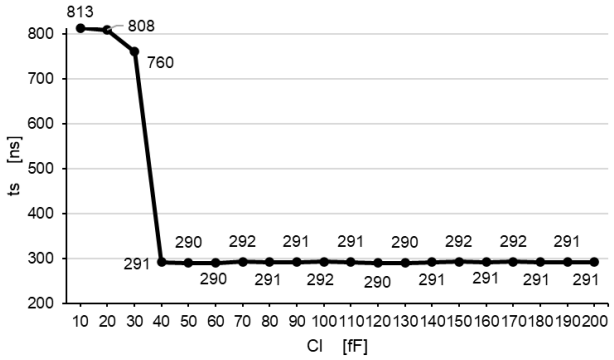

Figure 29. Variation of the phase-locked time according to the load capacity (Cl) for PLL with combined VCO

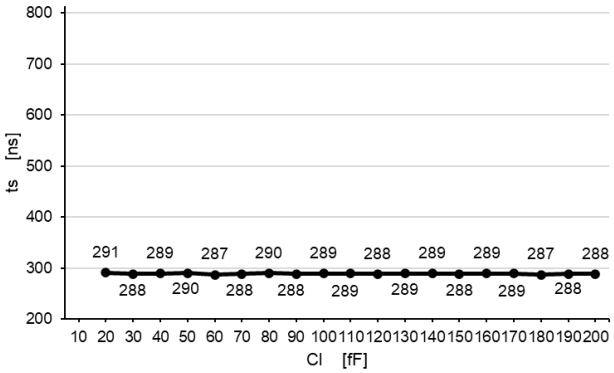

Figure 30. Variation of the phase-locked time according to the load capacity (Cl) for PLL with combined VCO, with an inverter to the output toward the load capacity

With NAND and NOR gates, lower frequencies are obtained, approximately equal to each other. Measured values, expressed in GHz, were illustrated on the figures' graphic. VDD varies between 1V and 5V, with a pitch of 0.5V. We obtained the highest oscillation frequencies for the transistors with dimensions of 8: 1 and 4: 1. For dimensions 2:1 and 1:1, the frequencies decrease, and for dimensions 8: 4 and 4: 4, the oscillation frequencies are lowest (below 1 GHz). It is also observed that the oscillation frequency has approximate linearity only in the 4-5 GHz range.

Another aspect we followed was the dependence of the oscillation frequency on the load capacity connected to the oscillator's output in the ring. The measurements were performed on a ring oscillator in a simple configuration with 5 inverters in three cases of transistors size. With the increase of the load capacity, in figure 17, a decrease of the oscillation frequency is observed.

We added an inverter toward the load capacity at the ring oscillator's output and repeated the measurements. The frequency oscillation measured values are shown in figure 18. From the measured values, we conclude that by adding an inverting gate to the ring oscillator's output towards the load capacity, we obtain a constant oscillation frequency, which does not depend on the value of the load. Furthermore, through measurements, we appreciated the dependence of the oscillation frequency on the Vctrl of a VCO with five inverters in three configurations. The results of the measurements are shown in Figures 19, 20, and 21. The three dimensions of the transistors composing the inverters, specified by the legend of the figures, were also considered.

We repeated the measurements after adding the inverter to the VCO output towards the load capacity and specified the resulting values on the graphs of Figures 22, 23, and 24, respectively.

Can be interpreted the measurement results by comparing Figures 19 with 22, 20 with 23, and 21 with 24. We can observe for simple VCO that it kept the linearity in the range 2-5 GHz. By using the inverter at the output, for the VCO in a simple configuration, with the transistors 2:1 and 1:1, there is an increase of the oscillation frequency, keeping the linearity in the same interval. For the VCO with an intermediate transistor in the current's mirror and the combined one, in addition to the increase of the oscillation frequency, an increase of linearity is observed in the 1-4 GHz range. In all cases, for 8:4 and 4:4 transistors, no significant changes were recorded by using the inverter at the VCO output.

Phase-lock time is an appreciating factor of the PLL loop. Following the measurements, we observed that for the VCO configurations without an inverter toward the load capacity, obtained very long phase-lock times, for load capacities up to 40fF in the case of combined VCO, up to 50 fF for VCO with an intermediate transistor, and up to 100 fF for simple VCO. Using the inverter at the VCO's output toward the load capacity, short phase-lock times we obtained, regardless of the load capacity. The shortest phase-lock time was obtained for the combined VCO configuration of 288 ns (figure 30), regardless of the load capacity value. Slightly higher values of 293 ns were obtained for the simple VCO configuration (figure 26) and 297 ns for the VCO configuration with an intermediate transistor in the current mirror (figure 28).

V. CONCLUSIONS

In this paper, we studied the variation of the oscillation frequency from the oscillators' output in the ring depending on the supply voltage and the load capacity. The studied ring oscillators were presented in three constructive variants, using reversing gates, NAND gates, and NOR gates. The number of used gates was 3, 5, 7, and 9. The results presented in the paper correspond to the number of 5 gates. We also considered three dimensions of transistors, 2:1 and 1:1, 8:1 and 4:1, and 8:4 and 4:4, respectively.

The measurement results showed that the oscillation frequency of these ring oscillators increases with the VDD supply voltage. Using an inverter at the oscillator's output, the oscillation frequency remains constant, i.e., it no longer depends on the supply voltage variation.

With the studied oscillators, we built VCOs that we implemented in a PLL loop. A VCO in three configurations was implemented: simple, with an intermediate transistor in the current's mirror and combined, with and without inverter to the output toward the load capacity. We studied the effect of the control voltage on the oscillation frequency at the output of the loop and the phase-lock time on the desired frequency. The results of the measurements indicated the curve of the oscillation frequency as a function of Vctrl. Using the inverter at the VCO output towards the load capacitor, we noticed an increase in the linearity of the oscillation frequency as a function of Vctrl, especially in the range 2-4 GHz.

Also, the application of the inverter to the VCO output ensures the shortest phase-lock time on the desired frequency, regardless of the load capacity, for all VCO configurations.

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