SIMULINK LIBRARY OF BASIC BUILDING BLOCKS FOR TERNARY LOGIC

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Abstract: A library of basic building blocks implemented in Simulink for ternary logic is presented. The basic blocks are: inverters, minimum, negated-minimum, maximum and negated-maximum. The considered ternary logic is unbalanced ones, with *0*, *1* and *2* logic levels. With basic building blocks we implement the ternary D flip-flap-flop, with binary and ternary clock. The simulation results validate the correct operation for all implemented building blocks.

Keywords: *ternary inverters, minim and maxim ternary circuits, D flip-flap-flop, Simulink block*

I. INTRODUCTION

Multi-valued logic compared to binary one, works with more than two logical levels. The minimum cost or complexity C, in a numerical system, is obtained for R=*e* (2.718), where R represents the radix. Since R must be an integer the minimum cost C is obtained for R=3, rather than for R=2 [1]. From this point of view, the ternary circuits are the most economically ones.

A ternary system has several important advantages over a binary one. These advantages can be summarized as: reductions in the interconnections required to implement logic functions, thereby reducing chip area; more information can be transmitted over a given set of lines; less memory requirement for a given data length. Besides this, serial and some serial-parallel operations can be carried out at higher speed. Its advantages have been confirmed in the application like memories, communications and digital signal processing etc [2].

In literature, many papers deal with ternary circuits. In [3-8] some ternary and multi-valued circuits are designed, in different algebras (Givone, Post), having multiple applications.

Instead, the subject of creating libraries of multi-valued logic circuits is not so present in the literature, mainly because there was no practical realization of multi-valued circuits until 2004. However, a library of basic quaternary logic circuits in a TSMC 0.18μm technology, simulated in Spice is presented in [9]. A research group in the domain of design and implementation of multi-valued logic circuits presents its results, including a library of multi-valued logic circuits in [10].

All the above mentioned realizations are technology dependent and suppose the design and simulation at the transistor level. This can be a disadvantage from the point of view of new circuits and applications development. Some functional building blocks can be more useful in developing new circuits or systems whose operation is simulated using high level models instead of lower level (transistor level) models.

Simulink is a software for modeling, simulating, and analyzing of dynamic systems. In a simple manner the user can develop new models according with its necessities. Models are hierarchical, the user can view the system at a high level, then double-click blocks to go down through the levels to see increasing levels of model detail. This approach provides insight into how a model is organized and how its parts interact. In a full design cycle, the functional models in Simulink are very useful being the support of model-based design of complex circuits.

The aim of the paper is to develop a Simulink library of basic ternary circuits, to assure the support for further design of more complex ternary systems. The library consists in: three ternary inverters, two minimum circuits (with two and three inputs), two negated-minimum circuits, two maximum circuits and two negated-maximum circuits. As an application of these basic ternary gates we implement the ternary D flip-flap-flop, with binary and ternary clock.

This paper deals with ternary logic, with logic levels “0” (corresponding to “0” logic in binary), “1” (an intermediary level) and “2” (corresponding to “1” logic in binary).

The paper is organized as follows. In Section 2 the basic ternary gates are described. For simple ternary inverter and negated-minimum circuit with three inputs the presented information’s are: operating table, schematic, symbol and simulation results. For the rest, only the differences are specified. In Section 3 the ternary

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D flip-flap-flop with binary and ternary clock is implemented. The paper ended with some concluding remarks, presented in Section 5.

II. BASIC TERNARY GATES IN SIMULINK

The most fundamental building blocks in the design of digital system are Inverters, NOR and NAND gates [2]. In ternary logic there are three different inverters: simple ternary inverter (STI), positive ternary inverters (PTI) and negative ternary inverters (NTI). The NAND gates from binary logic become negated-minimum gates in ternary logic, and the NOR gates from binary become negated-maximum gates in ternary.

All basic gates are implemented in voltage mode. The corresponding voltage levels are: 0V for *0 logic*, 2.5V for *1 logic* and 5V for *2 logic*.

II.1. Ternary inverters

The truth table for all inverters is presented below, in Table 1 [2].

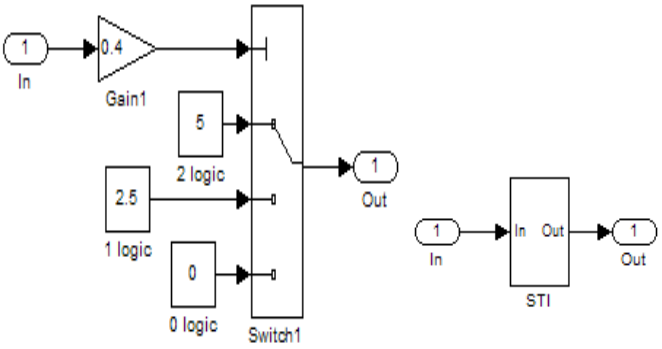
Table 1. Truth table of ternary inverters

Input	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

II.1.1. Simple Ternary Inverter (STI)

For STI one possibility to build the circuit in Simulink is to use a multiport switch block, with one control port (the first one) and three data ports. The block diagram is presented in Figure 1.

Depending on *In* values, the *Switch 1* transmits to the output *Out* the electrical value corresponding to one of the three logical levels. For example, if the input *In* is 0V, the control is "0" and to output the *2 logic* will be transmitted, meaning 5V. If the input is 2.5V, the control is "1" (due to the gain block *Gain2*) and the output is 2.5V (*1 logic*). And finally, considering for input 5V, the control will be "2" and the output will be 0V (*0 logic*).



a) b)

Figure 1. Simple Ternary Inverter. a) Block diagram; b) Symbol

The simulation results for STI circuit are presented in Figure 2.

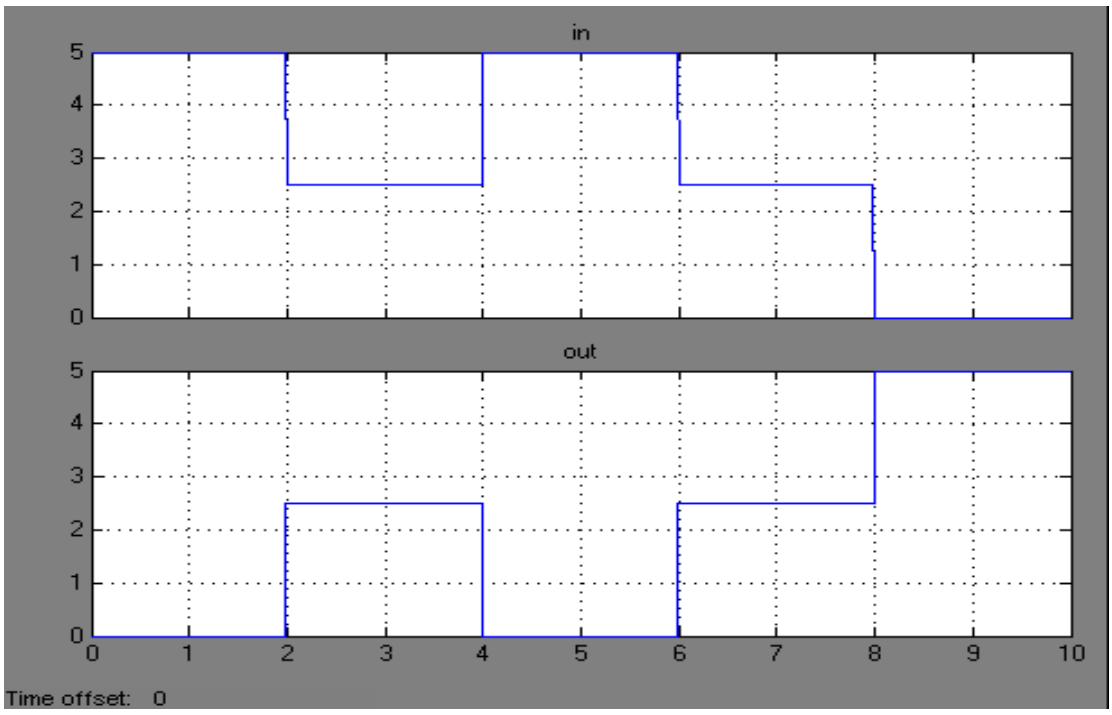


Figure 2. Simple Ternary Inverter – Simulation waveforms

II.1.2. Negative Ternary Inverter (NTI)
For NTI we use the a similar block diagram with the one used for STI, but when the input *In* is 2.5V the *Out* becomes 0V (*0 logic*).

II.1.3. Positive Ternary Inverter (PTI)
The difference between NTI and STI is that for the second one the output *Out* becomes 5V (*2 logic*), instead *1 logic* for STI. In the rest, the block diagram remains unchanged.

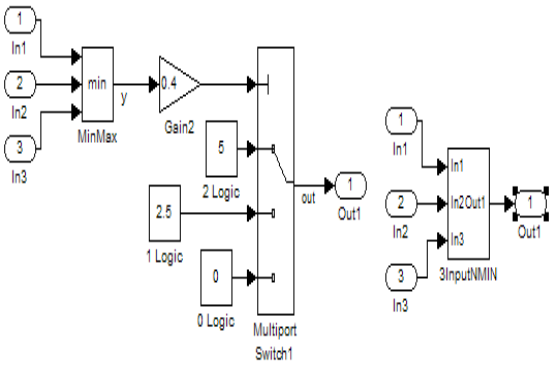
II.2. Minimum and negated-minimum gates
The equations of the minimum gates output Out_{MIN} and the negated-minimum gates output Out_{NMIN} (regardless of the inputs number) are:
$Out_{MIN} = \min(in_1, in_2 \dots in_x)$
Out_{NMIN}= 2 if $\min(in_1, in_2 \dots in_x)=0$
= 1 if $\min(in_1, in_2 \dots in_x)=1$
= 0 if $\min(in_1, in_2 \dots in_x)=2$

The minimum circuits are realized in Simulink using the MIN blocks. To obtain the negated-minimum gates we simply connect two gates: the minimum gate and the STI gate (the output of minimum gate is considered input for STI gate); the output of STI represent the output of the negated-minimum gate. In this manner we can design minimum and negated-minimum gates with more inputs.
The most used are two-input and three-input gates. For the three-input negated-minimum gate the block diagram and the symbol are presented in Figure 3, while the simulation results are presented in Figure 4.

II.3. Maximum and negated-maximum gates
For the maximum gates and the negated-maximum gates the equations of outputs becomes:

$Out_{MAX} = \max(in_1, in_2 \dots in_x)$
Out_{NMAX}= 2 if $\max(in_1, in_2 \dots in_x)=0$
= 1 if $\max(in_1, in_2 \dots in_x)=1$
= 0 if $\max(in_1, in_2 \dots in_x)=2$

We use the MAX block from Simulink to realize the maximum circuits. The negated-maximum gates are obtained connecting the maximum gate and the STI gate (the output of maximum gate is considered input for STI gate); the output of STI represent the output of the negated-maximum gate.



a) b)

Figure 3. Three-input negated-minimum gate a) Block diagram; b) Symbol.

We built in Simulink the maximum and negated-maximum gates with two and three inputs. Due to the lack of space, the block diagram, the symbol, and the simulation results are not presented here.

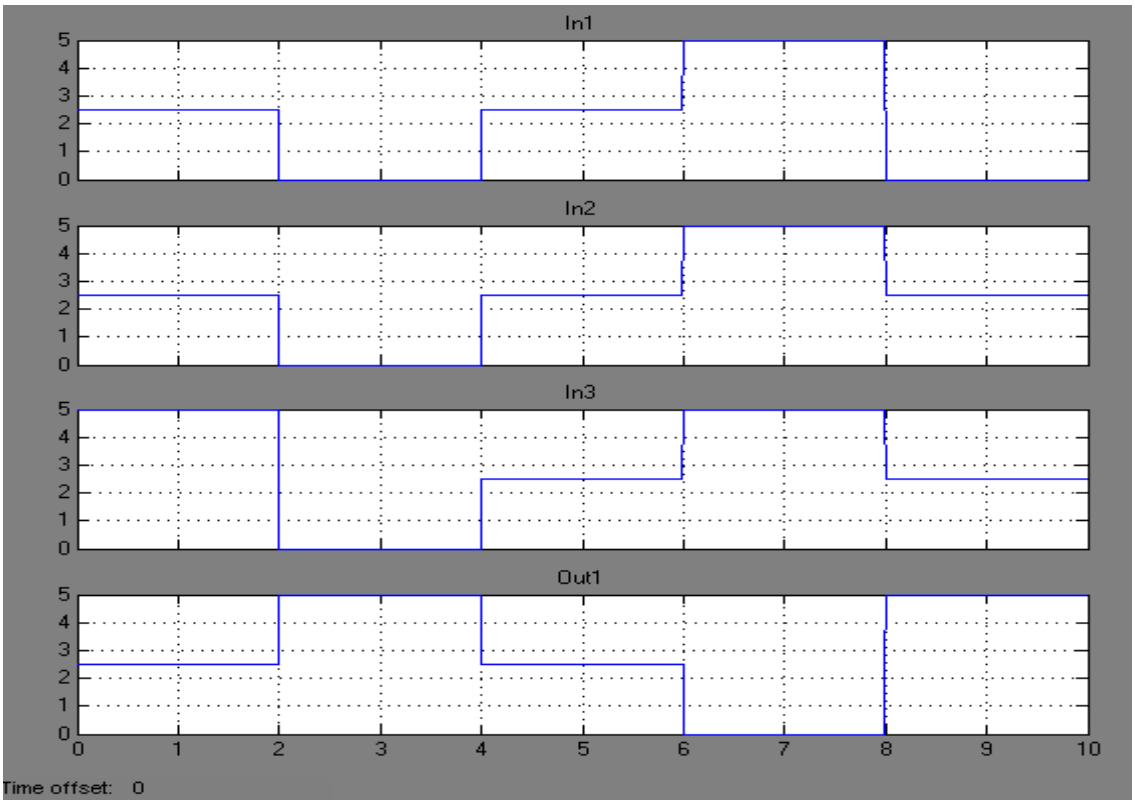


Figure 4. Three-input negated-minimum gate – Simulation waveforms

III. TERNARY D FLIP-FLAP-FLOPS

With the basic gates from our library, combinational and sequential circuits can be designed. The sequential circuits are more difficult to implement, comparing with the combinational ones, due to the appearance of the clock signal.

The binary flip-flops are used in many applications, such as: shift registers, frequency dividers, counters, parallel data storage circuit phase detectors [11-13]. The D flip-flap-flop can be also used in all above mentioned applications.

III.1. D Flip-flap-flop with binary clock

The starting point to implement the ternary D flip-flap-flop is the circuit of the binary D flip-flop [2]. The "core" of the D flip-flop is the RS flip-flop.

So, first, we implemented in Simulink the ternary RS flip-flap-flop, replacing the binary NAND gates with the ternary negated-minimum gates. Next, using the STI gate, we develop the ternary D flip-flap-flop. The block diagram and the symbol of ternary D flip-flap-flop are presented in Fig.5.

As inputs, the D flip-flap-flop has the *clk* and the *Data* inputs, and the outputs are denoted *Q* and *Qneg* (negated *Q*). The operation of the ternary D flip-flap-flop is illustrated in Table 2. Qprev is the previous state of the Q output. x denotes a *Don't care* condition, meaning the signal is irrelevant.

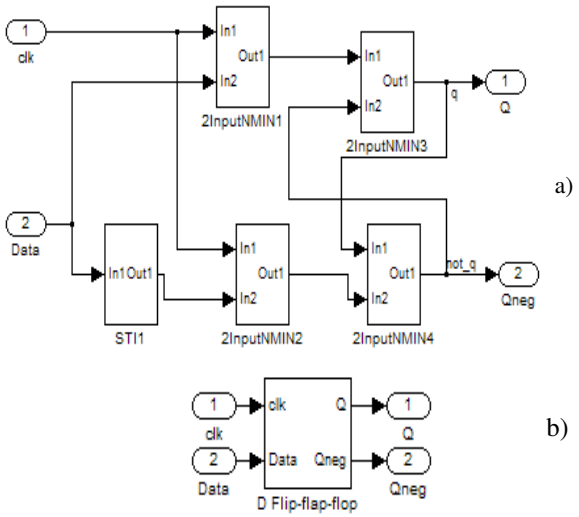


Figure 5. Ternary D flip-flap-flop
a) Block diagram; b) Symbol

Table 2. Truth table of the ternary D flip-flap-flop

clk	Data	Q	Qprev
2	0	0	x
2	1	1	x
2	2	2	x
0	x	Qprev	

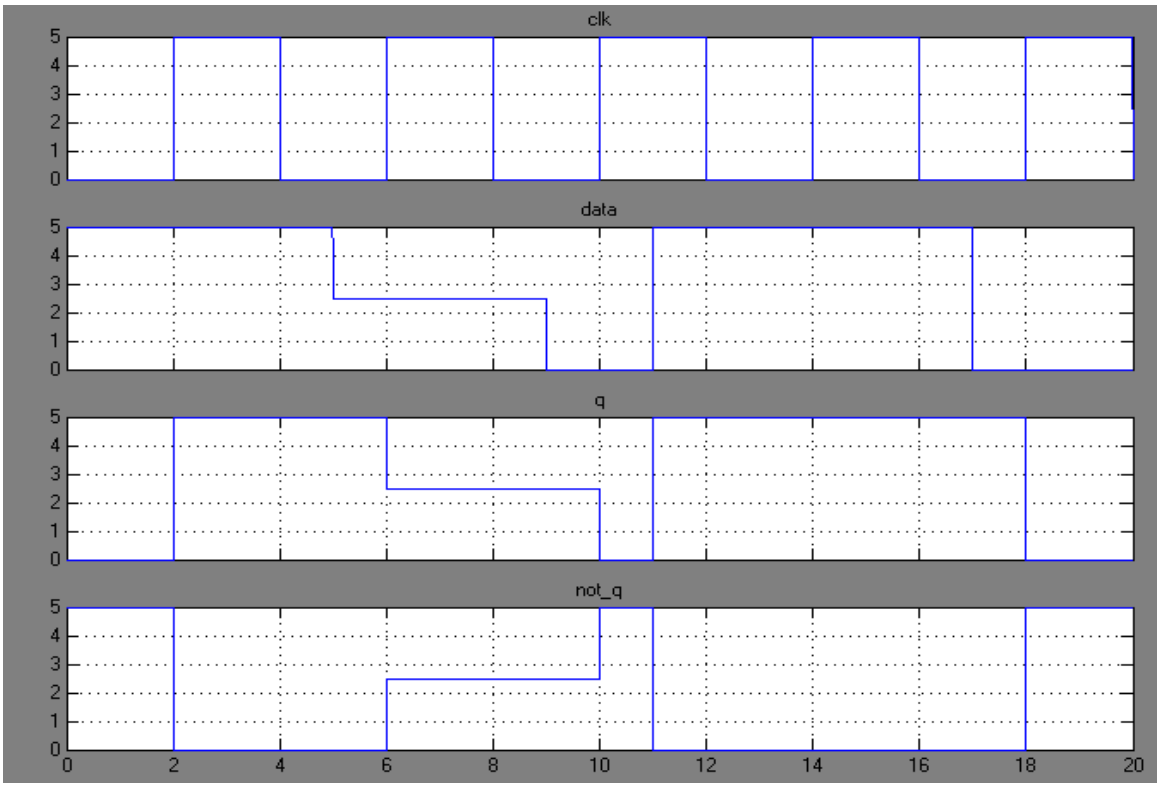


Figure 6. Ternary D flip-flap-flop with binary clock – Simulation waveforms

The *Data* input is a ternary one, and we keep the binary clock as *clk* input. The simulation results are presented in Figure 6.

When clock is high, the D flip-flap-flop read the value of *Data* input and transmit this value to the output *Q*. The ternary D flip-flap-flop is able to transmit all three logic levels: *0 logic* (11-12 and 18-20 time intervals in Fig.6 – *q* waveform), *1 logic* (6-8 time interval) and *2 logic* (2-4, 11-12 and 14-16 time intervals). When clock is low, the D flip-flap-flop keeps its previous state.

III.2. D Flip-flap-flop with ternary clock

In applications where the clock has a bigger importance, such as frequency dividers, the ternary D flip-flap-flop with binary clock works like a binary D flip-flop. In such applications the clock must be a ternary one. The simulation results for our ternary D flip-flap-flop when a ternary clock is used are presented in Fig.7.

When the clock takes extreme values (*0 logic* and *2 logic*) the D flip-flap-flop with ternary clock works similar with D flip-flap-flop with binary clock. When the clock takes the intermediate logic value (*1 logic*) the value of the *Q* input depends on the value of *Data*.

The truth table of the obtained D flip-flap-flop with ternary clock is Table 3.

Table 3. Truth table of the ternary clocked D flip-flap-flop

clk	Data	Q	Qprev
2	0	0	x
2	1	1	x
2	2	2	x
1	0	0	0
		1	1, 2
1	1	1	x
1	2	1	0, 1
		2	2
0	x	Qprev	

IV. CONCLUSIONS

A library of ternary basic building blocks implemented in Simulink is presented. The blocks are: inverters, minimum, negated-minimum, maximum and negated-maximum. With these basic gates we constructed sequential ternary circuits, such as D flip-flap-flops, with binary and ternary clock. The output of binary clocked D flip-flap-flop depend on the current state of *clk* and *Data* inputs, and the output of ternary clocked D flip-flap-flop depend on the current state of *clk* input and the current and previous states of *Data* input. The simulation results validate the correct operation for all implemented building blocks.

The basic building blocks can be further used to

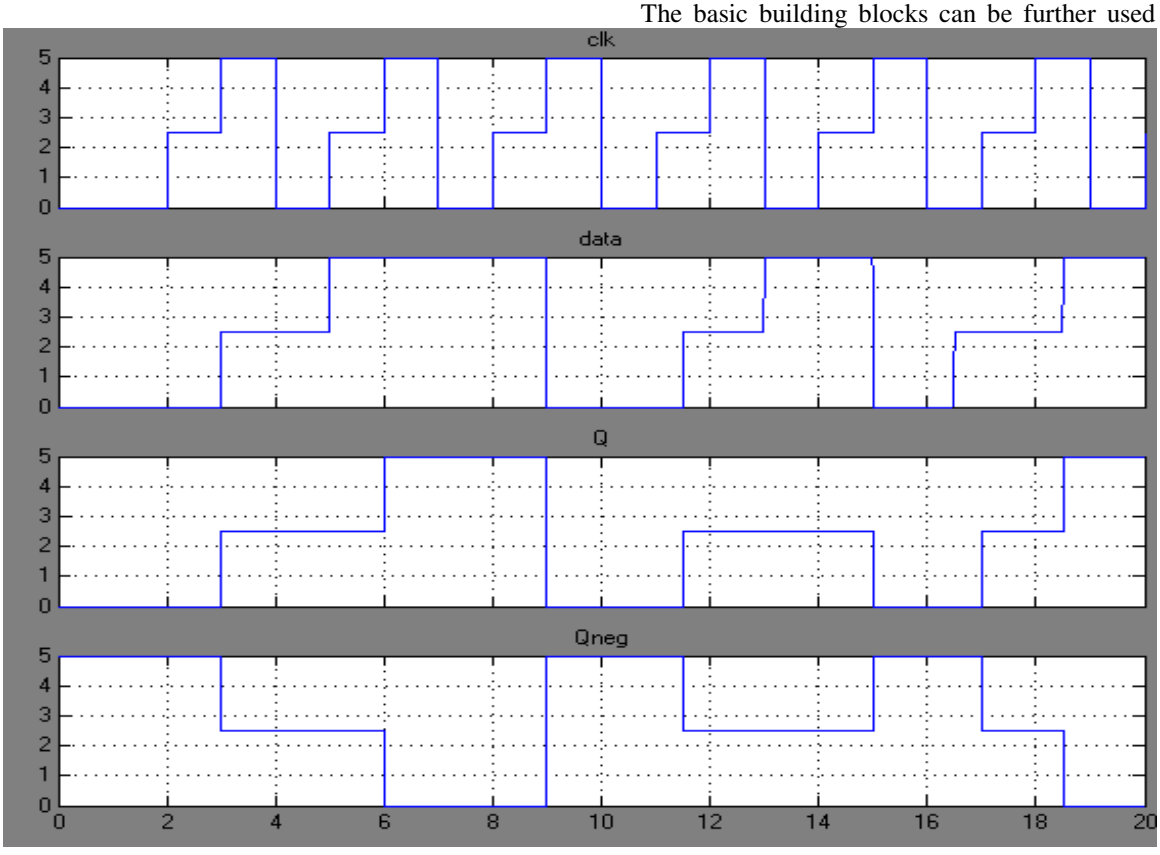


Figure7. Ternary D flip-flap-flop with ternary clock – Simulation waveforms

design even more complex circuits, like multiplexers, arithmetic circuits, coding circuits, etc. And ternary D flip-flap-flop offers the possibilities for complex applications to be realized. Basically, all the applications of binary D flip-flops can be accomplished, with less wiring, by ternary D flip-flap-flops. Another advantage of the implemented ternary
flip-flap-flop is that the flip-flap-flop can be used in today binary technologies, without any adaptation circuits.

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