HARDWARE IMPLEMENTATION OF DIVERSITY SCHEME FOR MIMO COMMUNICATION

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Abstract: Because of the tremendous growth of wireless communication and the demand for faster communication, new applications have developed such as broadband wireless Internet access. To cope this demand for increased capacity, multiple antennas can be used for improving the performance of wireless communication systems. The aim of this paper is to implement a simple multi-antenna scheme, a 2x1 Alamouti code, on a Xilinx FPGA connected via UART to an Iris mote. Our focus is to make a practical testing for MIMO system within indoor environment using external peripherals of Iris mote and communication protocols. To accomplish this, the Iris platform has to be configured to run over I2C to the class Spartan 3E board, and the Spartan's UART port is utilized to issue Iris radio communication stack.

Keywords: *FPGA, MIMO, Iris mote, radio communication.*

I. INTRODUCTION

Multi-antenna transmission schemes, using multiple antennas at the transmitter and/or receiver and the associated coding techniques have been proposed as a way to meet the demand for increased capacity and the performance of wireless communication systems. Multiple antennas have the capacity to increase communication data rates by 10-20 times above current system data rates. To have reliable wireless communications it is useful to use more channels, which in multi-antennas system these individual channels are not quite separate transmission channels. These systems use multipath propagation to provide independent channels even though the radio signals are being sent across the same transmission environment. Unfortunately, the wireless environment is characterized by time-varying multipath propagation. The most efficient way to mitigate fading effect in a wireless system is transmitter power control but the problem with this approach is the dynamic range. Another technique are time and frequency diversity, which have been applied to base station in order to improve their reception quality.

There are some interesting approaches for transmit diversity that have been suggested, but the technique proposed by Alamouti is the scope of this article. The Alamouti scheme improves the signal quality at the receiver by simple processing across two transmit antennas. This is done without feedback from the receiver to the transmitter and requires no bandwidth expansion. So, with small computation complexity , the transmit diversity scheme can improve the error performance,data rate or capacity of wireless systems. In other words the new scheme, with small computation complexity, is effective in all of the applications where system capacity is limited by mutipath fading.

The objective of the project is to present a hardware implementation of a wireless communication system based on Alamouti's transmit diversity technique using two transmit antennas and one receive antenna. The reason for wanting such a system is to be able to make a practical testing of MIMO systems. This system uses programmable logic components as FPGAs (field programmable gate array) which offers a high performance hardware alternative and can be reprogrammed to perform different tasks. The radio modules are based on IRIS mote which is a product fabricated and distributed by Crossbow Technology. These chips are used on the FPGA as radio transmitters ans receivers.

II. SYSTEM ARCHITECTURE

The system includes two transmitters and a receiver each equipped with two Iris motes separated by a wireless channel. The relationship between the transmitted and received signals is:

$$r = Hs + n \tag{1}$$

where H is the channel matrix, s is the transmitted signal vector, r is the received signal vector and n is the noise vector. There are some assumption made for the designed system concerning the fading and inputs which are constant for the duration of the enconding process, two consecutive symbols. As an optimization, the input bits are modulated into symbols of real and imaginary and these numbers and integers. The receiver is assumed to have knowledge of the channel experienced by the signal. That way the design needs a Maximum Likelihood detector and a channel estimator. A way of implementing the channel estimator is to multiply a matrix

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by another constant matrix, meaning a complex matrix multiplier. Also, there is no noise and intereference present at the receiver.

The components which have been implemented in VHDL were the transmitter and the receiver part, except for the channel by mentioning the transmission between the designed transmitter and receiver system is done in a real wireless environment. The implemented components were first tested to verify the correct operation. However, the individual components have not yet been joined together to form a complete system. So, further is presented by detail structure of each component in the system and the characteristic waveform.

ALAMOUTI TRANSMITTER

Fig.1 shows the block diagram of Alamouti transmitter consist of three sub-blocks, serial-to-parallel converter, QPSK modulator and Alamouti encoder.

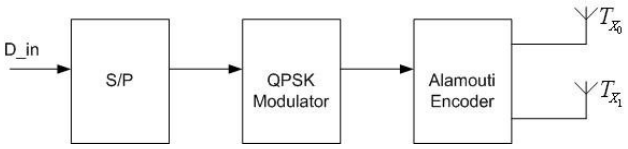

Figure 1. Alamouti transmitter.

The modulator takes a single bit as input and outputs 8 bit signed numbers representing the real and imaginary parts of the modulated numbers. A litlle more complicated is the Alamouti encoder because containts sequential logic which requires some control logic and clock signal. The encoder has four eight bit inputs, the real and imaginary parts of the two symbols being encoded. The inputs are not saved and are assumed to be constant for two clock cycles, how long it takes the encoding process. The encoder outputs four eight bit symbols for the real and imaginary part. These outputs are further fed over the eight bit UART connection into the radio modules on the motes. The transmitter block is designed to operate at the same clock speed as the data rate of the FPGA, so one clock cycle is assumed to be one symbol period. Therefore, two clock cycles are needed to encode two symbols and the resulted output waveforms are shown in Fig.2.

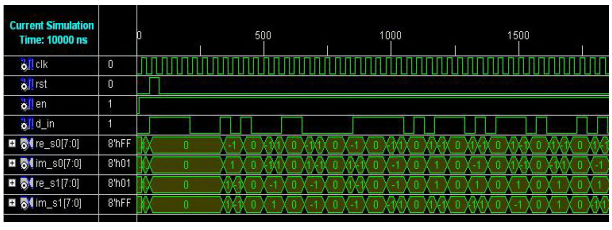

Figure 2. Output waveform of Alamouti transmitter.

ALAMOUTI RECEIVER

The next part of the communication system is the receiver, which consists of two sub-blocks. The Alamouti decoder and QPSK demodulator form the Alamouti receiver. The signal received at the antenna is injected into the Alamouti decoder where the signal is decoded according to the decoding algorithm of the Alamouti transmit diversity technique. The Alamouti diversity technique design consists of four complex multiplier units and four associated add/substract units with registers two store intermediate results.

There is also a finite state machine component for driving the datapath's control lines of the multiplier, add/substract and registers with the correct values in the appropriate clock cycles. The control signals are shown in fig.4. Seven states are required since the datapath's operation is repeating computation covering seven clock cycles. The reception of several signals from a Alamouti transmitter at one antenna may combat the intersymbol interference (ISI) created by multipath propagation. Therefore, from Fig.3 it can be seen the implementation of a 2X1 MIMO receiver based on equalizers, used for decoding the signals.

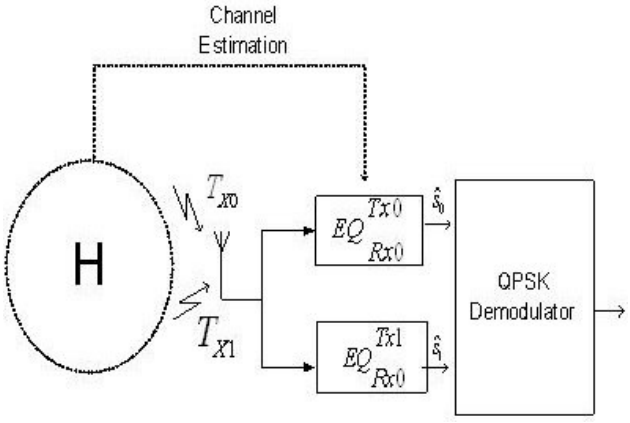

Figure 3. Alamouti receiver based on equalizer.

For each bit stream broadcasted there is an equalizer present at each receive antenna. Assuming that the receiver has knowledge of the channel, the transmited signal is asserted in the equalizer and the result produced is drawn in fig.4. Upon the combining process the signals are sent to the Maximum Likelihood detector which is decoupled since two symbols are coded together and detected independently at the receiver. In order to verify the hole testbed design written in VHDL, the channel estimator and the Maximum Likelihood detector were not implemented since the channel modeling modifies the transmitted signal to behave as if the signal had been propagated over the wireless medium. These two complex numbers from each antenna are received at two consecutive symbol periods.

The ecuations proper to each antenna are decoded according to the code matrix of Alamouti. Therefore, the design consists of four multipliers, four add/substract blocks and registers to store the data. All the equations for the symbol estimates are computed in parallel, so each equation has two multiplexers(one for the channel coefficients and one for the transmitted signal), one multiplier and one add/substract. As mentioned earlier the control logic is implemented as a state machine in order to control the add/substract units, registers and multiplexers. Since the multipliers take one clock cycle to process the result and the add/substract block another clock cycle, two symbol estimates (real and imaginary parts) are computed after eight clock cycles.

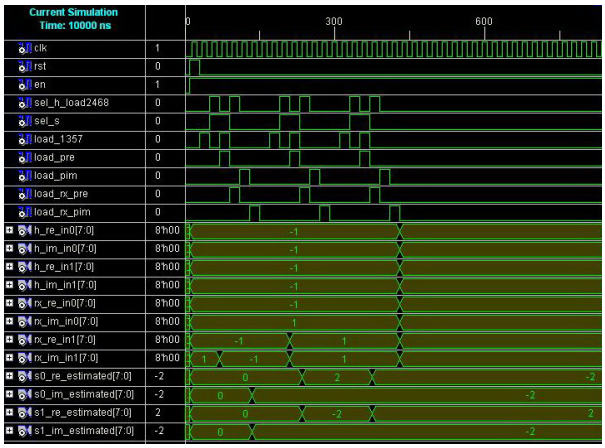

Figure 4. Output of the estimated signals at the receiver

SPARTAN 3E

The Spartan board is a versatile device with many options. For our project it is possible to use only one of the two jumpers interfaces, J1 or J2, both configured for I^2C communication, and both UARTs configured for Iris (the latest generation of motes from Crossbow Technology[3]). We have to create extension cables from Hirose 51-pin expansion connector on the motes to the Spartan board. We also have the flexibility of using either of the UART ports, as the cable connection for connecting to the mote devices is a female and our serial cables for connecting to the computer is a male. Because we decided to do serial transmission we also have to do a choice regarding the type of communication. Now, if we are using synchronous communication means to share the same clock between the mote and FPGA. Therefore the FPGA rate must be slowed because the mote has a 8 Mhz oscillator and the Spartan 3E operates at 50 Mhz oscillator.

The FPGA is the main processing component under the control of a Picoblaze processor on the Spartan board. Further, we use a terminal emulator, such as Hyperterminal, to download SPI Flash programming data via the PC's serial port to the FPGA[1].

INTERFACING FPGA WITH IRIS MOTE

The second testing platform (fig. 5) is a small device which belongs from a Wireless Sensor Network developed by Crossbow, equipped with an RF transceiver, a battery, multiple sensors and typically a small microcontroller. The transceiver enables communication with other nodes and base station while the microcontroller controls the communication and gives the nodes local data processing ability. The part which will be used is a 2.4 GHz radio transceiver module integrated with a Atmega1281 micro-controller and it's used to establish communication between the link parts.

The mote software is a free and open source operating system (TinyOS) and support platform developed specifically for wireless networks. It's written in nesC programming language and provides a common set of commands and libraries that can be used on multiple hardware platforms.

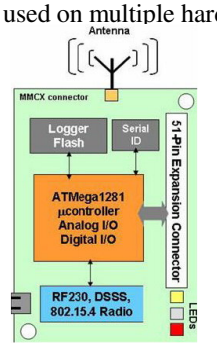

Figure 5. Block diagram of the Iris

The project plan is summarized in fig.6 and involves testing all the components as a system to verify that it performs the required task. First of all, at the transmitter part, the Alamouti diversity scheme impelemented in VHDL is downloaded on the FPGA. Further, the mote connected with the FPGA expects a sample when is ready to send data.

The mote it will be programmed to receive and transmit data before it is connected to the Spartan 3E platform. This initial programming allows the mote to communicate with the other mote and also with the FPGA module. Initially the mote will be connected to the mib520 module (which acts as a master node for motes) developed also by Crossbow and further will be programmed to enable communication with other mote through radio channel. On the receiver it is configured as required, gathered data from the transmitter's mote is passed into the microcontroller of the receiver mote and further transferred to the FPGA.

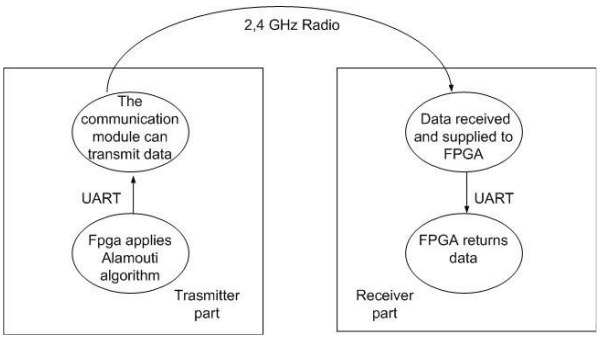

Figure 5. Dataflow of the communication process

III. CONCLUSIONS

In this paper has been proposed a hardware implementation of a wireless communication system based on Alamouti's transmit diversity technique using two transmit antennas and one receive antenna. The reason for wanting such a system is to be able to make a practical testing of MIMO systems within indoor environments using FPGAs and Iris mote.

First milestone was to code and verify using VHDL the functionality of the two transmit antenna and one receive antenna with the encoding and decoding algorithm. The enconder from the transmitter design does not increase significantly complexity since the only operation the Alamouti

encoder makes on modulated signals is the negation of either real or imaginary part of a symbol. The output are two streams of modulated symbols which are downloaded in FPGAs each driving a separate antenna. The receiver's design implied more complexity since the Alamouti decoder implemented complex multipliers meaning an amount of resources on the FPGA. Therefore this work proved it is feasible to implement an Alamouti code on the FPGAs.

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