AN ADAPTIVE DIGITAL COMPENSATION DESIGN FOR BUCK CONVERTER TOPOLOGY

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Abstract: This paper presents a digital type III compensator that needs no calculation made by a designer. First an analog type III compensator is designed for a buck converter and based on it the digital model is obtained. Both the analog and digital approaches are simulated in PSIM and the digital compensator is written in a Microchip dsPIC for experimental results. The dynamic response of these controllers under input voltage change and load current variations are presented.

Keywords: *digital control, buck converter, type III analog compensator, type III digital compensator.*

I. INTRODUCTION

Digital control is more and more used in switched mode power supplies because of the ease of implementation and the advantages given by the adaptability of the controller to the changes in the compensation loop [1], [5]-[7], [11]-[14].

The easiest way to obtain a digital controller is first to design an analog compensator and transpose it in the digital domain using the bilinear transformer [10].

The disadvantages of such a method are the mathematical calculus needed to obtain the values of the passive components for the compensator and the fact that if the designer decides to change the hardware, the calculus must be reevaluated.

In this paper first a type III [8] analog controller with its time domain transfer function and frequency response is presented. The analog compensator was designed without any adjustments only by placing the position of the poles and zeros by a first approximation based on the buck converters passive components. This method it is used because the goal of this paper is to obtain a digital controller dependent only on the values of the converter.

The type III digital controller is obtained from the transfer function of an analog type III controller transposed into digital using the bilinear transformer [2], [3], [6].

After mathematical calculations the z coefficients for the linear difference, equation needed to implement the compensator in a microcontroller, are obtained. These coefficients are dependent only on the pole-zero placements.

The pole zero placements, are obtained from calculation similar to the analog design using only the given values of the converter parameters.

The advantage of this digital compensator is that the user does not need to calculate anything if he wants to close the loop for a converter, the only data needed to be transferred to the controller are the parameters of the converter.

The control mode used in this paper is voltage mode control [9], [4].

The models are first simulated and the results are compared, and then the experimental results are presented.

The analog compensator was built using the TL494 circuit for the modulated control signal, and the digital compensator was implemented in a Microchip dsPIC30F2020 for the same buck converter in voltage mode control.

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II. THE BUCK CONVERTER IN ANALOG VOLTAGE MODE CONTROL

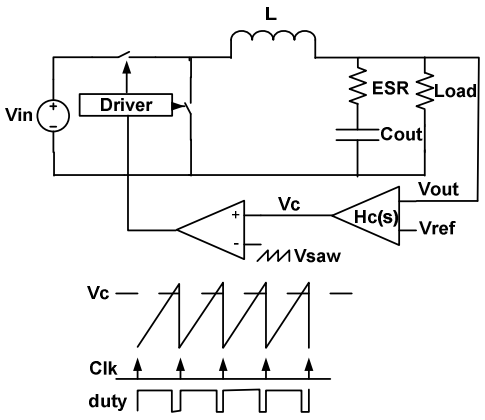

Figure 1. Voltage mode control buck converter.

In figure 1 a synchronous buck converter in voltage mode control is presented.

In voltage mode control an external signal is compared with the control signal obtained, for generating the duty cycle needed to have the wanted output voltage (*figure 1*).

The output voltage V_{out} is monitored and subtracted from the reference value V_{ref} and an error signal results. This error signal is then used for the resulting control signal. The control signal is compared with the external ramp and a pulse width modulated signal is sent to the drivers of the switches so the converter can react in such a way to reduce the output error.

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The type III compensator presented in figure 2 introduces two zeros and three poles. The two zeros boost up the phase with 180 degrees needed to counteract the effect of the output double pole.

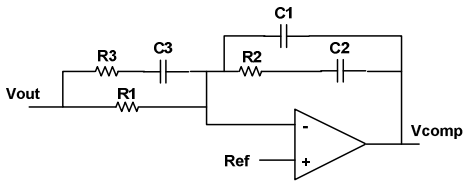

Figure 2. Analog type III compensator.

The transfer function for the type III converter is presented in equation 1.

$$H_c(s) = \frac{\omega_{p0}}{s} \cdot \frac{\left(\frac{s}{\omega_{z1}} + 1\right) \cdot \left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right) \cdot \left(\frac{s}{\omega_{p3}} + 1\right)} \tag{1}$$

The ω_p and ω_z coefficients represent the angular frequencies of the poles and zeros of the compensator. For the ease of interpretation the angular frequencies are replaced by frequencies in table 1.

The link between the angular frequencies of the poles and zeros and the passive components of the type III compensator is presented in the equations 2-6.

$$\omega_{z1} = \frac{1}{R_2 \cdot C_1} \tag{2}$$

$$\omega_{z2} = \frac{1}{C_2 \cdot (R_1 \cdot R_3)} \tag{3}$$

$$\omega_{p0} = \frac{1}{R_1 \cdot (C_1 + C_3)} \tag{4}$$

$$\omega_{p2} = \frac{(C_1 + C_3)}{R_1 \cdot C_1 \cdot C_3} \tag{5}$$

$$\omega_{p3} = \frac{1}{R_3 \cdot C_2} \tag{6}$$

By choosing the frequencies of the poles and zeros in such a way that the system is stable and the response of the converter is fast enough at load changes one can determine the physical values of the passive components.

In figure 3 the theoretical Bode plot of the type III compensator is presented. The position of the poles and zeros is chosen based on the parameters of the buck converter using the simple approximate method.

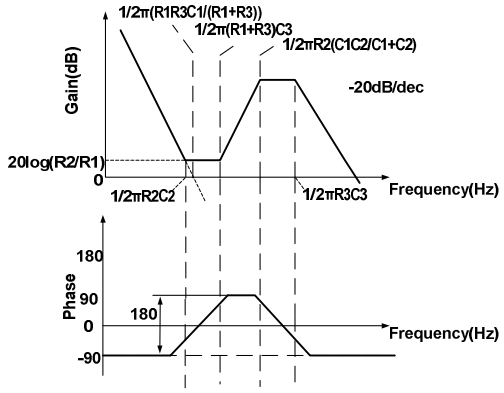

Figure 3. Theoretical Bode plot.

First the frequency of the output double pole (*equation 7*) and the frequency of the pole introduced by the output capacitor and its parasitic series resistance (*equation 8*) are calculated.

$$F_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{out} \cdot C_{out}}} \tag{7}$$

$$F_{ESR} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{out}} \tag{8}$$

In table 1 the choice of the poles and zeros based on the parameters of the converter is presented.

F_{p0}	F_{p2}	F_{p3}	F_{z1}	F_{z2}
$\frac{V_{ramp} \cdot f_x}{V_{in}}$	F_{ESR}	$\frac{F_{sw}}{2}$	$\frac{F_{LC}}{2}$	F_{LC}

Table 1 Poles and zeros placement

V_{ramp} is the amplitude of the sawtooth signal, f_x is the crossover frequency, V_{in} is the input voltage and f_{sw} is the switching frequency of the converter.

Parameters	Value
Output Voltage(V_{out})	5V
Input Voltage(V_{in})	8V
Switching frequency(f_{sw})	100kHz
Load(R_L)	5Ω
Output capacitance(C_{out})	680μF
Inductance(L_{out})	47μH
Capacitor parasitic resistance(ESR)	0.1Ω
Sawtooth amplitude(V_{saw})	1V
Cross over frequency(F_x)	5kHz

Table 2 Buck converter parameters

Based on the parameters of the buck converter from table 2 the calculated values of the poles and zeros frequencies for

the type III compensator are presented in table 3.

F_{p0}	F_{p2}	F_{p3}	F_{z1}	F_{z2}
625Hz	2.34kHz	50kHz	445Hz	890Hz

Table 3 Poles and zeros position

From equations 2-6 and with R_1 chosen to be 5.1kΩ to reduce the degrees of freedom, the values of the passive components for the analog type III compensator are determined and presented in table 4.

R_1	R_2	R_3	C_1	C_2	C_3
5.1kΩ	9.1kΩ	91Ω	47nF	33nF	10nF

Table 4 Type III compensator passive components

With this calculated values the converter with type III analog compensation voltage mode control is simulated in Psim software (*figure 4*).

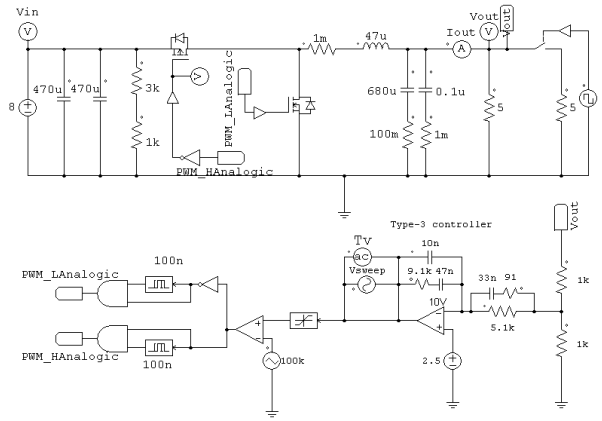

Figure 4. Analog voltage mode control buck converter.

In the simulation the dead time for the PWM is set to 100ns and for load change a 5Ω resistor is connected in parallel.

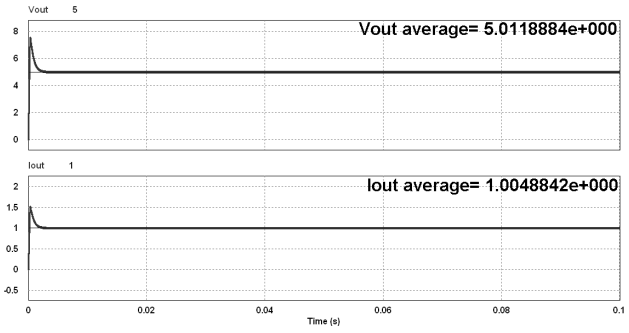

Figure 5. Simulated output voltage and current.

In normal working condition without any change in the input voltage and output load the average value of the output voltage is 5.0V and the average output current is 1A (*figure 5*).

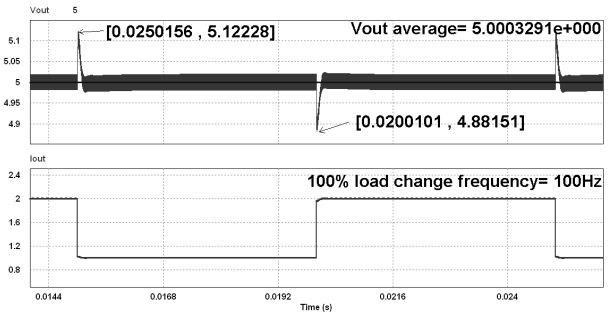

Figure 6. Output voltage at load change.

In figure 6 the output voltage when the load changes by 100%, is illustrated. It can be observed that the maximum output voltage at positive current step of 1A is 5.122V and the minimum output voltage at negative current step of 1A is 4.88V.

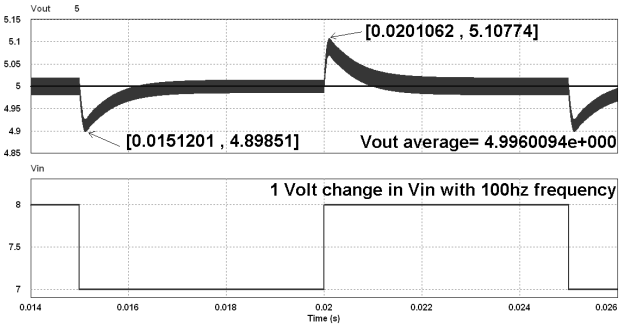

Figure 7. Output voltage at input voltage change.

In figure 7 the output voltage when the input voltage drops with 1V is illustrated and it can be seen that at positive step the output voltage reaches 5.1V and at negative step it reaches 4.89V.

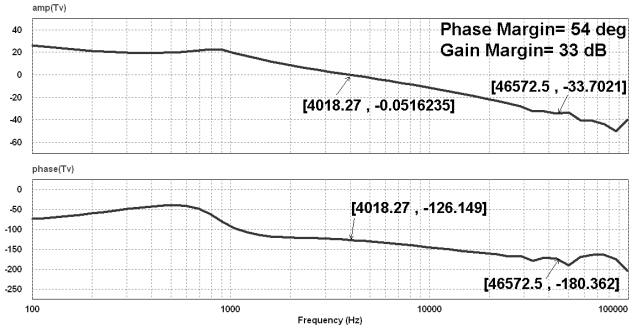

Figure 8. Closed loop bode plot.

In figure 8 the closed loop bode plot of the buck converter is illustrated and some conclusions can be drawn about the stability of the power supply.

The phase margin of the converter is 54 degrees and the gain margin is 33 dB. In order for the power supply to be stable the phase margin must be greater than 40 degrees and the gain margin must be greater than 10 dB. From figure 8

one can conclude that the design is stable.

As a result a digital controller is built using the same simple approximate method when choosing the position of the poles and zeros.

III. DIGITAL CONTROL

Based on the analog compensator time domain transfer function using the bilinear transformer (*equation 9*) the z domain transfer function of the digital controller is obtained.

$$s = \frac{2}{T_s} \cdot \frac{(z-1)}{(z+1)} \tag{9}$$

In equation 9 T_s is the sampling interval of the converter.

Substituting s (equation 9) in H(s) the following H[z] transfer function (e*quation 10*) is obtained.

$$H[z] = \frac{y[z]}{x[z]} = \frac{B_3 \cdot z^{-3} + B_2 \cdot z^{-2} + B_1 \cdot z^{-1} + B_0}{-A_3 \cdot z^{-3} - A_2 \cdot z^{-2} - A_1 \cdot z^{-1} + 1} \tag{10}$$

The parameters of the digital filter B_3, B_2, B_1, B_0, A_3, A_2, A_1 are determined by identification after H[z] is calculated. In this case x represents the error signal and y the value of the duty cycle.

After the calculations the values of the digital filters coefficients based on the position of the zeros and poles are presented in equations 11-17.

$$B_0 = \frac{T_s \cdot \omega_{p0} \cdot \omega_{p2} \cdot \omega_{p3} \cdot (2 + T_s \cdot \omega_{z1}) \cdot (2 + T_s \cdot \omega_{z2})}{2 \cdot \omega_{z1} \cdot \omega_{z2} \cdot (2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{11}$$

$$B_1 = \frac{T_s \cdot \omega_{p0} \cdot \omega_{p2} \cdot \omega_{p3} \cdot \left[-4 + 2 \cdot T_s \cdot (\omega_{z1} + \omega_{z2}) + 3 \cdot T_s^2 \cdot \omega_{z1} \cdot \omega_{z2}\right]}{2 \cdot \omega_{z1} \cdot \omega_{z2} \cdot (2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{12}$$

$$B_2 = \frac{T_s \cdot \omega_{p0} \cdot \omega_{p2} \cdot \omega_{p3} \cdot \left[-4 - 2 \cdot T_s \cdot (\omega_{z1} + \omega_{z2}) + 3 \cdot T_s^2 \cdot \omega_{z1} \cdot \omega_{z2}\right]}{2 \cdot \omega_{z1} \cdot \omega_{z2} \cdot (2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{13}$$

$$B_3 = \frac{T_s \cdot \omega_{p0} \cdot \omega_{p2} \cdot \omega_{p3} \cdot \left[4 - 2 \cdot T_s \cdot (\omega_{z1} + \omega_{z2}) + T_s^2 \cdot \omega_{z1} \cdot \omega_{z2}\right]}{2 \cdot \omega_{z1} \cdot \omega_{z2} \cdot (2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{14}$$

$$A_1 = \frac{12 - T_s^2 \cdot \omega_{p2} \cdot \omega_{p3} + 2 \cdot T_s \cdot (\omega_{p2} + \omega_{p3})}{(2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{15}$$

$$A_2 = \frac{-12 + T_s^2 \cdot \omega_{p2} \cdot \omega_{p3} + 2 \cdot T_s \cdot (\omega_{p2} + \omega_{p3})}{(2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{16}$$

$$A_1 = \frac{4 + T_s^2 \cdot \omega_{p2} \cdot \omega_{p3} - 2 \cdot T_s \cdot (\omega_{p2} + \omega_{p3})}{(2 + T_s \cdot \omega_{p2}) \cdot (2 + T_s \cdot \omega_{p3})} \tag{17}$$

In figure 9 the direct form of the IIR digital filter structure is presented. The time domain representation of this filter gives the linear difference equation (*equation 18*) needed by the microcontroller to perform the calculations for the duty cycle.

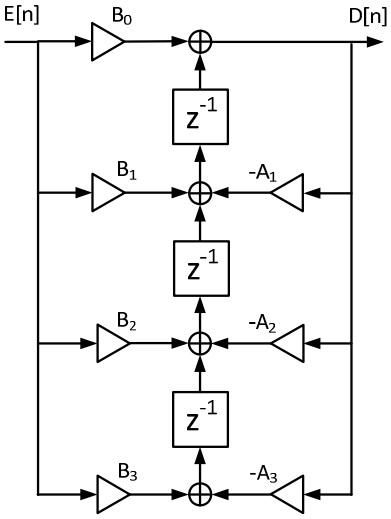

Figure 9. Digital filter structure.

$$\begin{aligned} y[n] &= A_1 \cdot y[n-1] + A_2 \cdot y[n-2] + A_3 \cdot y[n-3] + \\ &+ B_0 \cdot x[n] + B_1 \cdot x[n-1] + B_2 \cdot x[n-2] + B_3 \cdot x[n-3] \end{aligned} \tag{18}$$

X[n] is the error signal, x[n-1] is the error signal delayed by one unit, x[n-2] the error signal delayed by two units and x[n-3] the error signal delayed by three units.

Y[n] is the duty cycle, and y[n-1], y[n-2], y[n-3], are the values of the previous duty cycles respecting the same delay units as the error.

For simulation a DLL block is created in PSIM where this equation is implemented and the parameters for the buck converter are declared as variables. Before closing the loop the microcontroller represented by the DLL block computes the position of the poles and zeros and the values of the IIR filter coefficients.

After the computing is done, the duty cycle is updated every cycle based on the linear equation.

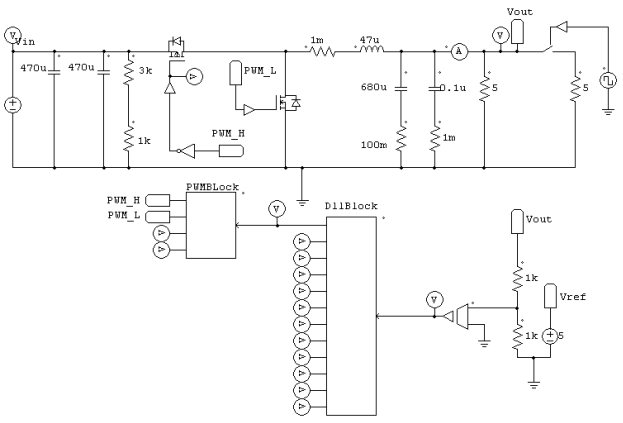

Figure 10. Simulation schematic for the digital compensator.

The simulation schematic for the digital compensator is presented in figure 10 and one can observe the DLL block containing the C code written for the 3-rd order IIR filter.

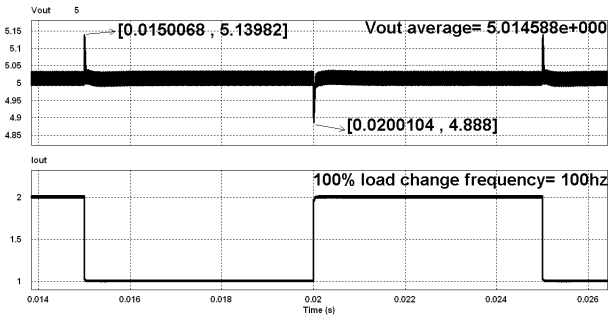

Figure 11. Output voltage at load change.

The response of the power supply at 100% load change is presented in figure 11 and the maximum value of the output voltage at positive output current step is 5.139V and at negative output current step is 4.888V. The average output voltage is 5.014 V.

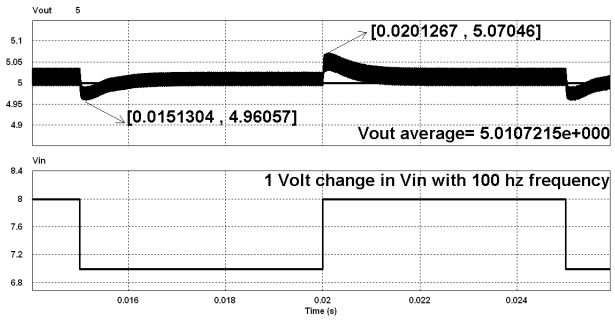

Figure 12. Output voltage at input voltage change.

In figure 12 the output voltage when the input voltage drops with 1V is illustrated and it can be seen that at positive step the output voltage reaches 5.07V and at negative step it reaches 4.96V and the average output voltage is 5.01V.

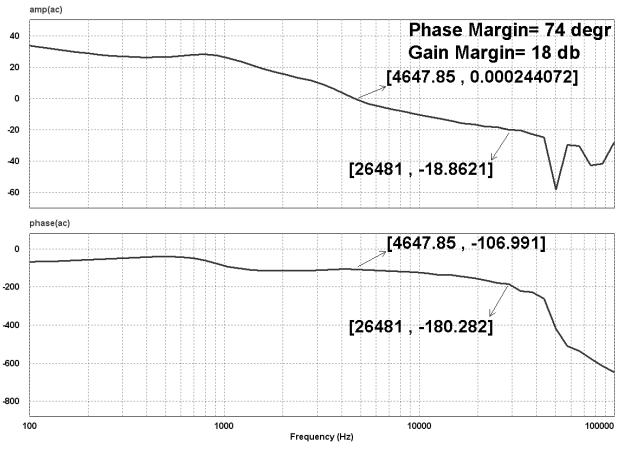

Figure 13. Closed loop bode plot.

For the buck converter in closed loop voltage mode control the Bode plots for gain and phase are illustrated in figure 13. The phase margin obtained after simulation is 74 degrees and the gain margin 18 dB. Both margins are greater than the limit and the power supply is stable.

IV. EXPERIMENTAL RESULTS

The experimental results for the analog domain are obtained using a buck converter laboratory made board with an analog type III compensator built around the TL494 PWM generator.

The board uses the same components for the buck as mentioned in table 2 and the same passive components for the type III compensator as obtained through calculation, that are presented in table 4.

The response of the power supply at 100% load change (750 mA to 1.5 A) is presented in figure 14. The converter is stable and as a conclusion the simple approximate method works well for the type III compensator. For the load step a Chrome electronic load was used and the waveforms were acquired with a Tektronix Ts2000 series oscilloscope.

For the digital controller experimental results a synchronous buck converter from Microchip using a dsPIC30F2020 is used and the 3-rd order digital IIR is implemented along with the equations for the calculation of the zeros and poles positions in Microchip MpLab using C language.

The algorithm includes a soft start, and in this time the values of the digital coefficients are computed using the passive components value provided by the designer.

For the output voltage measurement, the internal ADC converter of the dsPIC30F2020 is used. The ADC's interrupt is triggered by the PWM. The PWM module is set to work in complementary mode at 100 kHz frequency.

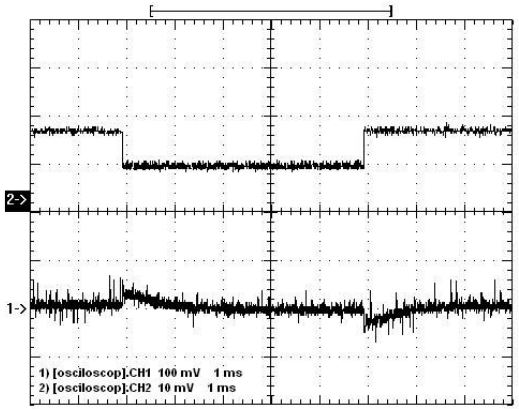

Figure 14. Response of analog experimental compensator.

In figure 15 the experimental results of the buck converter at 100% load change are presented. Compared with the results in figure 11 one can observe that the results are similar. The experimental results demonstrate that the mathematical model can be applied and the simple approximation method can be used in digital controllers.

The parameters needed by the microcontroller to calculate the poles and zeros positions are the one stated in table 2 and the user must change their values if there is any

change in the buck converter's hardware.

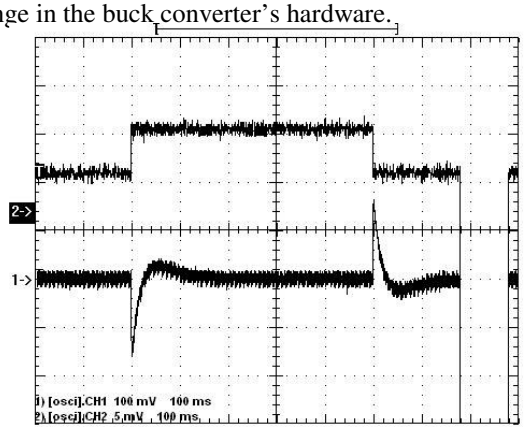

Figure 15. Response of experimental digital compensator.

The same equipments are used for the dynamic load and for the waveforms acquisition as for the analog controller.

V. CONCLUSIONS

The aim of this paper was to design a type III digital compensator that needs for closing the loop only the values of the passive components used in hardware.

The type III analog compensator was designed in the same manner as for the digital controller so a comparison can be made and the advantages and disadvantages of each method can be highlighted.

As it can be seen in the article the analog controller needs a lot of calculations to determine the values of the analog components used for the compensator and if the parameters of the converter are changed the mathematics must be reevaluated to get the new values of the compensation components.

Not only that a new set of values must be calculated but the physical compensator must be changed. This means that the engineer must solder new passive components to the board and this costs time and in some cases a new hardware.

Using the 3rd order digital IIR filter proposed in this paper, once the algorithm is implemented in the microcontroller if there is a change in the converter hardware, the designer has only to deliver the new values of the components to the controller. The advantages of the digital controller are the adaptability and the time it takes to use the controller for a new converter. Compared with the analog controller, the proposed digital controller needs no calculations made by the engineer if the hardware is changed, and also the compensator because it is software implemented needs no soldering or redesign of the board.

In terms of performance the analog controller is better than the digital controller but in low power designs and taking into account that the digital controller is more versatile and can deliver a stable converter without any calculation from the designer regarding the compensator, one can conclude that the digital compensator can be used successfully.

The digital controller can be tuned and more features can be added to the functionality.

In the paper the digital compensator was not tuned and the digital filter's coefficients were implemented in the hardware based on the equations obtained in the z domain and based on the simple approximation made upon the position of the poles and zeros, to show that even using the simplest method a stable system with good dynamics can be obtained knowing only the values of the converter, and without any calculations needed from the engineer.

In conclusion the simulations and the experimental results validate the method used and the implemented digital controller can be used for synchronous buck converters without any further calculation as long as the parameters of the converter are delivered to the controller.

ACKNOWLEDGMENT

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