TEST POWER OPTIMIZATION WITH REORDERING OF GENETIC TEST VECTORS FOR VLSI CIRCUITS

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Abstract: Power optimization is one of the important challenges in VLSI circuit for testing engineers. Larger power dissipation becomes the reason for overheating and with every increase in 10°C in operating temperature, failure rates for the component on a chip doubles. Power dissipation is directly proportional to switching activities of the components on Integrated Circuits. Power optimization is possible only by minimizing the toggling count (switching activity) for combinational and sequential components on a chip area. This paper describes novel technique of power optimization by rearranging the test patterns generated by Genetic Algorithm. The logic discussed here calculates and re-arrange these genetic test patterns according to minimum toggling arrangement of test patterns. This algorithm is applied on the ISCAS85 and ISCAS89 benchmark circuits. The experimental results show that maximum power dissipation in the combinational and sequential logic circuits are reduced by the average of 31% and 36% respectively.

Keywords: *GA (Genetic Algorithm), power optimization, Hamming Distance (HD), CUT (Circuit under Test)*

I. INTRODUCTION

With the continuous growth in the technology, the numbers of transistors on a chip are increasing at a rapid rate. Due to this testing of VLSI circuits becomes a very challenging job for the test engineers. There are various methods available for testing purpose but due to advancement there will be increase in number of transistors on a chip up to 180 million per square cm by 2012 [1].

The amount of test vectors required to test complex VLSI circuits are increasing. Handling with these large amounts of test vectors is a very tedious job. The new approach like genetic algorithm (GA), detects the faults with less number of test patterns and with in less span of time. The GA is a biological genetic process [2] producing optimal solution by selecting the parents from population which are in the form of binary strings and producing new infants by using cross over and mutation process. The fitness function is written according to the requirement of problem, and best solution is selected from new infants. GA is also effective in other VLSI applications like, cell placement [3], compacting randomly generated test sets [4] and channel routing [5]. In this paper target is to present the way to utilize GA for power optimization of VLSI circuits in conjunction with minimum hamming distance (HD) approach.

Power dissipation in complex circuits is related to various parameters like gate delays, switching or toggling of transistors clock frequency, process parameters, circuit topology and structure, and the input vectors applied. But here only two parameters are considered that are, applied input vectors and the switching of transistors. Patterns generated by GA process are able to detect the faults but it is not necessary that switching of transistor is less for that applied test pattern. Here emphasis is given on switching of transistors because power is directly related to the toggling count of the transistors according to the equation 1 [6].

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$$P = \left(\frac{V^2{}_{dd}}{2 * clock\ period}\right) * \left(\sum_{for\ all\ gates\ g} \left(toggle(g) * C(g)\right)\right) \quad (1)$$

Where V_{dd} represents biasing voltage, C(g) is the output capacitance of the nodes and toggle (g) is switching of the gates 'g'. From equation 1 it is clear that power is not only related to switching of gates but also related to output capacitance of the gate nodes. So during power optimization both number of toggles on a gate and its output capacitance is considered. Fitness function for GA is so written that it selects only those nodes which have highest output capacitance and the nodes on which maximum switching occurs. In this way maximum dissipated power and the input pattern for which it occur is calculated. So Total Power Dissipated (TPD) is given by equation 2 [7].

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$$TPD = \sum IT_n I * C_n \qquad (2)$$

Where, T_n is set of transitions and C_n is the output capacitance. Thus power dissipated is reduced by managing the HD value between the test pattern. Test patterns are so arranged that the HD is minimized.
Section II includes the related work-study. In section III GA for test vector generation is described. Power optimization by controlling toggling rate to its minimum value is described in section IV. Finally experimental work is described in section V and concluded in the last section.

II. RELATED WORK

F. Corno *et al.* [8] gives the GATTO algorithm for testing of combinational and sequential elements in the VLSI circuits, by following the general GA. Y. A. Skobtsov *et al* .[9] explains two ways of test pattern generation. One method is based on the classical genetic algorithm. Another way includes genetic programming, in which test patterns are represented as a micro operation sequence. In this, linear graph representation is used for the representation of patterns and their related operations that is cross over and mutation.

Michael S. Hsiao *et al.* [7] presented a spot optimization technique based on GA, for the estimation of peak power in large circuits. He presents the four ways for power determination in large circuits that are node-based, path-based, cone-based, and distance-based. K. Paramasivam *et al.* [2] [3] discussed the reordering of test vectors on the basis of graph theory for reordering algorithm to reduce the HD. Pinaki Mazumder *et al*. [6] in his book present the relation between the switching of transistors and power. It is mentioned that for the peak power determination for sequential circuits, their initialization is necessary. Buttitta B. *et al.* [10] discussed the way to use GA for effective channel routing in the complex VLSI circuits. Dhiraj K.Pradhan *et al.* [11] purposed a LFSR based on the minimum HD between the two consecutive test patterns to have shortest test length for test pattern generator with improved fault coverage.

Robbery Sanchez *et al.* [12] proposed techniques in which minimization of HD between the physical-chemical properties of ammonia acid is done. In the haze diagram minimum HD is preferred to have less change in the hydrophobic ties properties of protein. Usha S. Mehta *et al.* [13] emphasis on minimum HD, to have a better compression ratio for the test patterns for fast testing of the CUT. Process used follow the steps as, first of all doing MHD based reordering of test patterns, followed by column bit stiffing, and then difference of the vector followed by run length codes to improve the compression drastically.

III. GENETIC ALGORITHM FOR TEST VECTOR GENERATION

Some common terms used for GA are described briefly.
Chromosome: Genetic information is stored in the chromosome. In case of testing, chromosomes are in the form bits 1's and 0's.
Cross-over: It is the reproduction process in which two chromosomes are swapped to have two new offspring, which hire the good properties of parent chromosomes.
Mutation: Mutation is the process of producing incremental random changes in the offspring generated through the cross over.
Fitness function: It is the measure of the goodness of final result with respect to problem under consideration.

GA is used to generate the test vector which detects the faults in the circuit. But if generated test vectors cause in excess of switching in the CUT (circuit under test), then it becomes the reason for power dissipation. If the transistors in CUT face test vectors of toggling nature at continuous interval of time't' for testing purpose then switching rate is increased. To represent the fault detection and to minimize the power dissipation for test vectors of Gas, Turbo Tester v.3.0 is used for genetic test patterns generation. During this process in turbo tester, mutation rate is set to 0.10 for the population size up to 32 and if population size increased beyond 32 then mutation rate is 0.5. Maximum generation is set to value of 1000. The overall work flow is presented in the flow chart as shown in figure 1. After this, test patterns are simulated in the HD simulator designed in Visual Basic 6 to calculate HD of GA test vectors as shown in figure 2.

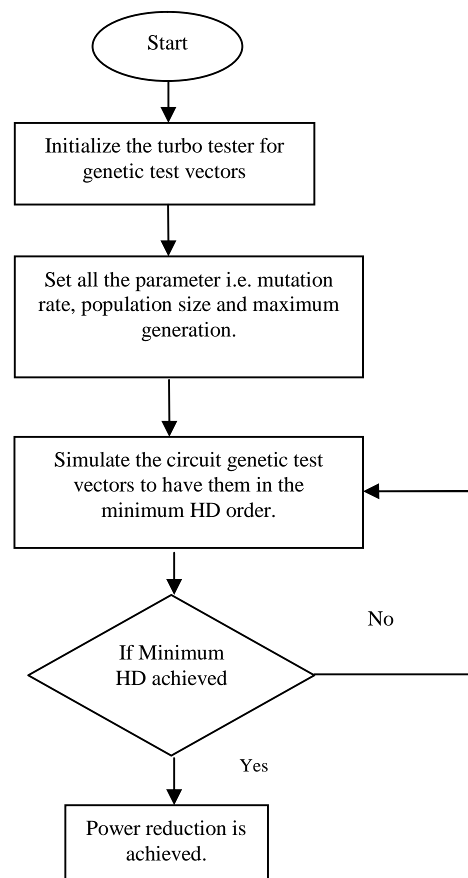

Figure 1: Flow chart of Power estimation Process

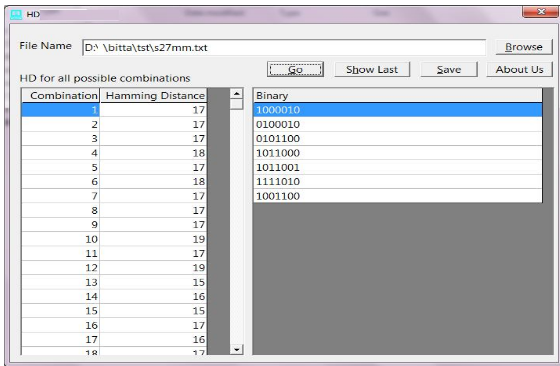

Figure 2: Simulator for rearranging the genetic test patterns in minimum HD

IV. RE-ARRANGING GENETIC TEST VECTORS FOR POWER OPTIMIZATION

To reduce switching rate, HD between the patterns is reduced. It is defined as the number of bits difference between two test vectors. Means, if HD is more, then the bits are more in distinct nature which causes the transistors to switch their state again and again. Whenever a new bit pattern is applied to check the state of the device, it forces the transistors to switch their state. The nodes with high output capacitance face charging and discharging at elevated rate, due to which it enters in meta stable state, which causes inaccuracy in results. The pseudo code for the calculation of HD is given below.

```
start
a=input('enter the population');
for i:= total number of rows in the population
set a counter which calculate total hamming distance
for i:=1 number first row of the population
if a(i)==a(i+1)
keep the older previous value counter
else
Increment counter by one
end
end
fprintf('the value of count %d\n', print the final value);
```

The calculated total HD is 26 for the test patterns generated for S27 benchmark circuit are shown in table 1. By following the mathematical relation between power and toggling of the gate value given in the equation 2, the TPD is 0.1664 nanowatts, for 160 pico-farad as total constant output capacitance of the circuit. Now, for reordering these patterns with minimum HD, the pseudo code is given below.

```
start
  {Call the "testfunc_HD" to calculate the Total HD}
    /* shown above*/;
 Function swapped_value=Main_swapper(input_ patterns)
{/* depending on the number of patterns, the number of timing occur varies. s*/}
/*swapping occur step by step after each swapping, new set of population is generated*/
{call the  "testfunc_HD" for each swapping;
   {stores the conter value for each swapping;
     {Compare counter value;
fprintf('the value of count  %d\n',print the minimum value);
        }; };
```

Overall steps to reduce the toggling activity or HD are given below:

(1)

Step 1: Generate the genetic test vector with turbo tester for a circuit with ‘p’ inputs and ‘q’ outputs through GA. Let’s suppose vector ‘n’ from GA.
Step 2: Calculate HD last generated test vectors, by the above designed function.
Step 3: Apply reordering to have patterns in the minimum HD form.
Step 4: Now apply this reorder patterns for fault simulation.

TABLE 1: GENETIC TEST PATTERNS BEFORE REARRANGING

S.No	Genetic test patterns before rearranging
1	1000010
2	1011000
3	0101100
4	1011001
5	0100010
6	1001100
7	1111010

TABLE 2: GENETIC TEST PATTERNS AFTER REARRANGING

S.No.	Genetic test patterns after rearranging
1	1000010
2	0100010
3	0101100
4	1001100
5	1011000
6	1011001
7	1111010

V. EXPERIMENTAL RESULTS

This section presents experimental results obtained by applying the proposed technique on ISCAS85 and ISCAS89 benchmark circuits. For this a power simulator is developed based on above mentioned techniques in Visual Basic as shown in figure 1. Firstly the CUT is simulated with Turbo Tester [14][15] to have Genetic algorithm based test patterns for maximum fault coverage and minimum number of possible patterns to test benchmark circuits. Fault coverage is plotted with respect to time as shown in figures 3 and 4 for combinational and sequential circuits respectively.

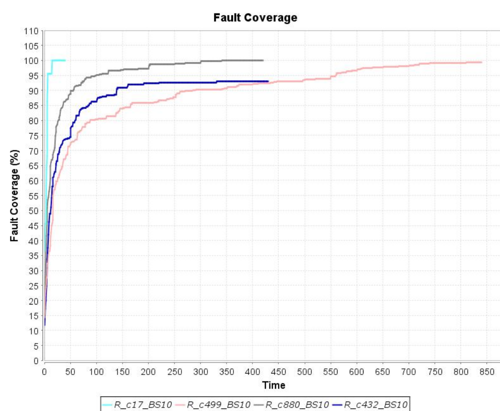

Figure 3: Results for combinational benchmark circuits

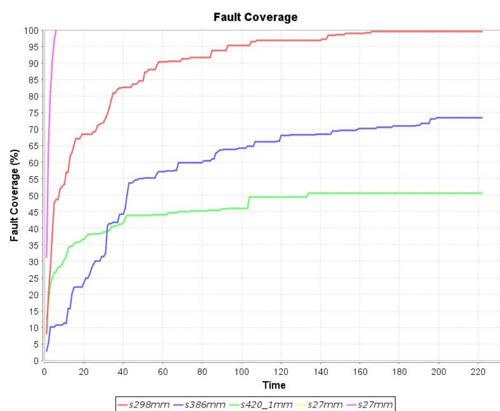

Figure 4: Fault coverage of sequential benchmark circuits

The possible combinations of re-arranged vectors are made and HD is calculated for each case. Also Total Power dissipated (TPD) is calculated with the developed power simulator. It saves the power during testing by choosing those arrangements of patterns which produce minimum HD. For example C17 benchmark circuit with output capacitance of 160 pico-farad requires minimum 4 patterns to achieve 100% fault coverage. There are 24 permutation or arrangements possible. In that set of permutation, 11 is the maximum value of Hamming distance and 7 is the minimum one. In respect to these HDs, TPD is 0.0352 nano-watts and 0.0224 nano-watts for 11(maximum) and 7 (minimum) HD respectively. In this way by choosing the pattern arrangement with minimum HD, the power dissipation is reduced up to 36% during testing. Table 3 and Table 4 list results of the suggested approach for ISCAS85 and ISCAS89 benchmark circuits.

VI. CONCLUSION

The power is optimized for VLSI circuit testing by applying the genetic algorithm in conjunction with the method of reducing hamming distance of the genetic test patterns. Algorithm arranges test patterns generated with GA to have minimum switching rate of the CUT. Experimental results of the proposed method shows benefits of power saving with re-arrangement of the test patterns. Results prove that maximum power dissipation is reduced by the average of 31% in case of combinational and 36 % sequential circuits.

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Table 3: Experimental results for Power Reduction Combinational Logic Benchmark Circuits

Results of Combinational Logic Circuits													
Bench mark circuits Characteristics				**Fault coverage and time**					**Power Dissipations(nW)**				
	No. of PI	No. of PO	No. of Gates	faults	Tested	%	Vector	time	In original Test Vectors		Proposed Method		%
									Hd	Power	Hd	Power	Saving
C17	5	2	6	22	22	100	4	0.001	11	0.0352	7	0.0224	36
C432	36	7	160	616	573	93.012	53	0.203	777	8.703	553	6.194	28
C499	41	32	202	1202	1194	99.335	85	0.328	1356	69.428	896	45.876	34
C880	60	26	383	994	994	100.00	994	0.328	1339	55.703	986	41.018	26
									Average	33.467		23.277	31

Table 4: Experimental Results for Power Reduction Sequential Logic Benchmark Circuits

Results of Sequential logic circuits														
Bench mark circuits Characteristics					**Fault coverage and time**					**Power Dissipations(nW)**				
	No. of PI	No. of PO	No. of Gates	No of FFs	faults	Tested	%	Vector	time	In original Test Vectors		Proposed Method		%
										Hd	Power	Hd	Power	Saving
S27	4	1	10	3	32	32	100	7	0.001	26	0.1664	14	0.0896	46
S298	3	6	119	14	358	358	100	34	0.109	241	7.712	172	5.5040	28
S420	18	1	218	16	480	467	97.29	66	0.171	1367	30.348	962	21.356	30
S386	7	7	159	6	454	454	100	75	0.109	392	8.153	241	5.0128	39
									Average	11.599		7.99	36	