AN EFFICIENT APPROACH TO MINIMIZE POWER AND AREA IN CARRY SELECT ADDER USING BINARY TO EXCESS ONE CONVERTER

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Abstract: Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for reducing the area and power consumption in the CSLA. This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 8, 16, 32, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in 0.18- nm CMOS process technology. The results analysis shows that the proposed CSLA structure is better than the regular SQRT CSLA. A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16, 32, and 64-b sizes which indicates the success of the method and not a mere trade-off of delay for power and area.

Keywords*: Application-Specific Integrated Circuit (ASIC), area-efficient, CSLA, low power.*

I. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1 then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with C in=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively. The ASIC implementation details and results are analyzed in Section VI. Finally, the work is concluded in Section VII.

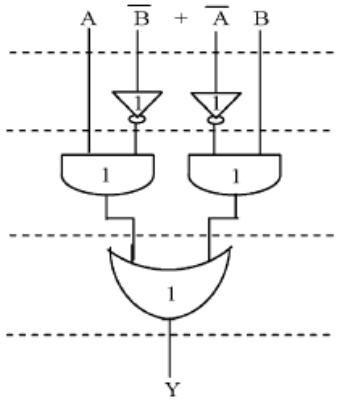

Figure1. Delay and Area evaluation of an XOR gate.

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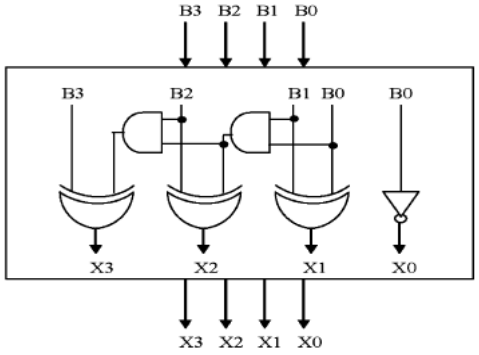


Figure 2. 4-b Binary To Excess One Converter (BEC).

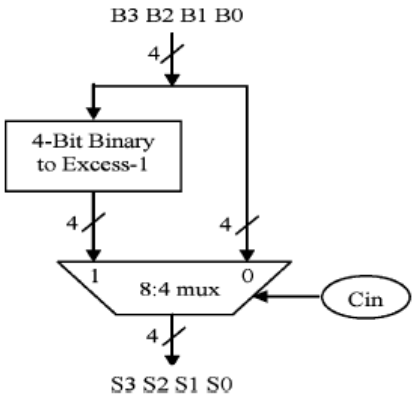


Figure. 3. 4-b BEC with 8:4 mux.

II. DELAY AND AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Figure. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

TABLE I
DELAY AND AREA COUNT OF THE BASIC BLOCKS OF CSLA

Address Blocks	Delay	Area
X-OR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

TABLE II
FUNCTION TABLE OF THE 4-b BEC

B(3:0)	X(3:0)
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

III. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with C in=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Figure 2 and Table II, respectively. Figure 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~NOT, & AND, ^XOR)

X0 = ~ B0
X1 = B0 ^ B1
X2 = B2^(B0 & B1)
X3 = B3^(B0 & B1 & B2)

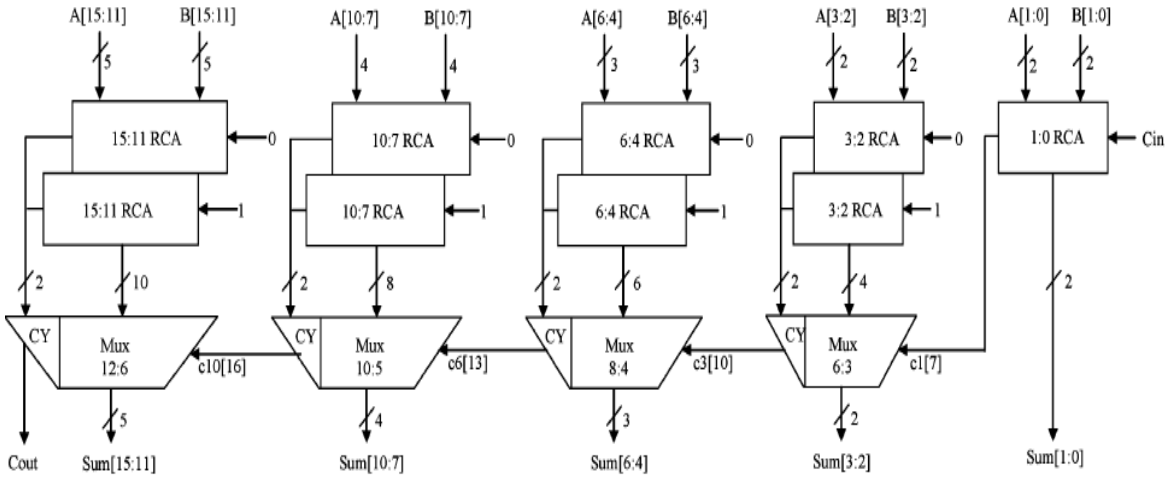


Figure. 4. Regular 16-b SQRT CSLA.

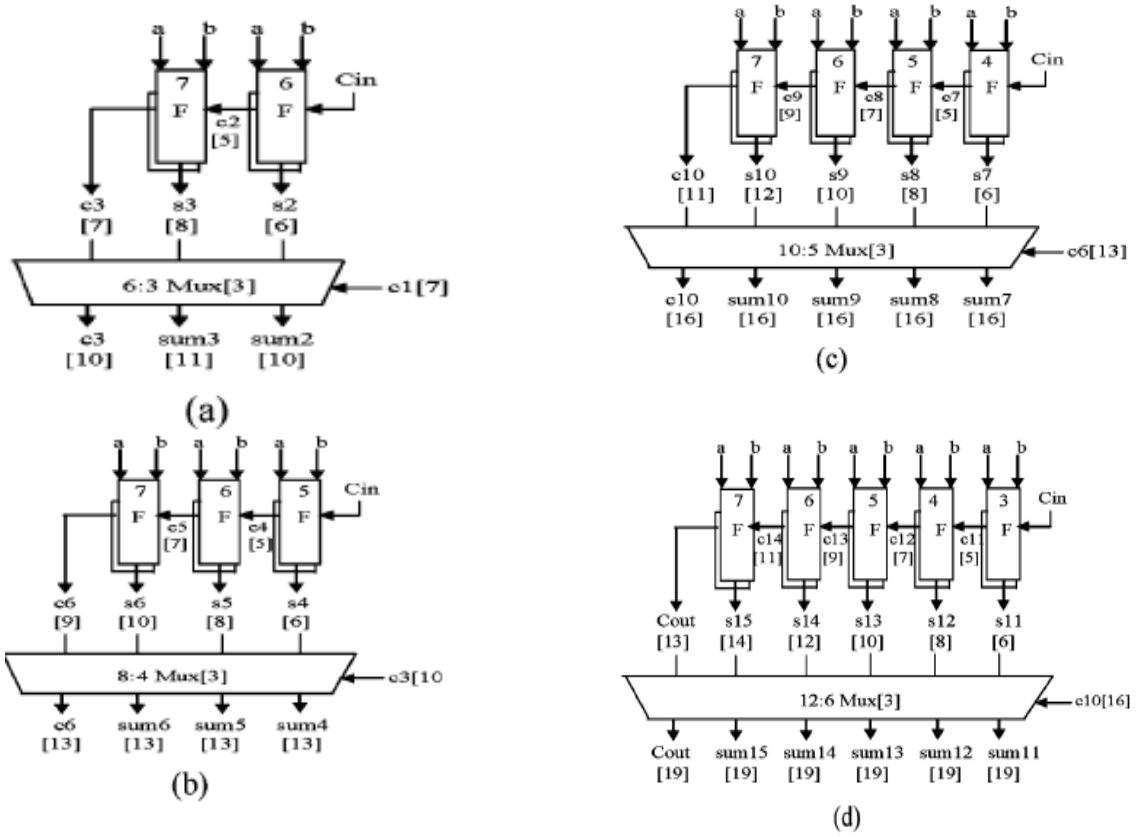


Figure. 5. Delay and area evaluation of regular SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. F is a Full Adder.

IV. DELAY AND AREA EVALUATION METHODOLOGY OF REGULAR 16-B SQRT CSLA

The structure of the 16-b regular SQRT CSLA is shown in Figure 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Figure.5, in which the numerals within [ ] specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

1) The group2 [see Figure 5(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input C1 [time (t) = 7] of 6:3 mux is earlier than s3[t=8] and later than s2[t=6].

Thus,sum3[t=11] is summation of s3 and mux[t=3] and sum2[t=10] is summation of c1and mux.

2) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

{c6,sum[6:4]}=c3[t=10]+mux
{c10,sum[10:7]}=c6[t=13]+mux
{cout,sum[15:11]}=c10[t=16]+mux

3) The one set of 2-b RCA in group2 has 2 FA for Cin=1 and thevother set has 1 FA and 1 HA for Cin=1. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

Gate count =57(FA+HA+Mux)
FA=39(3*13)
HA=6(1*6)
Mux=12(3*4)

4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table III.

HA=6(1*6)
AND=1
NOT=1
XOR=10(2*5)
Mux=12(3*4).

TABLE III
DELAY AND AREA COUNT OF REGULAR SQRT CSLA GROUPS

Group	Delay	Area
Group 2	11	57
Group 3	13	87
Group 4	16	117
Group 5	19	147

V. DELAY AND AREA EVALUATION METHODOLOGY OF MODIFIED 16-B SQRT CSLA

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Figure 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Figure 7. The steps leading to the evaluation are given here.

1) The group2 [see Figure 7(a)] has one 2-b RCA which has 1 FA and 1 HA for Cin-0. Instead of another 2-b RCA with Cin=1 a 3-b BEC is used which adds one to the output from 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input c1 [time (t) =7] of 6:3 mux is earlier than the s3[t=9] and c3[t=10] and later than the s2[t=4]. Thus, the sum3 and final c3(output from mux) are depending on s3 and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.

2) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

3) The area count of group2 is determined as follows:

Gate count=43(FA+HA+Mux+BEC)
FA=13(1*13)

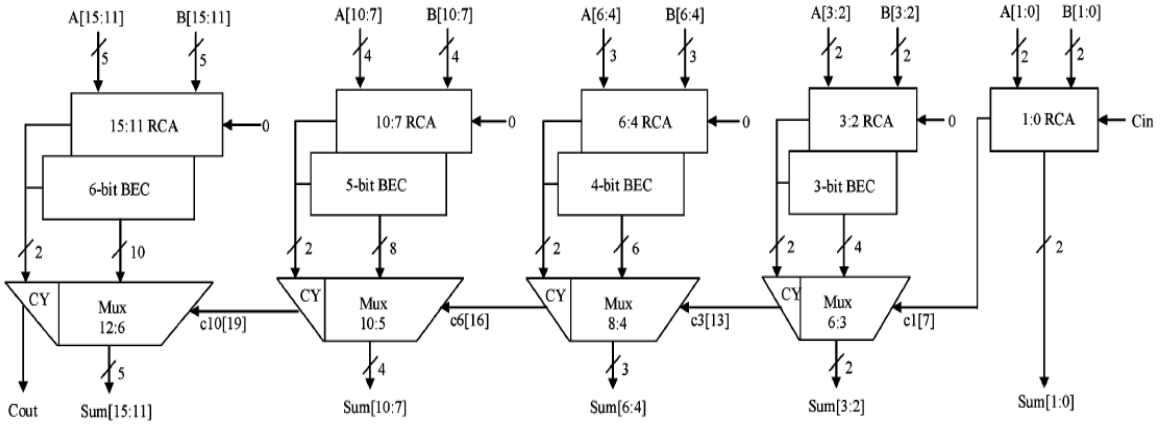
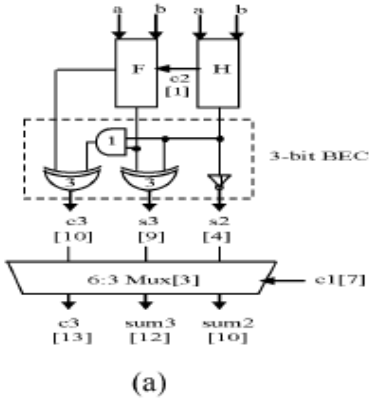
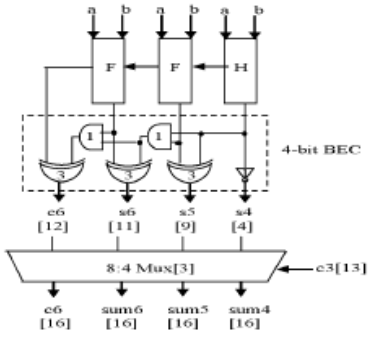


Figure. 6. Modified 16-b SQRT CSLA. The parallel RCA with Cin=1 is replaced with BEC.

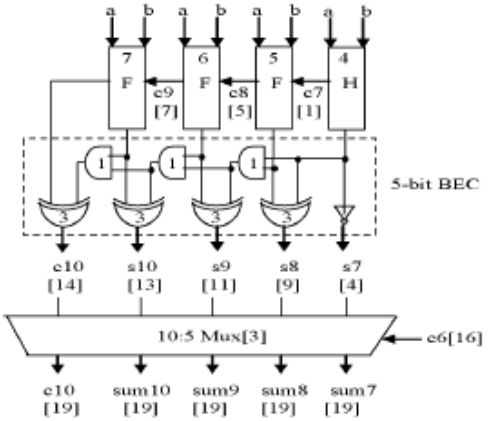
4) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.



(a)



(b)



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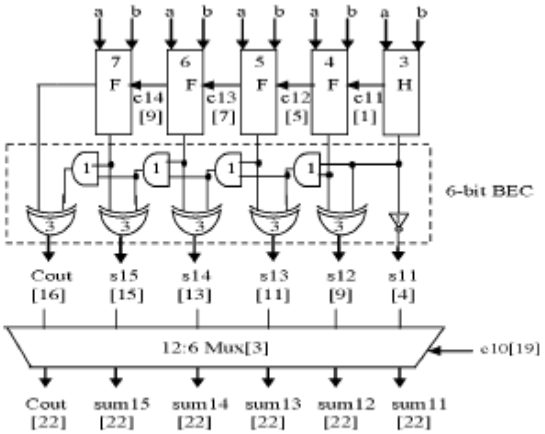

(d)

Figure 7. Delay and area evaluation of modified SQRT CSLA: (a) group2, (b) group3, (c) group4, and (d) group5. H is a Half Adder.

TABLE IV
DELAY AND AREA COUNT OF MODIFIED SQRT CSLA

Group	Delay	Area
Group2	13	43
Group3	16	61
Group4	19	84
Group5	22	107

Comparing Tables III and IV, it is clear that the proposed modified SQRT CSLA saves 113 gate areas than the regular SQRT CSLA, with only 11 increases in gate delays. To further evaluate the performance, we have resorted to ASIC implementation and simulation.

VI. ASIC IMPLEMENTATION RESULTS

The design proposed in this paper has been developed using Verilog- HDL and synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology. The synthesized Verilog netlist and their respective design constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing [7]. Parasitic extraction is performed using Encounter's Native *RC*

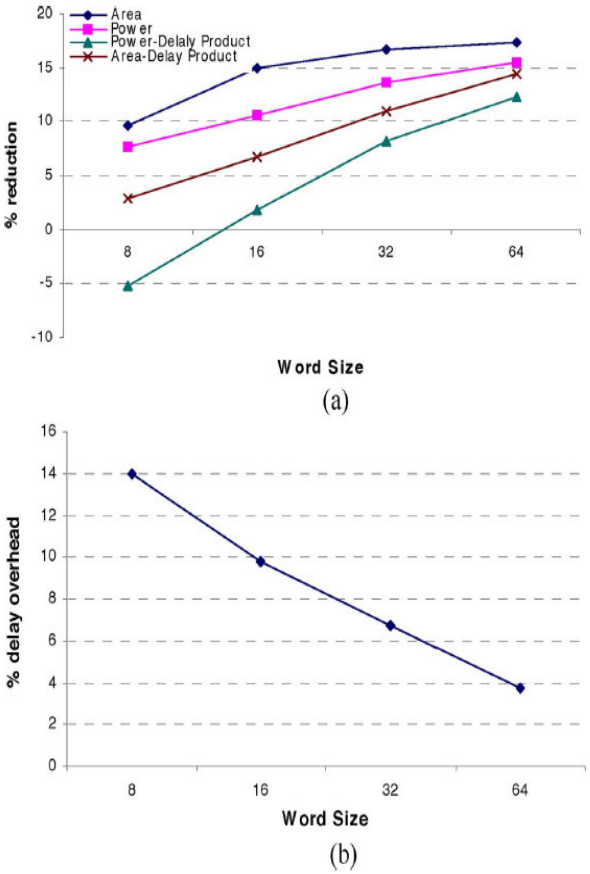

Figure. 8. (a) Percentage reduction in the cell area, total power, power–delay product, and area–delay product. (b) Percentage of delay overhead.

extraction tool and the extracted parasitic *RC* (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis. For each word size of the adder, the same value changed dump (VCD) file is generated for all possible input conditions and imported the same to Cadence Encounter Power Analysis to perform the power simulations. The similar design flow is followed for both the regular and modified SQRT CSLA.

Table V exhibits the simulation results of both the CSLA structures in terms of delay, area and power. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power. The percentage reduction in the cell area, total power, power-delay product and the area–delay product as function of the bit size are shown in Figure 8(a). Also plotted is the percentage delay overhead in Figure 8(b). It is clear that the area of the 8-, 16-, 32-, and 64-b proposed SQRT CSLA is reduced by 9.7%, 15%, 16.7%, and 17.4%, respectively.

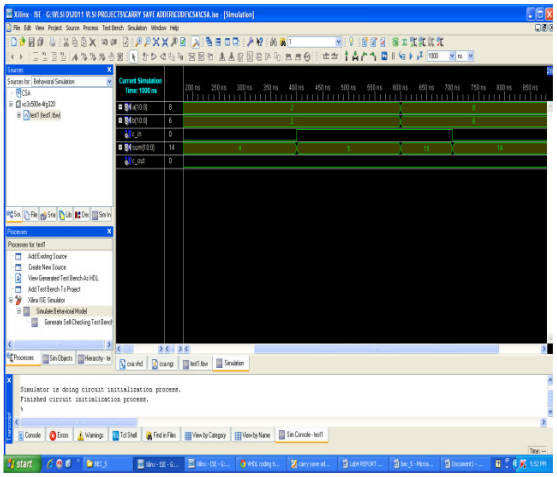

Figure.9. Simulation output

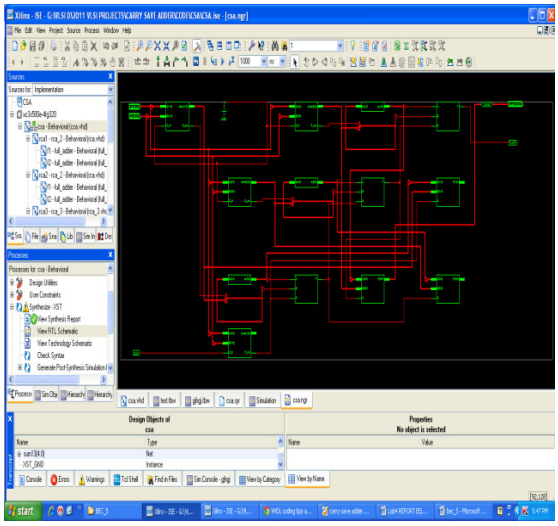

Figure.10. Schematic output

The total power consumed shows a similar trend of increasing reduction in power consumption 7.6%, 10.56%, 13.63%, and 15.46 % with the bit size. Interestingly, the delay overhead also exhibits a similarly decreasing trend with bit size. The delay overhead for the 8, 16, and 32-b is 14%, 9.8%, and 6.7% respectively, whereas for the 64-b it reduces to only 3.76%. The power–delay product of the proposed 8-b is higher than that of the regular SQRT CSLA by 5.2% and the area-delay product is lower by 2.9%. However, the power-delay product of the proposed 16-b SQRT CSLA reduces by 1.76% and for the 32-b and 64-b by as much as 8.18%, and 12.28% respectively. Similarly the area-delay product of the proposed design for 16-, 32-, and 64-b is also reduced by 6.7%, 11%, and 14.4% respectively

VII. SYNTHESIS REPORT

Clock Information: No clock signals found in this design
Asynchronous Control Signals Information: No asynchronous control signals found in this design
Timing Summary: Speed Grade: -5
Minimum period: No path found Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 11.231ns
Timing Detail:
All values displayed in nanoseconds (ns)
Timing constraint: Default path analysis
Total number of paths / destination ports: 291 / 19
Delay: 11.231ns (Levels of Logic = 12)
Total 11.231ns (8.136ns logic, 3.095ns route) 72.4% logic, 27.6% route)
CPU : 5.91 / 6.44 s | Elapsed : 6.00 / 7.00 s
Total memory usage is 153980 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings: 12 (0 filtered)
Number of infos : 2 (0 filtered)

VIII. RESULT

In the process the schematic of both the existing one and the proposed 16 bit square root carry select adder has been designed by using transistors. A simulation environment realistic to the actual circuit operational conditions has been set up, where the cells has both driving and driven circuit. The input buffers before they are fed into 16 bit CSLA circuit and the outputs are also loaded to the buffer after they are exported. All the circuits are simulated using TSPICE based on the Tanner tool. For each simulation TSPICE will generate an average power consumption value. Comparison of the regular and modified square root carry select adder in terms of power dissipation is listed in the Table.

Word size	16bit	
Adder	Regular CSLA	Modified CSLA
Delay (ns)	2.77	3.04
No of transistor	3086	2558
Leakage power	0.13117	0.0217
Switching power	104.6	0.5299
Total power	3.16	0.1448

Word size	16bit	
Adder	Regular CSLA	Modified CSLA
Delay (ns)	2.77	3.04
No of transistor	3086	2558
Leakage power	0.13117	0.0217
Switching power	104.6	0.5299
Total power	3.16	0.1448

VIII. CONCLUSION

A simple approach is proposed in this paper to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere trade-off of delay for power and area. The modified CSLA architecture is therefore, low area, low Power, simple and efficient for VLSI hardware implementation. It would be interesting to test the design of the modified 128-b SQRT CSLA.

FUTURE SCOPE

In this CSLA we have proposed large no of bits. And same wise we are going to increase again the more number of bits to be added. With RCA we cannot achieve the highest target of reaching the most number of bits to increase. For e.g., if we are transmitting the 32 bits of the RCA values and BEC means we need to do more than the number of bits. Same way not only increasing the bitrate but also the area of the architecture, power and also the efficiency of the designed circuits. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The design proposed in this paper has been developed using Verilog- HDL and synthesized in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology. The synthesized Verilog net list and their respective design constraints file (SDC) are imported to Cadence SoC Encounter and are used to generate automated layout from standard cells and placement and routing. Parasitic extraction is performed using Encounter's Native RC extraction tool and the extracted parasitic RC (SPEF format) is back annotated to Common Timing Engine in Encounter platform for static timing analysis. For each word size of the adder, the same value changed dump (VCD) file is generated for all possible input conditions and imported the same to Cadence Encounter Power Analysis to perform the power simulations. The similar design flow is followed for both the regular and modified SQRT CSLA. The area indicates the total cell area of the design and the total power is sum of the leakage power, internal power and switching power.

TABLE V
COMPARISON OF THE REGULAR AND MODIFIED SQRT CSLA

Word size	Adder	Delay (ns)	Area ($um^{2)}$	Power (uw)			Power-Delay Product (10^{-15})	Area-Delay Product (10^{-15})
				Leakage Power	Power Switching	Total Power		
8-bits	Regular CSLA	1.719	991	0.007	101.9	203.9	350.5	1703.5
	Modified CSLA	1.958	895	0.006	94.2	188.4	368.8	1752.4
16-bits	Regular CSLA	2.775	2272	0.017	263.7	527.5	1463.8	6304.8
	Modified CSLA	3.048	1929	0.013	235.9	471.8	1438.0	5879.6
32-bits	Regular CSLA	5.317	4783	0.036	563.6	1127.3	5790.9	24570.2
	Modified CSLA	5.482	3985	0.027	484.9	969.9	5316.9	21845.7
64-bits	Regular CSLA	9.174	9916	0.075	1212.4	2425.0	22246.9	90969.3
	Modified CSLA	9.519	8183	0.057	1025.0	2050.1	19514.9	77893.9

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