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SLIDING MODE CONTROL OF BUCK CONVERTERS FOR IMPROVED TRANSIENT RESPONSE

Cristian ORIAN, Dorin PETREUŞ, Radu ETZ
Technical University of Cluj-Napoca, Cluj-Napoca, Romania
26-28 G. Baritiu Street, 400027 Phone +40264202348, Email: cristian.orian@ael.utcluj.ro

Abstract: The following paper describes a method to design a sliding mode (SM) controller for a dc-dc converter. It focuses on producing an aperiodic response and a controlled settling time. The method can be used for a given set of disturbances, and thus lends itself to subsequent worst case or weighted convex optimization solutions. The impact of an analog to digital converter is presented. Additionally, the restriction of the switching frequency, a challenge particular to sliding mode control (SMC), is discussed. The work comprises Mathcad modeling, Psim simulation and experimental results. The control block was implemented on an Artix 7 FPGA.

Keywords: *sliding mode control, aperiodic response, time costant, dc-dc buck converter, nonlinear control.*

I. INTRODUCTION

Switched-mode power supplies are widespread circuits used in household items, office equipment, communication equipment etc. They are also used to extract power from distributed energy resources in microgrids. The control requirements of such systems are increasing in complexity, which is why it is necessary to identify all issues which hinder performance and to try to alleviate them. The importance of control loops and system dynamics is presented in [1].

The transition from analog to digital control presents both advantages and disadvantages. On the one hand, the control may be slower, which means longer settling times. Additionally, the sampling and processing delays may impact the quality of the transient response. On the other hand, digital control is impervious to ageing effects and external factors such as temperature or capacitor bias voltage, both of which influence the performance of analog control circuits. They also allow simple control law reconfiguration, communication facilities, autocalibration and debugging. The drawbacks are gradually eliminated by semiconductor manufacturers.

The most commonly used solution for designing the control of a dc-dc converter is the PID regulator [2], [3]. It is very well documented, but it is not robust [4]. This is why phase margins must be allowed. Even so, the variance of any of the system's parameters impacts the quality of the transient response. The PID coefficients can be determined by using tuning methods [5], [6]. They can also be determined as described in [7]. Additionally, self-tuning PID controllers have been presented in [8]. There is also the integrator plus dead time model, which is correlated to Ziegler-Nichols as in [9]. The PID algorithm can provide a solution for the step-down converter, but it may create problems for higher order systems by degrading transient response parameters such as overshoot and settling time, or it can even lead to oscillations [10].

Sliding mode (SM) is a method used for robust control. Sliding mode control (SMC) design guidelines are presented in [11]. The main idea is to drive the system towards steady state every time there is a disturbance by restricting the evolution of the state variables to follow the projections of a control manifold in the state space. This control manifold is defined during design and it must intersect one point corresponding to steady state, irrespective of the operating conditions. If the natural state variables do not allow the existence of such a point, then a new set of state variables must be defined to meet this requirement. This paper handles such a situation.

There are several variations which stem from the SMC. Among them, the double integral sliding manifold increases the number of state variables, but decreases the output steady state error [12]. Nonlinear sliding control laws can be defined, such as terminal sliding mode control (TSMC) [13] and adaptive terminal sliding mode control (ASMC) in [14]. The claim is that they can influence transient response parameters, but rely on accurate sensing just like the conventional linear SMC.

The advantages of SMC render it suitable for a large range of applications. Among them, the control of dc-dc converters [15]–[17], actuated systems [18], industrial gas turbines [19], road vehicles [20].

This paper presents the design of a SM controller for a step down converter. The state space model of the converter and the theory of the SMC are briefly introduced. Subsequently, the desired transient response is defined qualitatively. An aperiodic response is the target. A method is proposed to meet this objective. Additionally, the duration of the transient response is determined as a result of the convenient polynomial approximation of exponential and trigonometric functions. The time constant, which corresponds to an exponential decay produced by the sliding phase, is expressed separately. After that, a possible solution for restricting the minimum and maximum values of the

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switching frequency is proposed. The control law is designed for a damped transient response and the settling time is calculated. In order to reduce component count, one voltage is sensed and an observer is employed. The effect of the sampling rate on the desired transient response is presented. Experimental results are provided.

The paper is organized as follows: section 0 presents the step-down converter, the SMC, defines the desired outcome and the design considerations; section 0 presents the Mathcad model and the Psim simulation results; section 0 presents a simulation augmented by the ADC delays and the experimental results; section 0 presents the conclusions of the work.

II. CONTROL METHOD AND DESIGN

II. 1 The model of the step-down converter

The step-down converter is a topology of a switched mode power supply which is used to maintain an output voltage lower than that at its input. The circuit does not use galvanic isolation. The schematic of a synchronous buck converter is presented in Figure 1. There are two switching devices *M1* and *M2* which control the power flow through the circuit, hence the name switched power supply. The command signals for *M1* and *M2* are complementary, thus averting the risk of a short circuit. The inductor *L* and the capacitor *C* successively store energy and release it to the load. Resistances R_L and the Equivalent Series Resistance (*ESR)* of the capacitor are parasitic components.

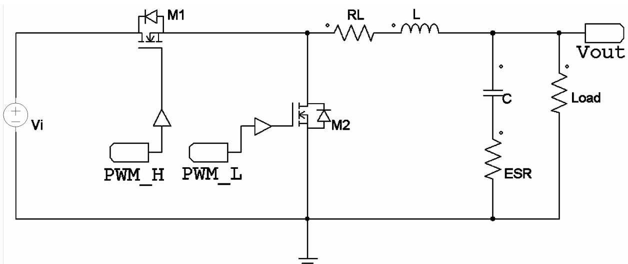

Figure 1. Schematic of a step-down converter.

The model of the converter is delivered by simply applying Kirchhoff's laws. It takes the form of a pair of coupled first order linear differential equations, as in (1)

$$\begin{cases} \dot{u}_C = -\dfrac{1}{C}\cdot\dfrac{1}{ESR+R}\cdot u_C + \dfrac{1}{C}\cdot\dfrac{R}{ESR+R}\cdot i_L \\ \dot{i}_L = -\dfrac{1}{L}\cdot\left(\dfrac{ESR\cdot R}{ESR+R}+R_L\right)\cdot i_L - \dfrac{1}{L}\cdot\dfrac{R}{ESR+R}\cdot u_C + \dfrac{1}{L}\cdot u_i \end{cases}, \qquad (1)$$

where u_i is a function taking values 0V when *M1* is OFF and V_I when *M1* is ON as in (2), *R* is the resistance of the load and u_c is the capacitance voltage and does not include the drop across the *ESR*. The state variables are the inductance current and the capacitance voltage. The model of the buck converter is required for feedback loop considerations. It allows for the removal of the nonlinear switching devices, provided that the ripple components of the inductor current and output capacitance voltage are neglected and that the voltage at the drain of *M2* is considered rectangular, namely the output voltage value does not change at all during a switching period. Also, continuous conduction mode is assumed.

$$u_i = \begin{cases} V_I, & if \text{ M1 is ON.} \\ 0V, & if \text{ M1 is OFF} \end{cases} \qquad (2)$$

II. 2 SMC for a second order system

The SMC is a nonlinear control method applicable to variable structure systems (VSS). It is suitable for power supplies even though the model presented previously is linear. That is because switching power converters are VSS. The method ensures the stability and robustness of the system. In fact, it is an approach to robust control.

The design of the SM controller starts with the identification of the state variables and the description of the plant. Assuming a second order system, the plant can be described as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\cdot\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}\cdot r, \qquad (3)$$

where $[x_1, x_2]^T$ is the state variable column vector, *r* is the applied time varying input and the coefficients a_{ij} and b_i are determined according to the physical properties of the system. The solution describing the evolution of the system depends upon the values taken by the input *r*. The control law can be given as

$$x_2 - \alpha\cdot x_1 = 0 \qquad (4)$$

This is a linear function on the phase plane and the equilibrium point is normally taken at the origin. The function does not overlap with the natural evolution of the system for a given constant input *r*, but it steers the state variables towards their steady state values via the high frequency switching of the input. In theory, the high frequency tends to infinity. In practice, its maximum value will be restricted in order to limit the switching losses.

The state variables must be selected in such a way that their zero values eliminate steady state error regardless of the operating point of the system. The equilibrium point will thus be at the origin of the phase plane. The selection of the appropriate state variables for a buck converter is detailed in the next section.

The values of the state variables are forced along the line given by the control law (4) towards equilibrium for any given transients. However, it is conceivable that the system evolution starting from certain initial values does not land on this line. This means that the control law must be defined in such a way that regardless of the disturbance, the system will evolve toward the sliding function defined in (4). This is called the hitting condition and it translates to

$$(x_2 - \alpha\cdot x_1)\left(\dot{x}_2 - \alpha\cdot\dot{x}_1\right) < 0 \qquad (5)$$

Equations (3) and (5) lead to

$$\dot{x}_2 - \alpha\cdot\dot{x}_1 = a_{21}\cdot x_1 + a_{22}\cdot x_2 + b_2\cdot r - \alpha\cdot(a_{11}\cdot x_1 - a_{12}\cdot x_2 - b_1\cdot r), \qquad (6)$$

for any fixed value of input *r* within its allowed set.

II. 3 Conveniently defined state variables

The model description of the Buck circuit given in (1) defines the inductance current and capacitance voltage as state variables. This is the usual choice for state variables. However, it is not advantageous for the purposes of the SM control law previously defined. The reason is the fact that the origin of such a phase plane would not correspond to the equilibrium point. In fact, the equilibrium would correspond to an entire line segment whose capacitance voltage coordinate would be fixed at the nominal value and inductance current coordinate would vary as a function of the load. Defining the control law in such a situation would require information about the load in order to select the appropriate inductance current coordinate.

An alternative state variables set comprises the capacitor current i_c and the capacitance voltage error e_o. Indeed, the average capacitor current is null during equilibrium regardless of the load and it reflects the average inductance current error during transient states. Additionally, the capacitance voltage error is null during equilibrium regardless of the nominal output voltage. The latter can be determined if a reference voltage V_{ref} is provided. Therefore, the SM control law given in (4) is adequate for the new state variables and the origin of this phase plane is the equilibrium point, regardless of the system's operating conditions. The substitution is possible using (7). The results are given in (8), with (9) and (10) detailing some of the terms in (8). The term β accounts for the attenuation produced by the resistive divider in the feedback loop.

$$\begin{cases} i_L = \dfrac{u_C}{R} + \dfrac{ESR+R}{R}\cdot i_C \\ u_C = -\dfrac{1}{\beta}\cdot e_o - ESR\cdot i_C + \dfrac{V_{ref}}{\beta} \end{cases} \tag{7}$$

$$\begin{bmatrix} \dot{e}_o \\ \dot{i}_C \end{bmatrix} = \begin{cases} \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\cdot\begin{bmatrix} e_o \\ i_C \end{bmatrix} + \begin{bmatrix} e_{fON} \\ i_{fON} \end{bmatrix}, & if \text{ M1 is ON.} \\ \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\cdot\begin{bmatrix} e_o \\ i_C \end{bmatrix} + \begin{bmatrix} e_{fOFF} \\ i_{fOFF} \end{bmatrix}, & if \text{ M1 is OFF.} \end{cases} \tag{8}$$

$$\begin{cases} a_{11} = -\dfrac{ESR}{L}\cdot\dfrac{R+R_L}{ESR+R} \\ a_{12} = \beta\cdot ESR\cdot\left(\dfrac{R\cdot R_L + \dfrac{L}{C}}{L\cdot(ESR+R)} - \dfrac{1}{ESR\cdot C}\right) \\ a_{21} = \dfrac{1}{\beta L}\cdot\dfrac{R+R_L}{ESR+R} \\ a_{22} = -\dfrac{1}{L\cdot(ESR+R)}\cdot\left(R\cdot R_L + \dfrac{L}{C}\right) \end{cases} \tag{9}$$

$$\begin{cases} e_{fON} = -\beta\cdot ESR\cdot\left(\dfrac{R}{ESR+R}\cdot\dfrac{V_i}{L} - \dfrac{R+R_L}{ESR+R}\cdot\dfrac{V_{ref}}{\beta L}\right) \\ i_{fON} = -\dfrac{1}{\beta L}\cdot\dfrac{R+R_L}{ESR+R}\cdot V_{ref} \\ e_{fOFF} = ESR\cdot\dfrac{R+R_L}{ESR+R}\cdot\dfrac{V_{ref}}{L} \\ i_{fOFF} = -\dfrac{1}{\beta L}\cdot\dfrac{R+R_L}{ESR+R}\cdot V_{ref} \end{cases} \tag{10}$$

Equation (8) describes the continuous conduction mode converter as a pair of first order autonomous systems. It is possible to express the solution for each provided that the initial values of the two state variables are known. The control circuit will generate the switching command such that the state variables reach the equilibrium point.

II. 4 The qualitative description of the desired transient response

The control law (4) must be selected in such a way that the steady state and transient state performances of the overall system comply with the specified requirements. It does not influence the steady state behavior of the system, because of the way it is designed to cancel the average value of the output voltage error. The general form for the control law was given in (4), though after the change in state variables (7), it becomes

$$\alpha\cdot e_o - \frac{\beta}{C}\cdot i_c = 0. \tag{11}$$

The one parameter which can be modified in the design of the control law given in (11) is α. Its value must be positive.

$$\alpha > 0 \tag{12}$$

This restriction places the graph of the control law in the first and third quadrant of the phase plane, which is in accord with the physical behavior of the system and the natural variation of the output voltage error and inductor current error in case a disturbance is present. Indeed, a decrease in load current leads to an increase in output capacitor voltage, which according to (7) means a negative voltage error (state variable). In order to handle this disturbance, a negative capacitor current must be enforced. Therefore, the system will evolve freely until it reaches the control law in the third quadrant of the phase plane. From there on, the sliding phase will force the system into its new steady state. A load increase is handled similarly, but in the first quadrant of the phase plane.

The transient response parameters such as settling time and overshoot vary as a function of the value of *α*. In fact, the entire shape of the transient response depends on it. This is because of the various ways in which the system trajectory can evolve before it reaches the sliding phase.
The time domain feature of the sliding phase is that both state variables vary towards their steady state values exponentially. This can be easily verified by substituting (7) into (11). The time interval for this phase depends on the time constant, which is

$$\tau = C\cdot\left(\frac{1}{\alpha C} + ESR\right). \tag{13}$$

Clearly, it is preferable to have the time constant as low as possible, which means increasing α as much as possible.

There is, however, a restriction on the increase of α. Prior to reaching the sliding phase, the system must intersect the control line in a region where condition (5) is met. However, it is possible that the first intersection – or the first several intersections – occur outside that region. This will lead to more cycles on the phase portrait, as presented in Figure 2b. In the time domain it translates to long ON/OFF pulses, which can lead to high currents through the inductor and even its saturation. However, the settling time will not necessarily be longer than in a case where the sliding phase occurs on the first intersection. Figure 2a presents an aperiodic transient response. The two situations presented in Fig. 2a and Fig. 2b feature the same dc-dc converter, the same initial conditions for the state variables, but different values for α.

II. 5 Design of the SM controller

The method described for the selection of α is oriented towards transient response performances. That is because regardless of this parameter, the steady state values of the output voltage error and inductor current error, respectively, will always go to zero. The transient phase will comprise the reaching phase designed to end at the first intersection with the control law characteristic, as in Figure 2a, and a sliding phase towards zero error, which will correspond to an exponential error decay in time. The time constant of the sliding phase is given in (13). The advantages of such a transient response are the elimination of high current values through the inductor, ensuring that it operates away from its saturation limit and the elimination of output voltage spikes. Starting from (5) and (11), we get (14)

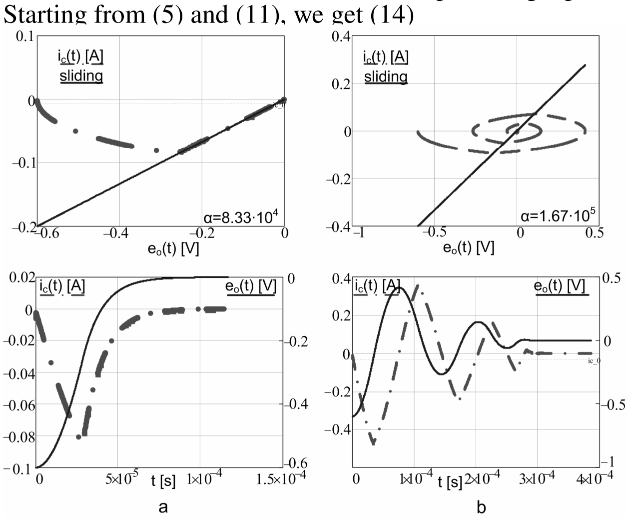

Figure 2. ***a****: phase plane and transient response for α = 8.33·10^4;* ***b****: phase plane and transient response for α = 1.67·10^5.*

$$\begin{cases}\alpha\cdot\dot{e}_o-\dfrac{\beta}{C}\dot{i}_C<0,\ \alpha\cdot e_o-\dfrac{\beta}{C}i_C>0\\ \alpha\cdot\dot{e}_o-\dfrac{\beta}{C}\dot{i}_C>0,\ \alpha\cdot e_o-\dfrac{\beta}{C}i_C<0\end{cases}. \qquad (14)$$

Substituting (8) into (14) yields the two conditions

$$\begin{cases}\left(\alpha\cdot a_{11}-\dfrac{\beta}{C}\cdot a_{21}\right)\cdot e_o+\left(\alpha\cdot a_{12}-\dfrac{\beta}{C}\cdot a_{22}\right)\cdot i_c+\alpha\cdot e_{fOFF}-\dfrac{\beta}{C}\cdot i_{fOFF}<0\\ \alpha\cdot e_o-\dfrac{\beta}{C}i_C>0\\ \left(\alpha\cdot a_{11}-\dfrac{\beta}{C}\cdot a_{21}\right)\cdot e_o+\left(\alpha\cdot a_{12}-\dfrac{\beta}{C}\cdot a_{22}\right)\cdot i_c+\alpha\cdot e_{fON}-\dfrac{\beta}{C}\cdot i_{fON}>0\\ \alpha\cdot e_o-\dfrac{\beta}{C}i_C<0\end{cases}. \qquad (15)$$

There is one linear equation and two affine equations which can be defined based upon the four inequations in (15):

$$\begin{cases}(s):\alpha\cdot e_o-\dfrac{\beta}{C}i_C=0\\ (d_1):\left(\alpha\cdot a_{11}-\dfrac{\beta}{C}\cdot a_{21}\right)\cdot e_o+\left(\alpha\cdot a_{12}-\dfrac{\beta}{C}\cdot a_{22}\right)\cdot i_c+\alpha\cdot e_{fOFF}-\dfrac{\beta}{C}\cdot i_{fOFF}=0\\ (d_2):\left(\alpha\cdot a_{11}-\dfrac{\beta}{C}\cdot a_{21}\right)\cdot e_o+\left(\alpha\cdot a_{12}-\dfrac{\beta}{C}\cdot a_{22}\right)\cdot i_c+\alpha\cdot e_{fON}-\dfrac{\beta}{C}\cdot i_{fON}=0\end{cases} \qquad (16)$$

The intersections of (s) and (d_1) and, respectively, of (s) and (d_2) determine the boundaries for the validity of (5).

$$\begin{cases}(d_1)\cap(s)=\{P_1\}\\ (d_2)\cap(s)=\{P_2\}\end{cases} \qquad (17)$$

A geometrical approach for the selection of α will be presented. In order to design the control law, it is necessary to determine the convenient points of intersection between the sliding curve (s) and the two characteristics of its derivatives (d_1) and (d_2), which are expressed in (16). All three are presented in the state variable plane in Figure 3. The goal is to make sure that for the given system and a known range of disturbances (output load step), the reaching phase always intersects the control law characteristic when conditions (15) are valid. This means that the intersection will always occur on the [P_1P_2] segment. In order to ensure that, it is necessary to evaluate the evolutions of the state variables during the reaching phase. They depend upon the various initial values (disturbances) and the system is subjected to no switching of the control signal. Generally, the reaching phase does not exceed the range of tens of µs, which is why the expressions of the state variables can be approximated as second order polynomials. Additionally, the time domain is selected in such a way that it prevents inductor saturation under worst case conditions. The stationary points of the state variables in the open time domain 0 - 50µs are evaluated. The solutions of (8) come in the form of a sum of trigonometric functions weighted by exponential functions. It is convenient to expand the exponential and trigonometric functions as Taylor series around the origin, which yields the second order polynomials in (18). The real coefficients a_{0e}, a_{1e}, a_{2e}, a_{0i}, a_{1i} and a_{2i} correspond to the second order approximations of the solutions of (8). The maximum relative error produced as a result of this approximation during the reaching phase is dependent upon the system and the initial conditions of the state variables. However, it was found to be less than 2% for the system used.

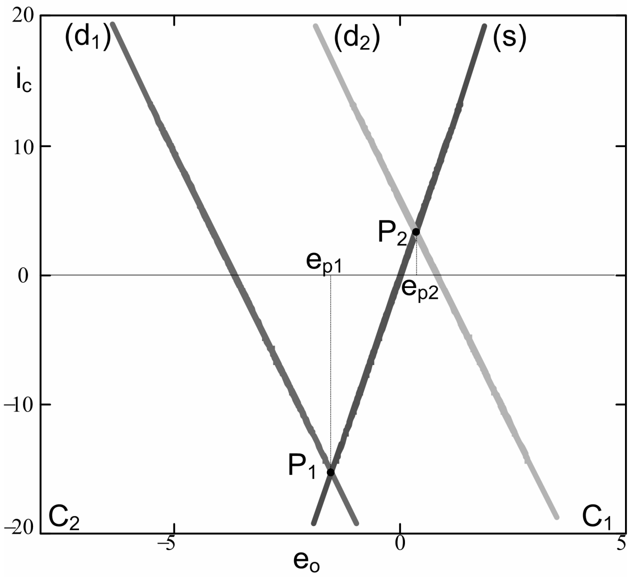

Figure 3. The three lines (s), (d1), (d2) and intersection points P1 and P2.

$$\begin{cases}e_o(t)=a_{2e}\cdot t^2+a_{1e}\cdot t+a_{0e}\\ i_c(t)=a_{2i}\cdot t^2+a_{1i}\cdot t+a_{0i}\end{cases} \qquad (18)$$

The time domain solutions of (8) and their approximations in (18) are plotted in Figure 4. If there is no vertex in the selected time domain, the maxima and minima are found at the domain limits. The maxima of the voltage error in the domain [0, 50 µs] are determined for various initial conditions, depending upon the disturbance, as shown in Figure 4. The selection of α will accommodate for the maximum absolute value of the voltage error.

The absolute maximum value of the voltage error will determine the boundaries of the region of convergence, which are the coordinates of points $\{P_1\}$ and $\{P_2\}$ in Figure 3. The next step is to determine α such that the width of this region is ensured.

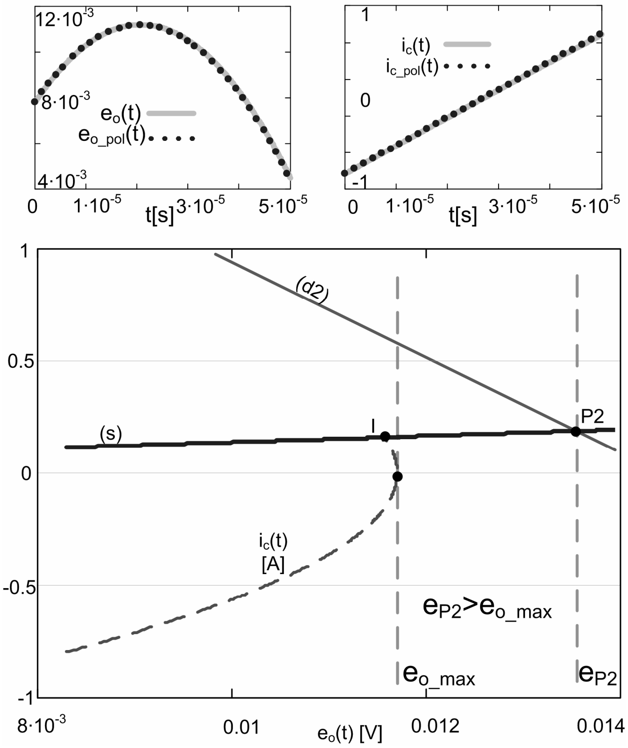

Figure 4. Top: Overlap of the state variables (solid line) and their second order polynomial approximations (dotted line). Bottom: The phase plane of the state variables and the reaching of (s) with respect to (d2).

Considering the maximum absolute value of the state measures determined previously, coordinates for points P_1 and P_2 can be imposed. In the following approach, the maximum absolute value of the voltage error was used, denoted as e_{max}.

$$\begin{cases} e_{P_1} \le -\left|e_{\max}\right| \\ e_{P_2} \ge e_{\max} \end{cases} \tag{19}$$

Conditions (15) become

$$\begin{cases} \dfrac{f_{11}(\alpha)}{f_{12}(\alpha)} \le 0 \\ \dfrac{f_{21}(\alpha)}{f_{22}(\alpha)} \ge 0 \end{cases}, \tag{20}$$

where functions $f11(\alpha)$, $f12(\alpha)$, $f21(\alpha)$ and $f22(\alpha)$ are all quadratic in α. The inequalities are solved and an acceptable range for α is determined.

Figure 5 presents the transient response behavior of a given system and a set of given initial conditions for two different values of α. The admissible range of the parameter was determined according to the previous method to be

$$\alpha \in \left[0;\ 8.2\cdot 10^3\right] \tag{21}$$

The two values in the example are

$$\begin{cases} \alpha 1 = 7.576\cdot 10^3 \in \left[0;\ 8.2\cdot 10^3\right] \\ \alpha 2 = 1.515\cdot 10^4 \notin \left[0;\ 8.2\cdot 10^3\right] \end{cases} \tag{22}$$

It is obvious from Figure 3 and (16) that the two points $\{P_1\}$ and $\{P_2\}$ belong to the third and first quadrant, respectively, on the state variables plane. The aperiodic transient response takes place in on quadrant or the other, as explained in Section 0. The example in Figure 5 considers a situation where the first quadrant is the only one of interest in the representation of the transient response. Therefore, it is only the position of $\{P_2\}$ that matters in this particular case.

These results confirm the validity of the method: when using α_1, the sliding phase commences as soon as the evolution of the system reaches the control line in the phase plane. This behavior stands in contrast to using α_2, when the sliding phase only commences after a second intersection. Additionally, the current peak produced during the transient response is double in magnitude. The same initial conditions were used in both cases.

The selection of α presented above leads to a transient response which comprises two stages: the reaching phase and the sliding phase. The latter is an exponential decay whose time constant is given in (13). Consequently, its duration can be considered to be proportional to the time constant. In this paper, the proportionality factor was considered to be three.

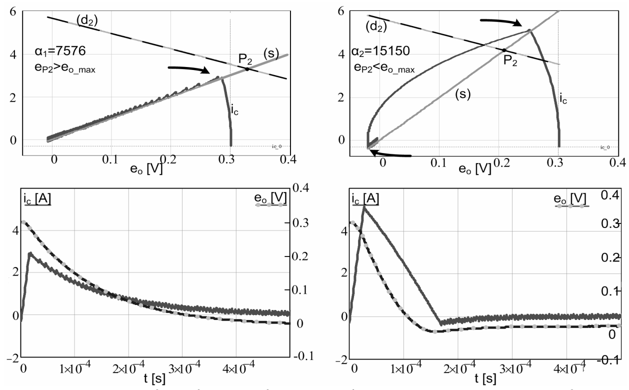

Figure 5. Left: phase plane and transient response for α = 7.57·10^3; Right: phase plane and transient response for α = 1.51·10^4.

The duration of the reaching period was determined using the polynomial approximations presented in Figure 4. Indeed, using (11) and (18), it was possible to determine the duration of the reaching phase as one of the roots of a second order polynomial. The solution had to be strictly positive (or else it would have yielded negative time duration). In order to clearly distinguish between roots if both happened to be positive, the lower value was chosen. A third order polynomial approximation can also be used for better precision. The same approach can be used to determine the stationary points of the state variables, which would lead to the capacitor voltage and inductor current maxima or minima during the transient response.

II. 6 Minimum and maximum switching frequency

Hitherto this version of control does not account for any maximum frequency limitation. This is necessary in order to limit the switching losses. The proposed method is to limit both the ON time and OFF time to take values between 1µs and 5µs. This also produces a minimum frequency limitation, which helps to avoid inductor saturation when necessary and the undesirable shift of frequency towards the audible spectrum. The logic diagram of the algorithm used for ON and OFF time limitation is presented in Figure 6.

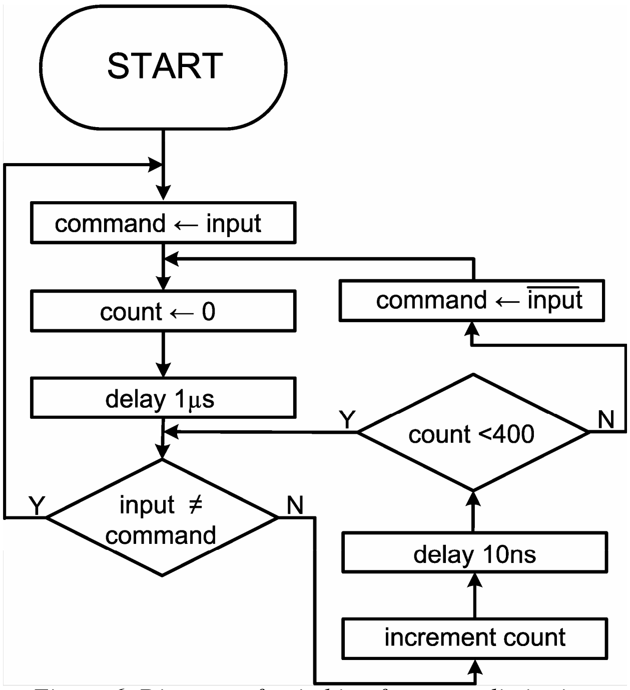

Figure 6. Diagram of switching frequency limitation.

III. MODELS AND SIMULATIONS

The control method presented in the previous sections was implemented in Mathcad by using a series of mathematical expressions. The solutions of (8) and the control law (11) were used in a sequence which follows the flowchart presented in Figure 7.

The step down converter used was specified as follows:

$$\begin{cases} V_i = 9V \\ V_0 = 4.02V \\ R = 1.75\Omega \\ V_{ref} = 0.8V \end{cases} \quad \begin{cases} L = 100\mu H \\ C = 660\mu F \\ \beta = 0.2 \\ R_L = 5m\Omega\,,\, ESR = 50m\Omega \end{cases} \tag{23}$$

The disturbance produced was a step variation in load resistance, from 2.7Ω to 1.75Ω, which translates to the initial conditions of (8) as

$$\begin{cases} e_o = 0.0078V \\ i_c = -0.8A \end{cases}. \tag{24}$$

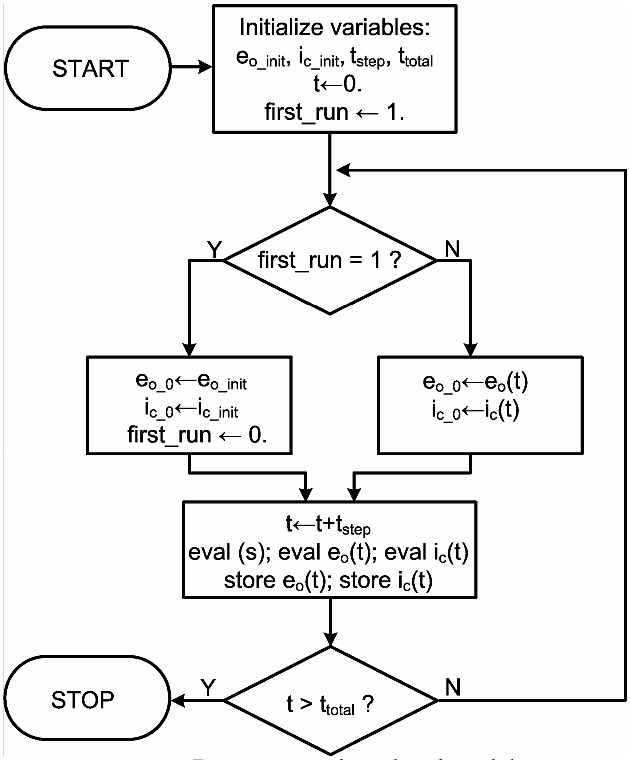

Figure 7. Diagram of Mathcad model.

The expected reaching phase duration and time constant according to (13) are

$$\begin{cases} t_r = 28.8\mu s \\ \tau = 205\mu s \end{cases}. \tag{25}$$

Thus, the expected settling time is

$$t \approx t_r + 3 \cdot \tau \approx 650\mu s. \tag{26}$$

The results are presented in Figure 8, Figure 9 and Figure 10.

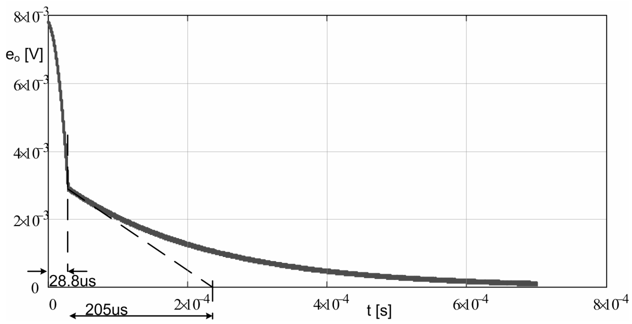

Figure 8. Time variation of error voltage returned by Mathcad model. At the bottom left reaching phase duration and time constant.

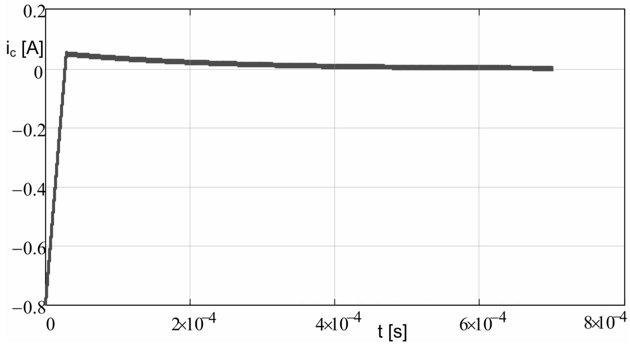

Figure 9. Time variation of capacitor current returned by Mathcad model.

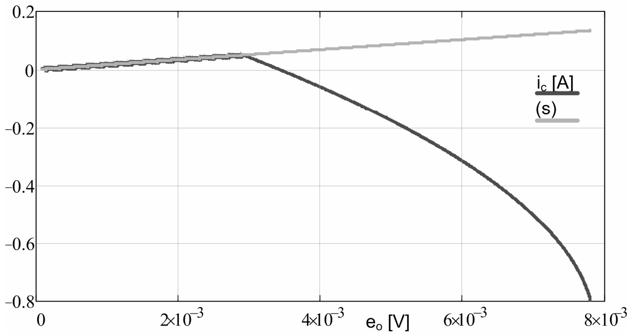

Figure 10. Phase portrait returned by Mathcad model.

The same system was modeled and simulated in Psim. The schematic of the simulation is presented in Figure 11.

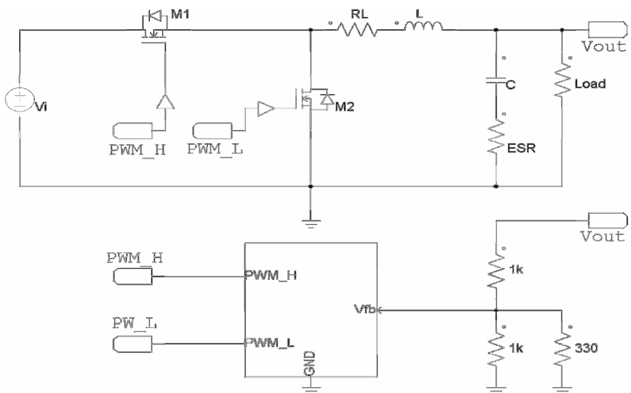

Figure 11. The PSim schematic used for simulation.

The same disturbance yielded the results presented in Figure 12, Figure 13 and Figure 14.

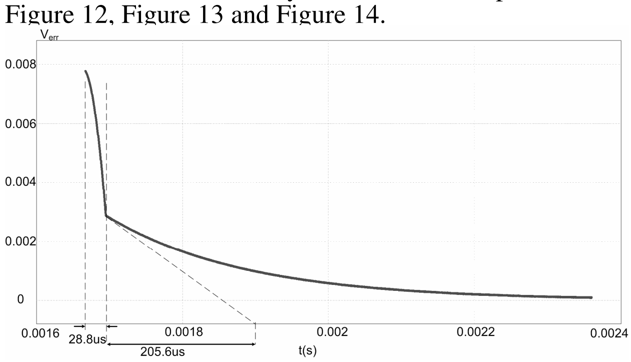

Figure 12. Time variation of error voltage returned by Psim simulation.

At the bottom left reaching phase duration and time constant.

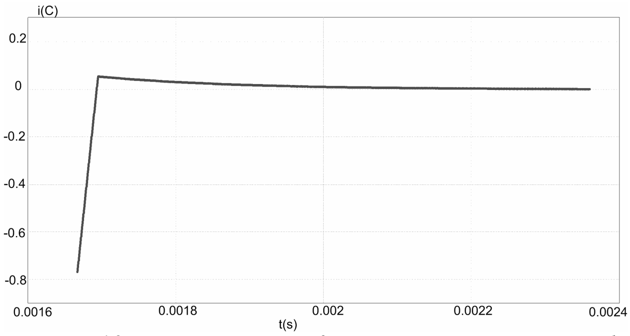

Figure 13. Time variation of capacitor current returned by Psim simulation.

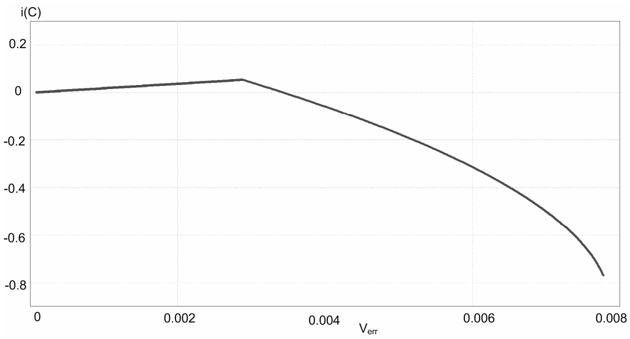

Figure 14. Phase portrait returned by Psim simulation.

Figure 12 indicates the measured values for the duration of the reaching phase and time constant, respectively.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The experimental results were performed on a Microchip development board - DS70181A. The control was implemented in an Artix 7 FPGA from Xilnx. The experimental setup is presented in Figure *15*.

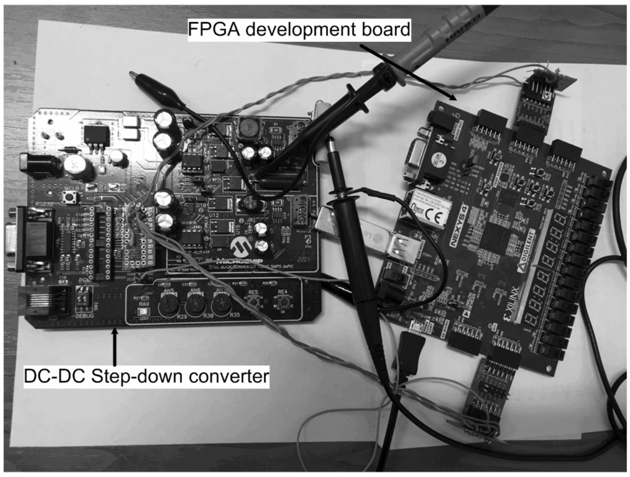

Figure 15. Experimental setup.

The inductor on the step-down converter was replaced by a 100 µH single coil shielded power inductor. The 12-bit data acquisition of the FPGA is possible via an ADC PmodAD1 which is set to operate at 730ksps. The track-and-hold maximum acquisition time and the conversion time are specified to be 400ns and 1.33µs, respectively. The Psim simulation model was amended to account for that. The new Psim simulation results are presented in Figure 16, Figure 17 and Figure 18.

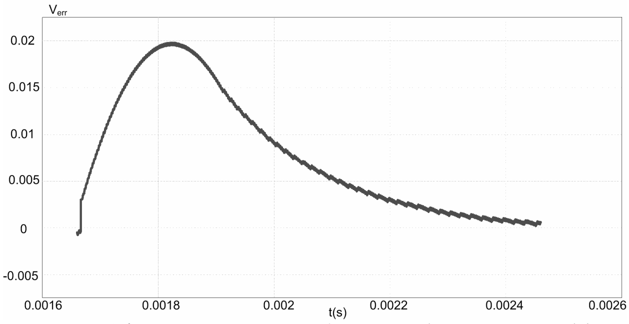

Figure 16. Time variation of error voltage returned by Psim simulation. The ADC sample & hold durations have been considered.

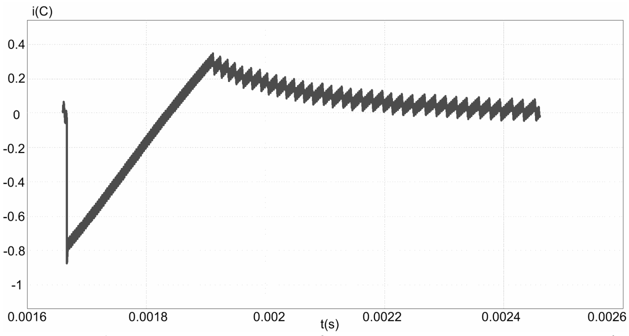

Figure 17. Time variation of capacitor current returned by Psim simulation. The ADC sample & hold durations have been considered.

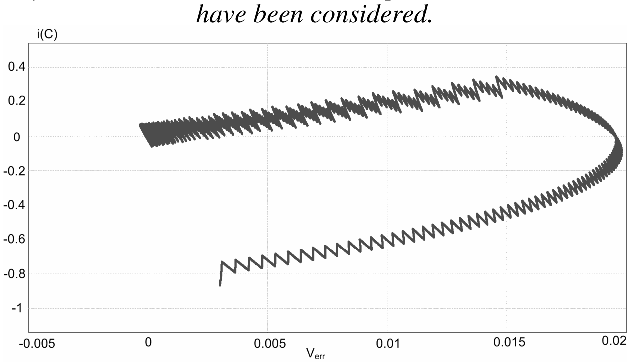

Figure 18. Phase portrait returned by Psim simulation. The ADC sample & hold durations have been considered.

One consequence of the previous operation is the fact that there will be switching cycles during the reaching phase. That is because the observed derivative component corresponding to the capacitor current swings between positive and negative values. In fact, the transient state derivative of the error voltage is no longer proportional to the capacitor current. It does go to zero in steady state, however. This is the impact of sampling and it may be alleviated by using a higher performance ADC. The aforementioned switching leads to longer transient times and higher values for the state variables.

In order to produce experimental results, the output voltage and the output current were measured instead of the state variables presented in the previous plots. The waveforms generated by the model in PSim are presented in Figure 19 and Figure 20. Their experimental counterparts are presented in Figure 21 and Figure 22. In order to emphasize the transient response, the ac coupling mode was used.
The output voltage of Figure 19 and Figure 21 both show a dip of approximately 40mV and a settling time of approximately 75µs.

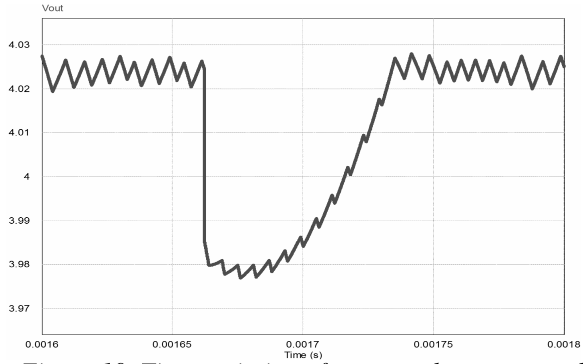

Figure 19. Time variation of output voltage returned by Psim simulation. The ON/OFF time limitation has been implemented.

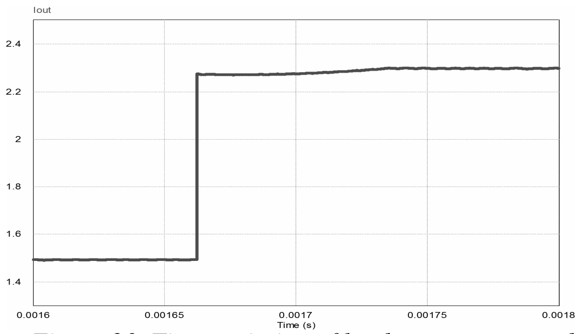

Figure 20. Time variation of load current returned by Psim simulation. The ON/OFF time limitation has been implemented.

The current measurement is performed using a 50mΩ sense resistance and an amplification of 50. The value corresponding to the initial load of 2.7Ω was subtracted in order to better emphasize the transient response.

The simulated and experimental results are correlated in terms of both amplitudes and settling times.

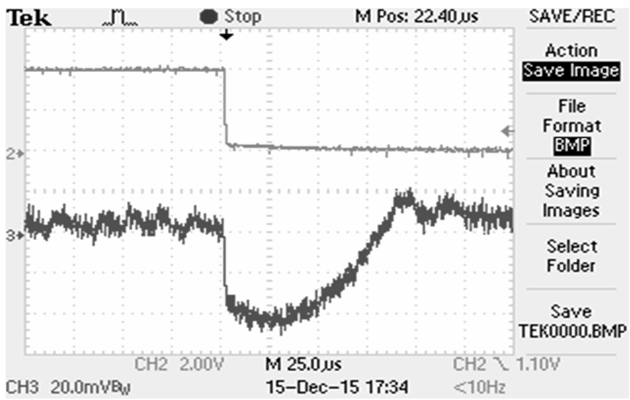

Figure 21. Time variation of output voltage. Experimental result.

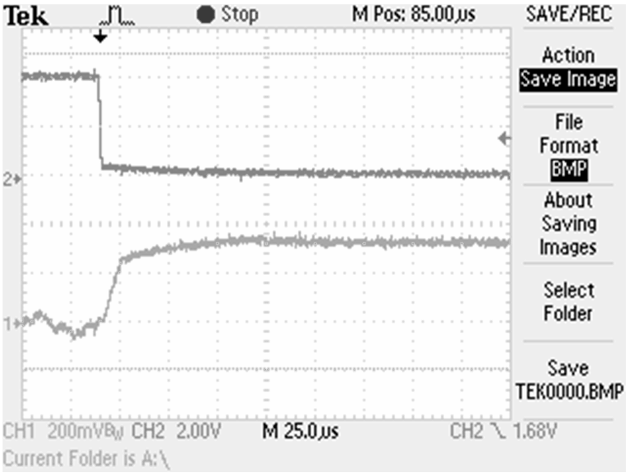

Figure 22. Time variation of load current. Experimental result.

V. CONCLUSION

The paper presents the design of a SM controller used with a step-down converter. The proposed design can produce an aperiodic transient response and it can estimate the settling time for a given disturbance. In order to achieve this goal, the step-down converter was modeled as a second order linear system. Additionally, the state variables were selected in such a way that the equilibrium point was the same, regardless of the system parameters. The new set of first order linear differential equations for this new set of state variables was inferred as two autonomous systems, as is the case for a VSS. The two are successively valid in the present case of continuous conduction mode and their validity only depends upon the command signal.

The SMC was briefly introduced, before it was expressed for the previously defined system. The entire system was modeled in Mathcad and simulated in Psim. The results are correlated, which confirms the validity of the created model. Subsequently, the Psim circuit was amended to account for the physical limitations imposed by the ADC. The new simulation results are correlated with the experimental results, which confirms the accuracy of the model. The investigation of the impact that the ADC speed has on the overall feedback loop can constitute the grounds for future work.

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