DISCRETE-TIME SIMULATION OF SWITCHED MODE POWER SUPPLIES USING NUMERICAL INTEGRATION FOR EDUCATIONAL PURPOSES

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Abstract: This paper presents a discrete time simulation procedure of switched mode power supply (SWPS) power stages using Euler's forward method for numerical integration. Usually, the simulation of SMPS power stages is carried out in PSPICE alike circuit simulators, but sometimes this is inconvenient and slow. The proposed simulation method may be used for educational purposes, whenever a quick and easy illustration of the SMPSs is desired. Furthermore, it can be deployed in the development of digital control algorithm, as the method may be implemented in logic simulators (event driven or delta time simulators). This discrete time modeling procedure can be implemented in any number crunching environment (Matlab, Octave, NumPy, etc.), in a logic (event-driven) simulator or in a simple spreadsheet. The procedure consists in (i) writing the ordinary differential equations (ODEs) of the modelled power stage, (ii) solving the ODE using numerical methods. Several power stage models were developed and simulated: (i) an ideal buck-boost was simulated in MATLAB, (ii) a boost converter simulated in a spreadsheet and (iii) an ideal synchronous buck converter was described in a hardware description language, VHDL. The numerical error between discrete time and PSCIPE simulation results are negligible.

Keywords: *Ordinary differential equations, Logic simulation, Switching converters, Euler's Method, VHDL.*

I. INTRODUCTION

The paper presents a discrete time simulation procedure of several switched mode power supply (SWPS) power stages. Usually, the power stages [1-2] are simulated in Spice like electrical circuit simulators. Spice simulations are completely legitimate, whenever the effects of the switching components (power diodes, MOSFETs, etc.) and other circuit nonidealities (equivalent serial resistance, parasitic components, inductor code magnetism) are sought to be analyzed [3]. A designer can obtain very accurate results in Spice, for the expense of simulation time. Nevertheless, Spice simulation remains just a simulation, there is no guarantee it will work the same in practice. Also, numerical convergence of the Spice solver is easily jeopardized, especially when SPMPs are simulated with ideal switches. Moreover, Spice simulations can be misleading: as the electrical ground is modelled with a 0 V voltage source, and it can inject charges in the simulated circuit – this can result in corrupted waveforms when simulating switching circuits.

In some situations, there is no need for high accuracy SPMS power stage modeling or Spice simulator is not an option. For example, designing a control loop for a power stage or the illustration of power converter behavior in student classes can have less accuracy. Ref. [4] emphasize the importance of computer techniques in the modeling of DC/DC converters. A widespread approach for power stage modeling and simulation is the state-space model [5-6]. In [5] power converter stages are modelled using a space-state approach, and implementation is carried out in Simulink. A state-space averaging model is described in [6], created with the intention of obtaining fast simulation algorithms. The average state space model recently was applied for modeling multiphase converters [7]. Ref. [8] propose a transient state analysis method based on the differential equations of equivalent converter circuits, applying Laplace and z transforms to solve the differential equations.

The use of simulation in class environments is almost mandatory and – in some cases – it was integrated to virtual training environments. A such Cyber Physical System to power electronics simulation, control and testing was presented in [9]. The presented framework achieves power electronic simulation by solving the state space equations of a power converter.

Another possible application of the proposed simulation method is related to the development and implementation of digital control on microcontrollers and field programmable gate arrays [10]. The co-simulation of digital control and analog power stage is carried out with costly mixed-signal simulators [11-12]. To avoid the use of a mixed-signal environment, a discrete time simulation of the power stage can be achieved, in any numerical environment, moreover, in a logic simulator, too. In [13] a step-by-step design guide for FPGA based compensator is given for a buck converter. The power stage is described using VHDL by means of the difference equations of the inductor current and capacitor voltage. In [14] the

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digitization process of an analog controller is described, the implementation targeting a microcontroller platform.

The main contribution of the paper is the discrete time simulation procedure, that follows the next steps: (i) the analysis of the power stage, drawing the equivalent circuits in each operation mode with respect to switch positions - this step is quite straightforward, as the operation of converters can be found in many text books [1-2]; (ii) writing an ordinary differential equation (ODE) system for the equivalent circuits – usually the inductor current and capacitor voltage are the two quantities that must be solved [5,13,14]; (iii) solving the ODEs with Euler's method [15] – basically, establishing the iterative process to solve for the inductor current and the capacitor voltage; (iv) use a numerical environment to evaluate the iterative process. Another significant contribution is the synthesizable VHDL description of the asynchronous buck power stage, thus the hardware emulation of the power stage can be achieved in a Field Programmable Gate Array (FPGA).

The paper is organized as follows: In section II, we will revisit Euler's forward method; in section III. The simulation procedure is applied for a buck-boost, a boost and a synchronous buck power stage. The buck-boost converter simulation was carried out in MATLAB. To validate the result of the simulations the steady state output voltage (equal to the capacitor voltage) is plotted against the duty cycle. The so obtained duty-cycle to output-voltage transfer function shows good numerical matching with the theoretical values. The boost stage was implemented using a spreadsheet application. The obtained time domain waveforms are compared to Spice simulation carried out in LTSPICE. The buck converter vas implemented in a hardware description language, VHDL, and simulations were carried out in an gHDL, an open-source logic simulator. The so obtained discrete time simulation results are compared with an LTSPICE simulation. In section IV results are reiterated. Finally in section V. conclusions are drawn and further work is appointed.

II. EULER'S METHOD - REVIEW

Simple ODEs could be solved using symbolic computation or analysis, for example integral transforms such as the continuous domain Laplace or the discrete domain z transform [16]. In [8] the power stage model contains only ideal components, no parasitic ones. Thus, the ODE is kept simple and Laplace transform could be deployed to solve it. Many ODE do not have a "nice", closed form, analytical solution. The best one can do is to approximate the solution knowing an initial value and the differential equation to be obeyed. The initial value problem is mathematically formulated as follows:

$$\frac{dy(t)}{dt} = f(t, y(t)) \qquad y(t_0) = a \tag{1}$$

where $f(t,y(t))$ is an arbitrary function of variables t and $y(t)$, t_0 is the initial moment, and a is the initial value. If the above is given, then Euler's method offers a way of computing the "trajectory" of any $y(t)$. To do this, first, the t variable discretized or sampled:

$$t_n = t_0 + n \cdot \Delta t \tag{2}$$

where n is the index of the sample, and Δt is a sufficiently small value. We shall refer to it as the simulation step size. The iterative process to compute $y(t_n)$ is:

$$y(t_{n+1}) = y(t_n) + \Delta t \cdot f(t_n, y(t_n)) \tag{3}$$

For simpler notation one can use $y_n = y(t_n)$. Note that other numerical integration methods can also be used.

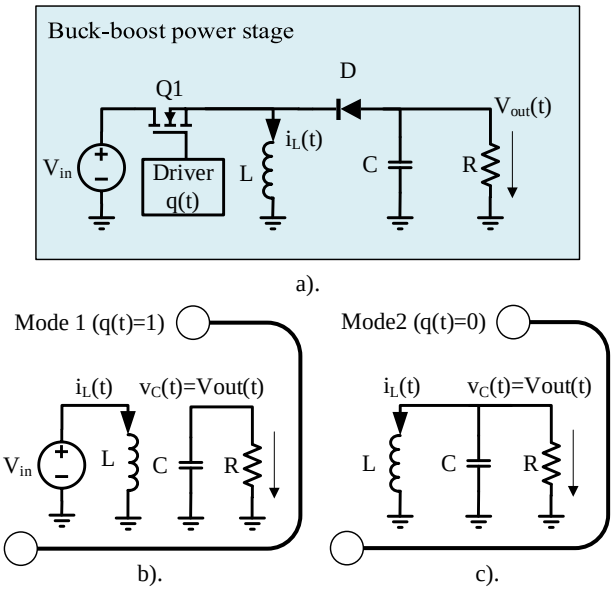

Figure 1. a) Buck-boost power stage b) operation mode while switch Q1 is closed c) operation mode while switch Q2 is open

III. DISCRETE TIME SIMULATION OF SPMS POWER STAGES

In this section, the proposed simulation method is illustrated for three converter topologies: buck-boost, boost, and buck.

A. Buck-Boost Discrete Time Simulation

In Fig. 1. the (invertor) buck-boost power stage is depicted (Fig. 1a), alongside its operation modes (Fig. 1b and 1c). The differential equations for both equivalent circuits are given in (4) and (5). A driver circuit generates the pulse width modulated (PWM) signal noted $q(t)$.

When $q(t)=1$, then the controlled switch is on; otherwise, $q(t)=0$, and the switch is off. In the first operation mode, the inductor current i_L is drawn from the voltage source, V_{in}; the energy is loaded into the inductor. In this case, the load current is upheld by the capacitor. In the second operation mode, the inductor is connected to the capacitance and the load. The energy stored in the inductor is now transferred into the capacitance and the load. The capacitor voltage v_C equals to the output voltage V_{out}.

The differential equation system for the equivalent circuit of Mode 1 and 2 are given in (4), respectively (5) [17].

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}V_{in} \\ \dfrac{dV_{out}(t)}{dt} = -\dfrac{1}{C}\dfrac{V_{out}(t)}{R} \end{cases} \quad (4)$$

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left(V_{out}(t)\right) \\ \dfrac{dV_{out}(t)}{dt} = -\dfrac{1}{C}\left(i_L(t) + \dfrac{V_{out}(t)}{R}\right) \end{cases} \quad (5)$$

Eq. system (4) and (5) can be merged with the help *q(t)*, which represents a PWM signal. Note that the value of *q(t)* is 1 when the switch is on, and it is 0 when the switch is off. For the first and second mode, the change of the inductor current is expressed $q(t)*V_{in}/L$, respectively $q'(t)*V_{out}(t)/L$, where *q'(t)* is the "complementary" of *q(t)*, and it is equal to *1-q(t)*. Overall, the inductor current variation is $q(t)*V_{in}/L + q'(t)*V_{out}(t)/L$. Similarly, the variation of capacitor voltage v_C can be obtained. The resulting ODE is:

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left[q(t)V_{in} - q'(t)V_{out}(t)\right] \\ \dfrac{dV_{out}(t)}{dt} = -\dfrac{1}{C}\left[q'(t)i_L(t) + \dfrac{V_{out}(t)}{R}\right] \end{cases} \quad (6)$$

The next step is to derive the iterative process, as Euler's method requires. The ODE in (6) is solved for the inductor current i_L and the capacitor voltage v_C. Note that the V_{out} equals v_C. Although q(t) varies with time, it is treated as a parameter as its value is known over the simulated time interval. We also assume, i_L =0 A and v_C = 0 V, as initial conditions. The resulting iterative process and its corresponding pseudocode are given in Eq. (7), respectively Fig. 2.

$$\begin{cases} i_L(t_0) = 0, V_{out}(t_0) = 0 \\ i_L(t_{n+1}) = i_L(t_n) + \left(q(t_n)V_{in} - V_{out}(t_n)\right)\dfrac{\Delta t}{L} \\ V_{out}(t_{n+1}) = V_{out}(t_n) - \left(q'(t_n)i_L(t_n) + \dfrac{V_{out}(t_n)}{R}\right)\dfrac{\Delta t}{C} \end{cases} \quad (7)$$

The algorithm presented in Fig. 2 was implemented in MATLAB; the implementation is attached in Appendix A. To verify the correctness of the simulation, we plotted the duty cycle to output voltage transfer function of the converter [18]:

$$V_{out}(D) = -\frac{D}{1-D}V_{in} \quad (8)$$

where *D* is the duty cycle of the PWM signal *q(t)*. To plot the transfer function, several discrete-time simulations were run with the input values summarized in Table I. The discrete-time simulations were run for 20 ms, as this time was considered enough for the converter to reach a steady state. The last 100 samples of the voltage waveform were averaged and noted. The so obtained values are presented in Fig. 3. In a first run, we considered the step size $\Delta t = 5 \cdot 10^{-7}$ s, the so obtained characteristics are depicted with a dotted line. A second run was carried out with $\Delta t = 10^{-7}$ s, the result being plotted with the dashed line. The theoretical value is depicted with the solid line. As expected, with the decrease of the simulation step the accuracy increase.

Algorithm: inverting buck-boost simulation
Input: Δt, L, C, R, Vin, q(t)
Output: Vout, iL
1: **initialize** Vout← 0, iL←0
2: **loop forever**
3: **compute** q' = 1-q
4: **compute** iL_new ← iL + (q·Vin + q'·Vout) Δt / L
5: **compute** Vout_new ← Vout-(q'·iL + Vout/R)Δt/C
6: **update** iL ← maximum(iL_new,1e-20)
7: **update** Vout ← Vout_new
8: **end loop**

Figure 2. Time domain simulation of inductor current $i_L(t)$ and capacitance voltage $v_C(t)$ in an inverter buck-boost converter

B. Boost Discrete Time Simulation

The simulation procedure was implemented for a boost converter in Excel (see Appendix C), to demonstrate the ease of implementing and deploying the proposed method.

Let us consider the boost converter architecture in Fig. 4. In the first operation mode, the inductor current i_L and the load current are supplied by the voltage source V_{in}, respectively, the accumulated charges in the capacitor. In the second operation mode, both the capacitor and load

TABLE I. POWER STAGE AND SIMULATION PARAMETERS

Input	*Value*
Δt simulation step size	10^{-7} s and $5 \cdot 10^{-7}$
Duty cycle	*0 to 1, with 0.1 step*
Simualtion time	*20 ms*
L - inductor	*100 uH*
C- capacitance	*100 nF*
R - load	*12.5 Ω*
fswitching	*100kHz*

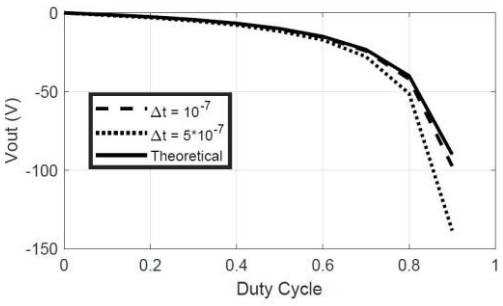

Figure 3. The buck-boost converter's transfer function with respect to considered step sizes Δt.

currents are sustained by the inductor current i_L. The differential equations of the two operation modes [19] are also given in Fig. 4. The next step is to establish a single ODE from this pair of equations, considering the control signal $q(t)$. The overall inductor current change is $q \cdot V_{in}/L + q' \cdot (V_{in} - V_{out}(t))/L$. As $q+q'=1$, the final expression is $di_L(t)/dt = (V_{in} - q' \cdot V_{out}(t))/L$. Similarly, the variation of capacitor voltage v_C can be obtained.

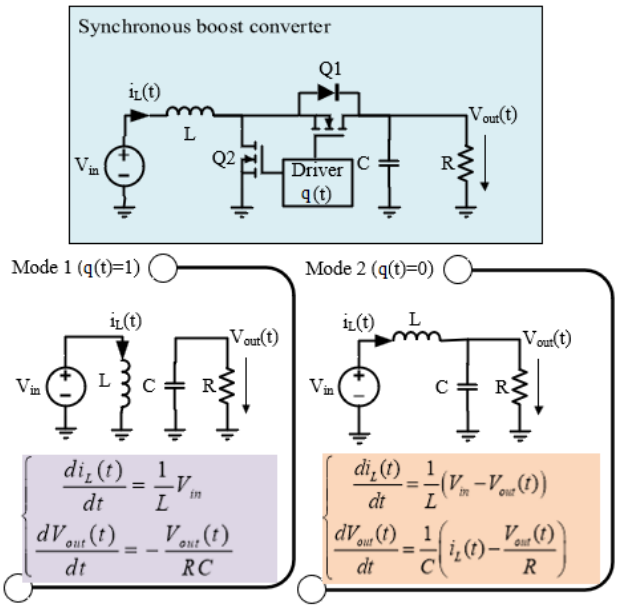

Figure 4. a). Boost power stage b) operation mode and equivalent circuit equation when switch Q1 is open (Q2 is closed) c). operation mode and equivalent circuit equation when switch Q1 is closed (Q2 is open)

$$\begin{cases} \dfrac{di_L(t)}{dt} = \dfrac{1}{L}\left[V_{in} - q'(t)V_{out}(t)\right] \\ \dfrac{dV_{out}(t)}{dt} = \dfrac{1}{C}\left[q'(t)i_L(t) - \dfrac{V_{out}(t)}{R}\right] \end{cases} \quad (9)$$

The iterative process to solve eq. (9), considering the initial inductor current and capacitor voltage to be 0A, respectively 0V, is obtained in eq. (10). The corresponding pseudocode is depicted in Fig. 5.

$$\begin{cases} i_L(t_0) = 0, V_{out}(t_0) = 0 \\ i_L(t_{n+1}) = i_L(t_n) + \left(V_{in} - q'(t)V_{out}(t_n)\right)\dfrac{\Delta t}{L} \\ V_{out}(t_{n+1}) = V_{out}(t_n) + \left(q'(t_n)i_L(t_n) - \dfrac{V_{out}(t_n)}{R}\right)\dfrac{\Delta t}{C} \end{cases} \quad (10)$$

The verification of the resulting simulation was carried out by a comparison with an electrical model simulated in LTSpice, presented in Appendix B. The results are depicted

Algorithm: boost simulation
Input: Δt, L, C, R, Vin, q(t)
Output: Vout, iL
1: **initialize** Vout← 0, iL←0
2: **loop forever**
3: **compute** q' = 1-q
4: **compute** iL_new ← iL + (Vin + q'·Vout) Δt / L
5: **compute** Vout_new ← Vout+(q'·iL – Vout/R)Δt/C
6: **update** iL ← maximum(iL_new,1e-20)
7: **update** Vout ← Vout_new
8: **end loop**

Figure 5. Time domain simulation of inductor current $i_L(t)$ and capacitance voltage $v_C(t)$ in a boost converter

in Fig. 6. In the first plot, the voltage waveform resulting from the discrete-time simulation – carried out in an Excel spreadsheet – and LTSPICE simulation are presented. The differences between the two waveforms are hard to distinguish. Moreover, a sample-to-sample comparison of the discrete-time simulation and the Spice model is not possible because the Spice solver uses variable step size, while the proposed simulation procedure has a fixed step size, the Δt. Instead, we evaluated the average of samples in a time-window, ie. 100 Δt and the relative error was computed and plotted. In the second plot, the relative error

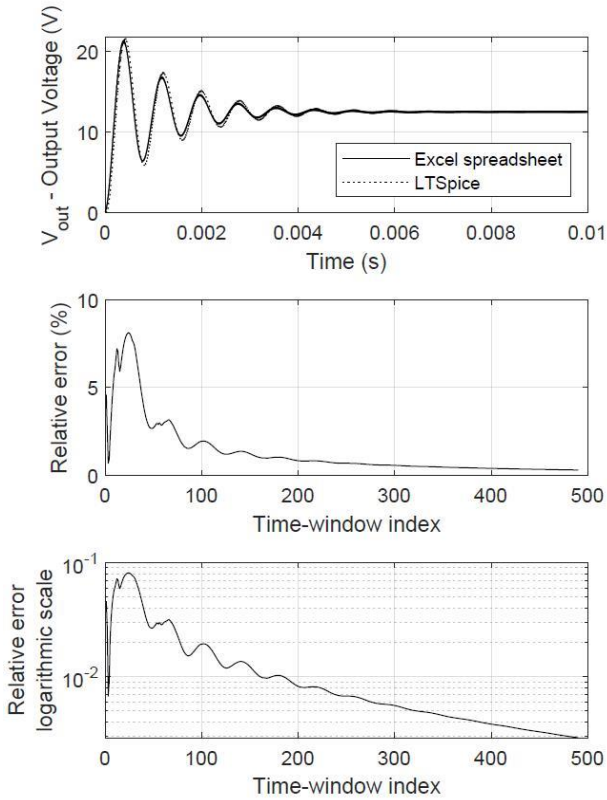

Figure 6. Waveform comparison of the proposed simulation procedure implemented in Excel and LTSPICE simulation. The plots show the two waveforms and the relative error in percent and on a logarithmic scale

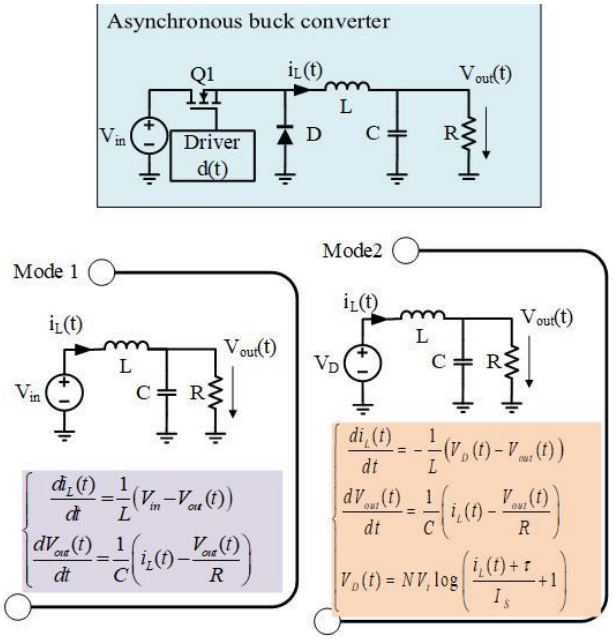

Figure 7. a). Buck power stage, b). operation mode when switch Q1 is closed and its equivalent differential equations c) operation mode when switch Q1 is open and its equivalent differential equations

is presented, where the peak value is approximately 0.08 (8%), and it is decaying as the converter reaches steady state. The relative error was also plotted on a logarithmic scale. As the converter reach steady state, the relative error approx. 10^{-3}. These differences between the discrete-time and Spice simulations are due to the ideal switch model in LTSpice, which has on and off resistances. These resistances are neglected in the discrete-time simulations, but their effects can be included in the ODE in (9).

C. Asynchronous Buck Simulation

The asynchronous buck converter was simulated in an event-driven simulation environment, gHDL. Event-driven or logic simulators are used for functional and timing simulation of digital circuits/systems. The possibility of simulating a power stage in an event-driven simulator permits the simulation of analog and digital stages in a single environment; thus, the development, testing, and verification of digital control algorithms are facilitated.

The asynchronous buck converter model is depicted in Fig. 7, alongside its operation modes and governing differential equations. In operation mode 1, the inductor stores the energy from the voltage source V_{in}, while in operation mode 2, the stored energy is transferred to the load [20]. In the previous examples (buck-boost and boost), the diodes were modeled as ideal switches. In the asynchronous buck model, we keep the forward voltage drop on the diode V_D in the model. The forward voltage of the diode was expressed from the diode current equation:

$$V_D = NV_t \log\left(\frac{I_D}{I_S}+1\right) \tag{11}$$

where N is the ideality factor of the diode, V_t is the thermal voltage at room temperature, I_s is the saturation current, and I_D is the current through the diode, which is equal to i_L in this case.

Algorithm: Asynchronous buck model
Input: Δt, L, C, R, Vin, q(t) converter parameters
N, Vt, Is (diode parameters)
Output: Vout, iL
1: **initialize** Vout← 0, iL←0
2: **loop forever**
3: **compute** iL_new ← iL+(q*Vin–(1–q)*Vd+Vout)*Δt/L
4: **compute** Vout_new ← Vout + (iL– Vout/R) * Δt / C
5: **update** iL ← maximum(iL_new,1e-20)
6: **update** Vout ← Vout_new
7: **update** Vd ← N*Vt*log((iL + 1e-9) / Is + 1)
8: **end loop**

Figure 8. Time domain simulation of inductor current $i_L(t)$ and capacitance voltage $v_C(t)$ in an ideal

As in previous examples, the next step is to establish a single ODE, considering the control signal *q(t)*. This step results in eq. (12):

$$\begin{cases} \dfrac{di_L(t)}{dt}=\dfrac{1}{L}\left[q(t)V_{in}-q'(t)V_D(t)+V_{out}(t)\right] \\ \dfrac{dV_{out}(t)}{dt}=\dfrac{1}{C}\left[i_L(t)-\dfrac{V_{out}(t)}{R}\right] \\ V_D(t)=NV_t\log\left(\dfrac{i_L(t)}{I_S}+1\right) \end{cases} \tag{12}$$

The corresponding iterative process to solve (12) and its pseudocode is presented in eq (13), respectively Fig. 8.

$$\begin{cases} i_L(t_0)=0, V_{out}(t_0)=0 \\ i_L(t_{n+1})=i_L(t_n)+\begin{pmatrix} q(t_n)V_{in}- \\ -q'(t_n)V_D(t_n)+ \\ +V_{out}(t_n) \end{pmatrix}\dfrac{\Delta t}{L} \\ V_{out}(t_{n+1})=V_{out}(t_n)+\left(i_L(t_n)-\dfrac{V_{out}(t_n)}{R}\right)\dfrac{\Delta t}{C} \\ V_D(t_{n+1})=NV_t\log\left(\dfrac{i_L(t_n)}{I_S}+1\right) \end{cases} \tag{13}$$

The algorithm depicted in Fig. 8. was implemented in VHDL (see the code in Appendix D), and discrete-time simulations were carried out in gHDL. The compare the resulting capacitor voltage waveform an electrical model in LTSpice was simulated (see the model in Appendix E). The resulting waveforms are presented in Fig. 9. The differences between the two waveforms are undistinguishable for the free eye. We evaluated the average of samples in a time-window, ie. 100 Δt and the relative error was computed and plotted. In the second plot, the relative error is presented, where the peak value is approximately 0.15 (15%), and it is decaying as the converter reaches steady state. The relative error was also plotted on a logarithmic scale. As the converter reaches steady state, the relative error approximately 10^{-2}. These

differences between the discrete-time and Spice simulations are due to on and off resistances of the Spice switch and diode models. These resistances are neglected in the discrete time simulations, but their effects can be included in the ODE in (13).

IV. NUMERICAL RESULTS

The results were presented in the previous section but let us revisit them. Three use cases of the proposed discrete time simulation method were presented: a buck-boost, a boost, and a buck power stage.

The buck-boost simulation was carried out in MATLAB. To validate the buck-boost power stage simulation, the duty cycle to output voltage characteristics was plotted in Fig. 3. As the simulation step Δt decrease (a higher precision simulation is carried out), the obtained characteristics converge to the theoretical solution.

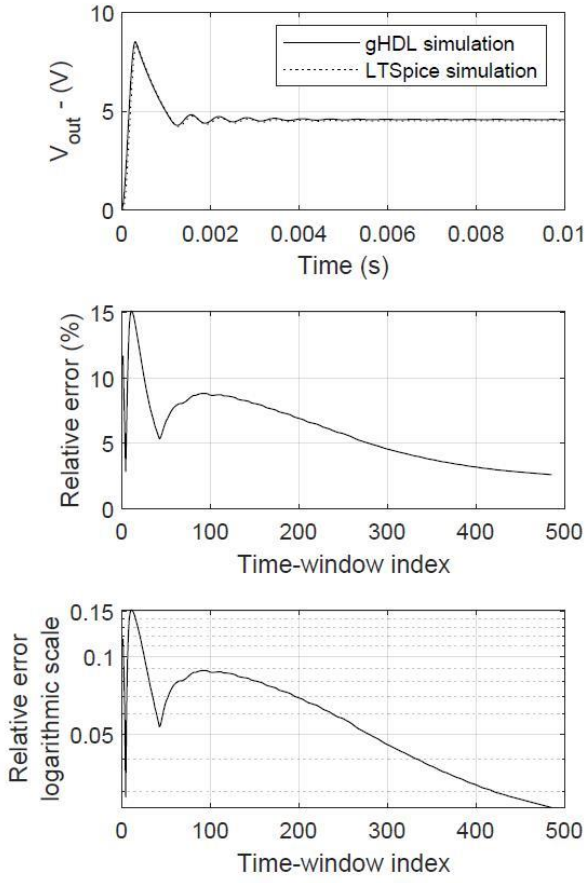

Figure 9. Waveform comparison of the proposed simulation procedure implemented in gHDL and LTSPICE simulation. The plots show the two waveforms and the relative error in percent and on a logarithmic scale.

The boost simulation was carried out in an Excel spreadsheet. The validation was done by comparing the output voltage waveform to the one resulting from a Spice transient analysis. In Fig. 6, the voltage waveforms are plotted. As the discrete time and Spice simulation results cannot be distinguished with the free eye, the relative error is plotted in percent and logarithmic scale. While the boost is in a transient state, the maximum relative error is 8%. When the power stage reaches steady state, the relative error falls below 10^{-3}. Note that the Spice electrical model includes the effect of the on and off resistances of the switching components.

The buck power stage was described in VHDL language and simulated in gHDL. The obtained output voltage waveform was compared to one resulting from a Spice simulation. In the case of the asynchronous buck converter, we also include the forward voltage drop of the diode in eq. (12). In Fig. 9. the voltage waveforms and the relative errors were plotted. In the transient state of the buck power stage, the maximum relative error is 15%, but as steady state is reached, the relative error is approx. 10^{-2}. Note that the Spice electrical model includes the effect of the on and off resistances of the switching components and the diode.

The event-driven real number (RN) modeling described in [21] is a working alternative of our procedure. The RN modeling consists of the discretization of a continuous time transfer function, end the evaluation of the discrete transfer function in the event-driven simulator. This solution fits linear components, such as operational amplifiers, filters, but not switch mode circuits as power converters.

V. DISCUSSION AND FURTHER WORK

A significant result is that the method could be implemented in an event-driven (logic) simulator, such as gHDL. The VHDL description of the power stages can be immediately used to develop of digital control circuits, as power and control sections can be simulated in the same environment, with no need for a mixed-signal or co-simulation.

In essence, an analogue circuit was simulated in a logic simulation environment. This opens a new possibility: if ordinary differential equations can describe the functionality of an analog circuit, then it can be simulated in an event-driven simulator. Further work is focused on applying the simulation method to other classes of analog circuits (analog filters, oscillators, etc.) and switched capacitor circuits (amplifiers, filters, relaxation oscillators, etc.).

The proposed discrete simulation process can be extended for other converter topologies, to name a few important ones: synonymous buck, Cuc [22], SEPIC [23], multiphase buck [24-25] and resonant converters [26].

This simulation model can be implemented in any hardware description language, thus creating hardware emulators. When actual power stages are not available, a customized emulator can be developed. However, these implementations require the use of an FPGA [27].

VI. CONCLUSIONS

The paper presents a discrete time simulation procedure of several switched-mode power supply (SWPS) power stages. The proposed discrete-time simulation procedure follows the following steps: (i) the analysis of the power stage, drawing the equivalent circuits in each operation mode with respect to switch positions (ii) writing an ODE system – usually the inductor current and capacity voltage are the two quantities expressed in the ODE; (iii) solving the ODEs with Euler method – or any other numerical integration method; (iv) use a numerical environment to compute the iterative process.

Three power stages – buck-boost, boost, and buck – were simulated in various number-crunching environments

– MATLAB, Excel, and gHDL. The resulting output voltage waveform was compared to Spice simulations. In the transient state of the power stage, the relative error did not exceed 15%. When the power stage reached a steady state, the relative errors are considerably lower, reaching 10^{-2} and 10^{-3} for the boost, respectively buck power stage.

APPENDIX A

The MATLAB code sequence in Fig. 10 illustrates a possible implementation of the discrete time buck-boost power stare simulation. The inputs of the script are the power stage parameters (capacitance, inductance, load, switching frequency, duty cycle), initial conditions (input voltage source, inductor current and capacitor (output) voltage), and simulation parameters (simulation step and simulation time).

```
%% Initializations
C=100e-6; %capacitor value 100uF
L=100e-6; %inductor value 100uH
R=12.5;         %load value 12.5Ω
deltaT=5e-8; %the step value Δt
duty = 0.75; %duty cycle
Vin = 10;               %Voltage source
fswitch = 100e3; %Switching frequency
tsim = 20e-3;                   %time interval
%%generate pwm signal
time=0:deltaT:tsim;
tri = (sawtooth(2*pi*fswitch*time)+1)/2;
pwm = double(tri < duty);
subplot(2,1,1)
Tau = 1e-9;
%% Initial conditions
iL = [0];
Vout = [0];
%% Iterative process
for i=1:length(time)
    iL = [iL max(Tau,iL(end) + 1/L*(Vin*pwm(i) +
(1 - pwm(i))*(Vout(end)))*deltaT)];
    Vout = [Vout Vout(end) - (iL(end)/C * (1-
pwm(i)) + Vout(end)/R/C)*deltaT];
end
%%plotting
subplot(2,1,1)
plot(time,iL(1:end-1));
subplot(2,1,2)
plot(time,Vout(1:end-1));
```

Figure 10. Matlab code for the buck-boost power stage simulations

APPENDIX B

The boost power stage was modeled in LTSpice (Fig. 11). The switching components were modeled with ideal switches, including on and off resistances *Ron* = 1mΩ, respectively *Roff* = 1MΩ. The PWM control signal was generated using Pulse voltage sources, heaving a duty cycle equal to 20% and switching frequency of 100kHz. The buck converter component values were listed earlier in Table I.

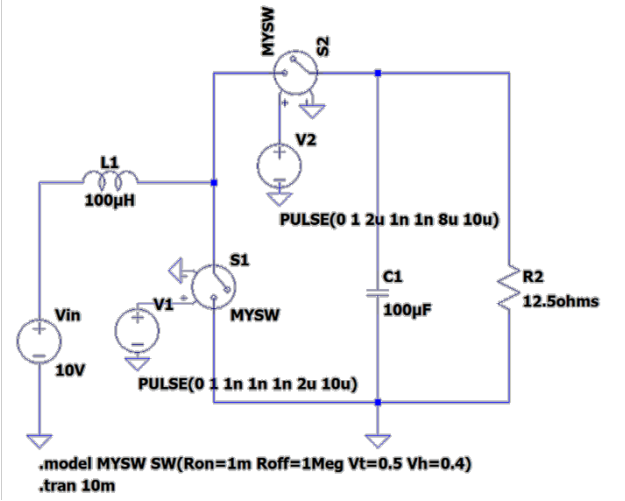

Figure 11. LTSpice model of the boost power stage

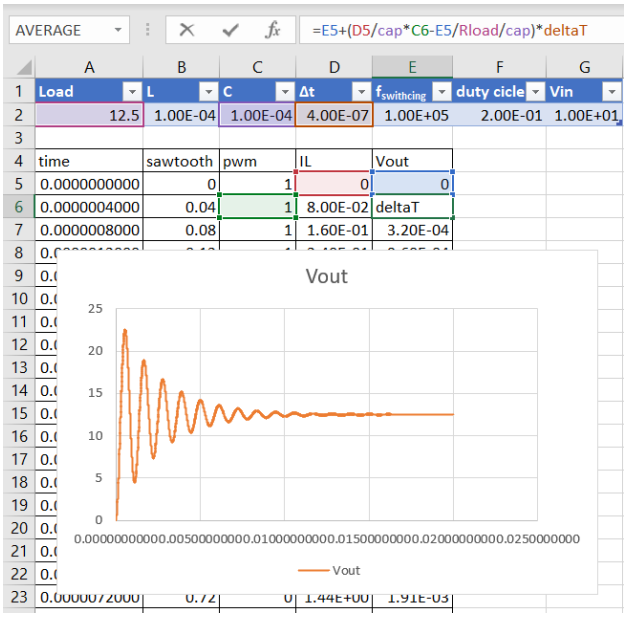

Figure 12. Screen capture of the Excel sheet used for boost power stage simulation

APPENDIX C

Fig. 12. is a screen capture of the Excel Spreadsheet used for simulating the boost power stage. In the second row, the user may enter the boost power stage parameters (inductance, capacitance, load, switching frequency and duty cycle, input voltage) and the simulation step. *Δt*. As the input values were introduced, columns A to E will automatically update, Column A to E represents the discrete-time, sawtooth signal, PWM control signal, *q(t)*, inductor current, and voltage/output current samples.

APPENDIX D

The VHDL module presented in Fig. 13. was written for buck power stage simulation. The buck power stage parameters (*L* – inductance, *C* – capacitance, *Vin* – input voltage, *Rload* – load impedance, *diode_Is* – reverse saturation current of the diode, *diode_N* – nonideality

factor, *deltaT* – simulation time-step) are passed to the module as global (generic) parameters. The module has an input signal, the PWM control signal *q(t)*, and two output signals, the inductor current *iL*, and the capacitor/output voltage *vC*. The thermal voltage *Vt* = 25.69 mV is introduced as a constant, assuming room temperature. The inductor current *iL* and capacitor voltage *vC* are initialized to 0A, respectively 0V. An infinite loop is used to periodically update *iL* and *vC*, and to compute the voltage on the switching diode *vD*, according to ODE system in equation (13).

```
library IEEE;
use IEEE.math_real.all;

entity ideal_asyncronious_buck is
        generic (   L : real;
                    C : real;
                    Vin : in real;
                    Rload : in real;
                    diode_Is : real;
                    diode_N : real;
                    deltaT : time);
        port (      vC : out real := 0.0;
                    iL : out real := 0.0;
                    duty : in real := 0.0);
        end entity;

architecture euler of ideal_asyncronious_buck is
begin

        process
          constant Vt: real := 25.69e-3;
          variable vD: real;
        begin
        ..  iL <= 0.0;
        .  .vC <= 0.0;
        ...while true loop
        ….wait for deltaT;
        ….vD := diode_N * Vt * log((iL + 1.0e-20)/ diode_Is + 1.0);
        ….iL <= maximum(iL + (duty * Vin - (1.0 - duty) * vD - vC)
* real(deltaT / 1 ns) * 1.0e-9 / L, 1.0e-20) ;
        ….vC <= vC + (iL - vC/Rload) * real(deltaT / 1 ns) * 1.0e-9 /
C;
        ..end loop;
        end process;
end architecture;
```

Figure 13. VHDL implementation of the buck-boost power stage simulations

APPENDIX E

The buck power stage was modeled in LTSpice (Fig. 14). The switching components were modeled with ideal switches, including on and off resistances. The simulated diode model was parameterized for ideality factor N=1.752, and saturation current I_s = 2.52 nA. The PWM control signal with a 50% duty cycle was generated using Pulse voltage sources.

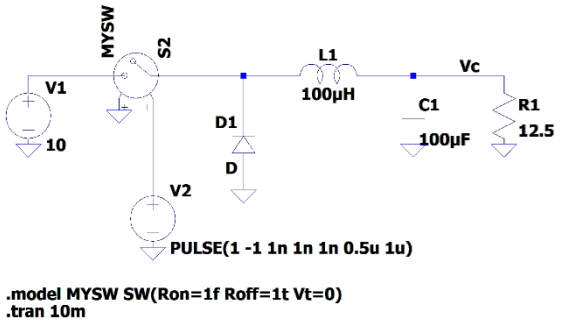

Figure 14. LTSpice model of the buck power stage

REFERENCES

[1] S. Maniktala, “Chapter 1 - The Principles of Switching Power Conversion” in *Switching Power Supplies A – Z (Second Edition)*, Ed.. S. Maniktala, Newnes , 2012, pp. 1–59, ISBN 9780123865335, https://doi.org/10.1016/B978-0-12-386533-5.00001-2.

[2] Y. P. Siwakoti, M. Forouzesh, N. H. Pham, “I Chapter 1 - The Principles of Switching Power Conversion,” in *Control of Power Electronic Converters and Systems*, Ed. F. Blaabjerg, Academic 2018, pp. 3-29 ISBN 9780128052457, https://doi.org/10.1016/B978-0-12-805245-7.00001-9.

[3] D. Naveda-Castillo and L. Adanaque-Infante, "Characterization of DC Converters for Energy Power Systems on Cubesats," *2020 IEEE XXVII International Conference on Electronics, Electrical Engineering and Computing (INTERCON)*, 2020, pp. 1-4, doi: 10.1109/INTERCON50315.2020.9220249

[4] Farzin Asadi; Jerry Hudgins, *Computer Techniques for Dynamic Modeling of DC-DC Power Converters* , Morgan & Claypool, 2018.

[5] R. H. G. Tan and L. Y. H. Hoo, "DC-DC converter modeling and simulation using state space approach," *2015 IEEE Conference on Energy Conversion (CENCON)*, 2015, pp. 42-47, doi: 10.1109/CENCON.2015.7409511.

[6] M. Plesnik, "Use of the State-Space Averaging Technique in Fast Steady-State Simulation Algorithms for Switching Power Converters," *2006 Canadian Conference on Electrical and Computer Engineering*, 2006, pp. 2224-2227, doi: 10.1109/CCECE.2006.277579.

[7] P. Azer and A. Emadi, "Generalized State Space Average Model for Multi-Phase Interleaved Buck, Boost and Buck-Boost DC-DC Converters: Transient, Steady-State and Switching Dynamics," in *IEEE Access*, vol. 8, pp. 77735-77745, 2020, doi: 10.1109/ACCESS.2020.2987277.

[8] S. Laali and H. M. Mahery, "Buck DC-DC converter: Mathematical modeling and transient state analyzes," *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 661-667, doi: 10.1109/PEDG.2012.6254073.

[9] N. L. Celanovic, I. L. Celanovic, Z. R. Ivanovic, "Cyber Physical Systems: A New Approach to Power Electronics Simulation, Control and Testing," Advances in Electrical and Computer Engineering, vol.12, no.1, pp.33-38, 2012, doi:10.4316/AECE.2012.01006

[10] L. Corradini, D. Maksimović, P. Mattavelli, R. Zane, “Digital Control of High-Frequency Switched-Mode Power Converters”, John Wiley & Sons, Inc, 2015, ISBN:9781118935101, DOI:10.1002/9781119025498

[11] D. Price and V. Serrano, "Co-Simulation as a Resource for the Control of a Buck Converter," *2019 7th International Engineering, Sciences and Technology Conference (IESTEC)*, 2019, pp. 550-555, doi: 10.1109/IESTEC46403.2019.00104.
[12] V. Boscaino, G. Capponi, G. M. Di Blasi, P. Livreri and F. Marino, "Modeling and simulation of a digital control design approach for power supply systems," *2006 IEEE Workshops on Computers in Power Electronics*, 2006, pp. 246-249, doi: 10.1109/COMPEL.2006.305638.
[13] P. Zumel, C. Fernandez, M. Sanz, A. Lazaro and A. Barrado, "Step-By-Step Design of an FPGA-Based Digital Compensator for DC/DC Converters Oriented to an Introductory Course," in *IEEE Transactions on Education*, vol. 54, no. 4, pp. 599-609, Nov. 2011, doi: 10.1109/TE.2010.2100397.
[14] N. L. Hinov, V. V. Dimitrov and T. H. Hranov, "Digitization of control systems for power electronic converters," *2020 XXIX International Scientific Conference Electronics (ET)*, 2020, pp. 1-4, doi: 10.1109/ET50336.2020.9238255.
[15] D.F. Griffiths, D.J. Higham, "Euler's Method. In: Numerical Methods for Ordinary Differential Equations" in *Springer Undergraduate Mathematics Series*, Springer, London, 2010, ISBN 978-0-85729-147-9, https://doi.org/10.1007/978-0-85729-148-6_2
[16] A. D. Polyanin and A. V. Manzhirov, "*Handbook of Integral Equations"*, CRC Press, Boca Raton, 1998, ISBN 0-8493-2876-4
[17] Xuelian Zhou and Qiang He, "Modeling and Simulation of Buck-Boost Converter with Voltage Feedback Control", MATEC Web of Conferences, 31 (2015) 10006, DOI: https://doi.org/10.1051/matecconf/20153110006
[18] R. W Erickson., D. Maksimovic, "Fundamentals of Power Electronics", Third Edition, 2020, Springer Nature, ISBN 978-3-030-43881-4, DOI 10.1007/978-0-306-48048-5
[19] J. Corcau and L. Dinca, "Numerical modeling of a Dc to Dc boost converter," 2014 International Conference on Applied and Theoretical Electricity (ICATE), 2014, pp. 1-6, doi: 10.1109/ICATE.2014.6972687.
[20] Sun Quan, Sun Yuan, "Closed-loop Simulation of Buck Converter Based on PSIM", E3S Web Conf. 256 02021 (2021), DOI: 10.1051/e3sconf/202125602021
[21] S. G. Sabiro, "Event-driven (RN) modeling for AMS circuits," Proceedings of the 2013 Forum on specification and Design Languages (FDL), 24-26 September 2013, pp. 1-8., : Paris, France, ISSN: 1636-9874
[22] Arango, E., Ramos-Paja, C.A., Giral, R., Serna, S., Petrone, G. (2011). Modeling and Control of Ćuk Converter Operating in DCM. In: Zhu, M. (eds) Electrical Engineering and Control. Lecture Notes in Electrical Engineering, vol 98. Springer, Berlin, Heidelberg. https://doi.org/10.1007/978-3-642-21765-4_55
[23] V. Eng, U. Pinsopon and C. Bunlaksananusorn, "Modeling of a SEPIC converter operating in Continuous Conduction Mode," 2009 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, 2009, pp. 136-139, doi: 10.1109/ECTICON.2009.5136982.
[24] "Multiphase Buck Converter with TLVR Output Filter", AN_2011_PL12_2012_221647, Infineon Technologies AG, 2021
[25] V. Morais and A. Martins, "Modelling, Analysis and Control of Multiphase Synchronous Buck Converters," Journal of Electrical Systems, vol. 18, (1), pp. 132-149, 2022. Available: https://www.proquest.com/scholarly-journals/modelling-analysis-control-multiphase-synchronous/docview/2644443107/se-2.
[26] Wang P, Liu C, Guo L. Modeling and Simulation of Full-Bridge Series Resonant Converter Based on Generalized State Space Averaging. AMM 2013; 347–350:1828–32. https://doi.org/10.4028/www.scientific.net/amm.347-350.1828.
[27] Marco Antonio Sánchez Vázquez, Ismael Araujo-Vargas, Kevin Cano-Pulido, "Emulator Based on Switching Functions for a Dual Interleaved Buck-Boost Converter", Mathematical Problems in Engineering, vol. 2019, Article ID 5930548, 10 pages, 2019. https://doi.org/10.1155/2019/5930548