NOVEL VOLTAGE-CONTROLLED AMPLIFIERS FOR MULTISTANDARD INTEGRATED RADIO RECEIVERS

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Abstract: This paper proposes a new architecture for transconductance (Gm)-based variable-gain amplifiers (VGA) that is better suited for multi-standard radio receivers than the classical two-Gm structure: its bandwidth and linearity are largely independent of the gain setting and both the gain range and the bandwidth can be programmed through digital controls. Unlike the classical structure - that uses two Gm cells and modifies the gain by changing the transconductance of at least one of them, usually by varying the biasing conditions - the new VGA employs three Gm cells with constant biasing; the gain variation is achieved through a differential current steering scheme. Two transistor-level implementations of the proposed VGA structure are presented, one using simple differential pairs and the other based on a more complex, highly linear Gm cell. New circuits for controlling the output common-mode voltage are proposed for both cases; these circuits do no require the placement of additional circuitry in the differential signal path. The VGAs were designed in a standard 0.18um CMOS technology to same specifications: to cover the gain range of 0dB-18dB while handling signals with amplitudes up to 800mVpkpkdiff without significant distortions; maximum bandwidth above 30MHz while driving 1pF; power consumption bellow 6mW. Simulation results show that both VGAs meet the requirements, thus validating the circuit implementations and proving the potential of the proposed architecture.

Key words: *variable-gain amplifier; transconductor; differential current steering; multi-standard radio receivers.*

I. INTRODUCTION

In recent years there has been considerable interest in the development of multi-standard radio receivers for mobile applications, driven by the commercial race to integrate more and more functions into the mobile phone. Nowadays one can use the mobile phone to listen to FM and DAB radio stations, watch mobile TV, communicate with other wireless devices using the Bluetooth or 802.11 standards and find out the phone location using the GPS system.

Adding new features by pilling up sets of one-operation mode circuitry is not a practical option due to space and cost constraints. Therefore specific architectures for multi-standard radio receivers have been developed, mostly based on programmable and re-configurable blocks, able to meet the various requirements of each standards/type of signal received by switching between their multiple operation modes that are set through digital controls.

Figure 1 presents a typical architecture for multi-band, multi-standard receivers for mobile TV signal, broadcasted using standards such as T-DMB, DVB-H and ISDB-T: it comprises a set of RF front-ends, each of them suited for a particular signal type/broadcast, with the outputs connected to a common base-band/IF analog chain. This way, signals for each standard/band will be picked-up by a specific antenna, amplified by a dedicated low-noise amplifier (LNA), then down-converted by the mixer (MIX) using a programmable frequency from the local oscillator - f_{LO} - from the input frequency – f_{RF} - directly to the baseband (in Zero-IF receivers) or to an intermediary frequency – f_{IF} – (in Low-IF receivers). The baseband/IF signal path is likely to comprise at least the blocks shown in Figure 1 : a programmable-gain amplifier (PGA) provides a coarse control – in steps of a few dB - of the signal amplitude that helps reduce the linearity requirements for the following blocks; a channel filter that realizes the part of the channel selection and image rejection that is done in the analogue domain; a variable-gain amplifier (VGA) able to adapt continuously the amplitude of the signal applied to the analog-to-digital converter (ADC). The more complex signal processing – including demodulation and decoding - is usually performed in the digital domain.

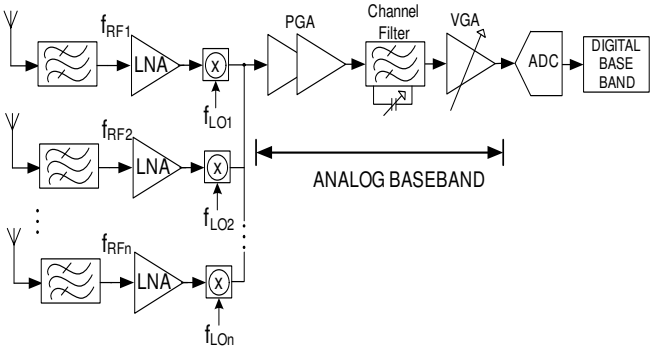

Figure 1. Typical architecture of a multi-standard receiver

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The ability to vary the gain of the RF and analog chains is essential for a radio receiver, as the strength of the signal captured by the antenna can vary over a wider range than is possible/practical to cover by the ADC dynamic range. For example, the DVB-H standard allows for the received signal level to vary between -94.6dBm and -28dBm [1]; at the input of a DAB receiver the signal power can vary from -100dBm to -10dBm. Moreover, the continuous control of signal amplitude provided by the VGA shown in Figure 1 is essential when receiving signals with large peak-to-average ratios, such as the OFDM-broadcasts employed by the mobile TV standards mentioned above.

Besides the usual amplifier parameters - gain range, linearity and noise - there are specific requirements for a VGA: a short and gain-independent settling time – usually achieved by implemented a linear-in-dB gain control characteristic; good linearity over the entire gain range – preferably a constant 1dB output compression point (OCP1dB); no (or very small) variation of the bandwidth and the group delay when the gain changes [2].

Numerous VGA circuits that have been proposed in the literature have closed-loop architectures, using the negative feedback to ensure good linearity. The gain is controlled by modifying the input and/or the feedback resistances [2], [3]. Their bandwidth is usually limited to a few MHz by the rapidly increasing power consumption and stability issues.

Open-loop VGAs based on transconductors (Gm cells) are better suited for applications requiring large bandwidths; however, it is difficult to achieve good linearity and a linear-in-dB gain characteristic. Section II of this paper discusses briefly several classical implementations of such VGA; a novel architecture is presented in Section III, along with a transistor-level implementation based on simple differential pair. A second implementation, based on a high-linearity transconductor, is proposed in Section IV. Both circuits have been designed in a standard 0.13um CMOS process; the simulation results shown in Section V validate the designs and prove the potential of the proposed architecture. Conclusions are drawn in Section VI.

II. CLASSICAL Gm-BASED VGA ARCHITECTURES

The block diagram shown in Figure 2 illustrates a very popular approach to the design of such VGAs [3], [4]: the transconductor Gm_{12} converts the input voltage into a current that is applied to a load resistor implemented by Gm_{56}. The voltage gain is determined by the Gm_{12}/Gm_{56} ratio, it can be varied by modifying one or both transconductances.

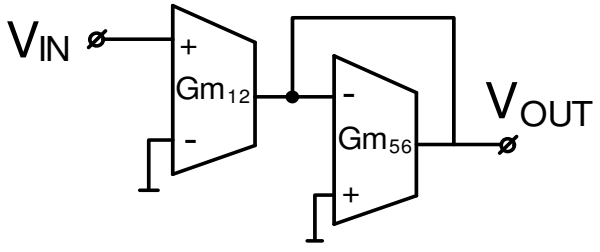

Figure 2. Block diagram of the classical Gm-based VGA

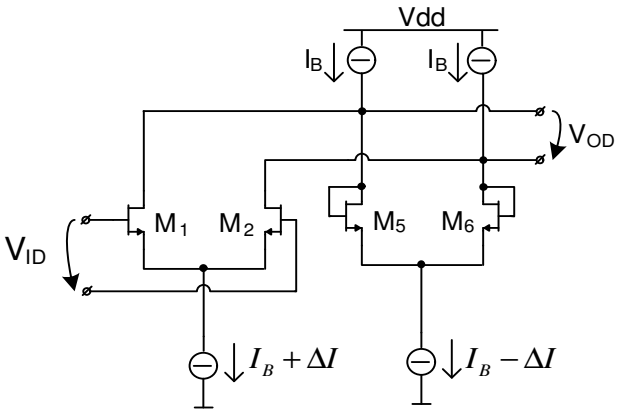

Figure 3. Classical VGA with dB-linear control

Figure 3 presents an implementation example: Gm_{12} and Gm_{56} are realized by simple differential pairs; the voltage gain is controlled by varying the biasing current (hence the transconductance) of both Gm cell with the same quantity – ΔI – in opposite directions; the gain-to-ΔI expression result:

$$A_0 = \frac{Gm_{12}}{Gm_{34}} = K\sqrt{\frac{I_B + \Delta I}{I_B - \Delta I}} = K\sqrt{\frac{1 + \frac{\Delta I}{I_B}}{1 - \frac{\Delta I}{I_B}}} \approx e^{\frac{\Delta I}{I_B}} \quad \text{if} \quad \frac{\Delta I}{I_B} \le 0.6 \tag{1}$$

It can be approximated by an exponential for low $\Delta I/I$ values, hence it provides a dB-linear control of the gain [5].

Of the many limitations of this simple approach two are particularly significant in our case: i). as the output (load) transconductance is modified in order to change the gain, the VGA bandwidth will change, as well; ii). as the bias current is modified in order to vary the transconductance of the differential pairs, the linearity of the Gm cells will also change. The later problem can be avoided by using the current steering technique, that is to steer a part of the signal current provided by the differential pairs away from the output of the transconductor [3].

III. THE PROPOSED VGA ARCHITECTURE

Figure 4 presents the proposed VGA architecture; it employs three Gm cells and a voltage-controlled current amplifier. There are two essential differences between this structure and the classical one shown in Figure 2:

- the transconductances of all the Gm cells are kept constant; this way the linearity will not change with the gain (as a first-order analysis).
- the gain is modified by varying the fraction of the current provided by Gm_{34} that is injected into the VGA output node; this is function is performed by the current amplifier **Aii**; by implementing it using a differential version of the classical current steering technique, the current-current gain Aii can be varied in the range [-1: +1] by modifying the voltage V_{CTRL}.

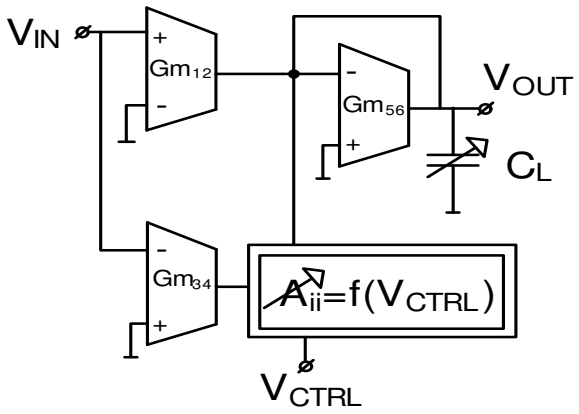

Figure 4. The proposed VGA architecture

The voltage gain expression results:

$$A_v = \frac{Gm_{12} - AiiGm_{34}}{Gm_{56}} \in [\frac{Gm_{12}}{Gm_{56}}(1 \pm \frac{Gm_{34}}{Gm_{12}})] \quad (2)$$

The proposed structure is well suited for multi-standard radio architectures as the one shown in Figure 1:

- the VGA bandwidth is largely independent of the gain setting, as it is determined by the output node impedance, which does not change when the gain is modified. Moreover, the VGA bandwidth can be made programmable, by placing a digitally-controlled capacitive matrix at its output, as suggested in Figure 4 by the variable capacitor C_L.
- the gain range is determined only by the ratio of Gm_{34} and Gm_{12}; therefore it can be modified without affecting the bandwidth.

Therefore both the bandwidth and the gain range can be easily tuned to new values when the receiver changes its operation mode. This feature is important for mobile TV receivers, as the channel bandwidth varies over a wide range: from 430KHz (ISDB-T, 1 segment) to 8MHz (DVB-H, mode 4).

As there are no internal nodes the phase characteristic should be smooth, resulting in relatively small variations of group delay over the operating frequency range.

An implementation of the proposed VGA structure using simple differential pairs is presented in Figure 5. Transconductances Gm_{12}, Gm_{34} and Gm_{56} are realized by the pairs M1-M2, M3-M4 and M5-M6, respectively. The feedback loop closed around Gm_{56} by M_Vcm and Mpcm, Mp5, Mp6 maintains the level of the common-mode output voltage equal to V_{CM}; note that no additional circuitry was used to sense the common-mode level.

Figure 6 presents the schematic of the voltage-controlled current gain cell **Aii**. The two differential pairs with cross-coupled outputs realize a differential current steering circuit: if the control voltage, $V_{CTRL} = V_A - V_B$, has a large positive (negative) value the circular current generated by Gm_{34}, denoted i_{signal} in Figure 6, is routed to the output OutP (OutM); for intermediate values of V_{CTRL} a positive or negative fraction of i_{signal} reaches OutP while the complement is routed to OutM.

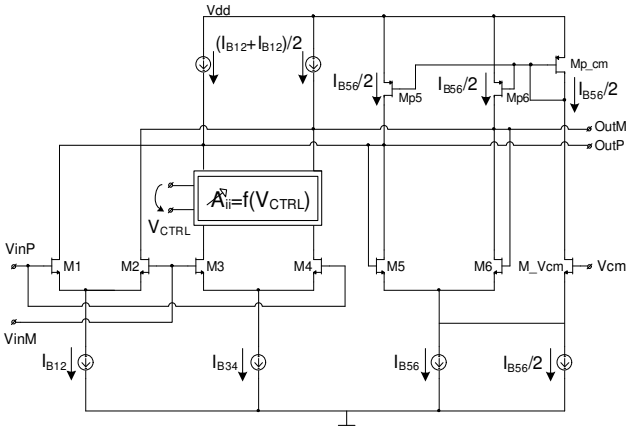

Figure 5. First proposal for VGA implementation

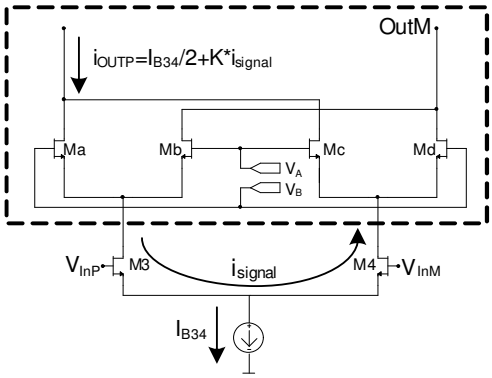

Figure 6. Differential current steering for cell Aii

Note that the DC current sunk from node OutP remains equal to the one sunk from node OutM (and both equal to $I_{B34}/2$), irrespective of V_{CTRL}.

IV. THE PROPOSED VGA IMPLEMENTED WITH HIGH-LINEARITY TRANSCONDUCTORS

The transconductance of the Gm cell shown in Figure 7 is set mainly by the resistors R, as the local feedback loops around the input transistors M1 and M2 increase their effective gm [6]. This arrangement also ensures a very good linearity, largely independent on MOS variations over PVT.

Note that the gate-source voltages of the input transistors are constant, therefore the potential at node M will follow the common-mode voltage at the input of the Gm cell.

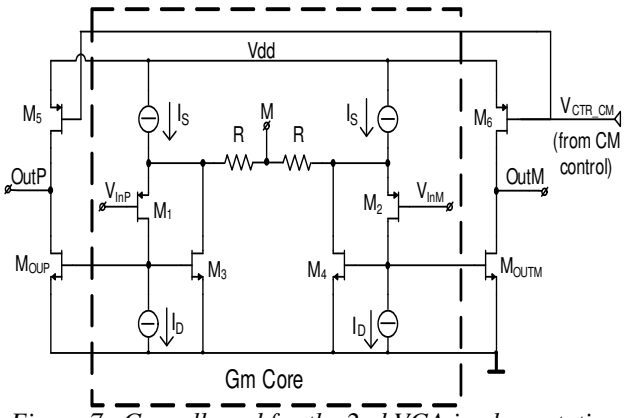

Figure 7. Gm cell used for the 2nd VGA implementation

In numerous Gm-based circuits the output of each transconductor is connected to the input of another one – as it is the case with the proposed VGA structure shown in Figure 4. It follows that the voltage common-mode level at the VGA output can be sensed at node M of Gm_{56}. Figure 8 proposes a circuit for controlling the common-mode output level based on these observations.

The differential current steering technique presented in the previous Section can be used in this case, as well: the simplified schematic is shown in Figure 9. Recently this approach was used to implement an amplifier with a gain varying between -1 and +1, but with the current-steering transistors, M_{11}-M_{14}, operating in weak-inversion [7].

A second implementation of the VGA structure proposed in Figure 4 can be obtained by combining the sub-circuits presented in Figures 8 and 9. The complete schematic cannot be shown here due to space constraints but a simplified schematic is presented in Appendix 1.

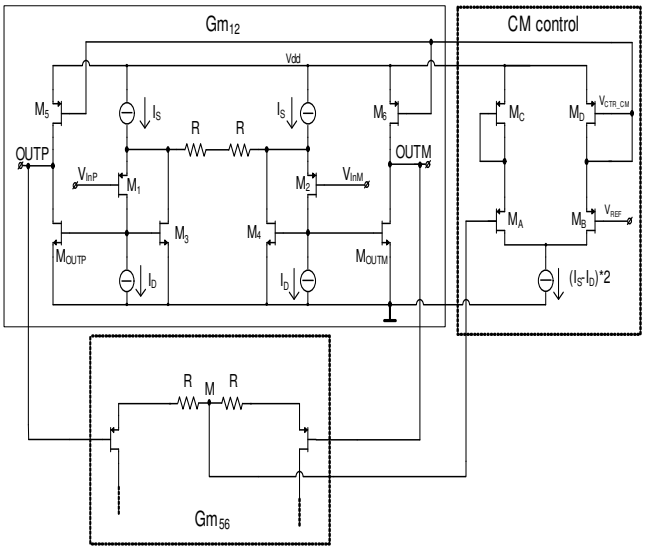

Figure 8. Circuit for controlling the output common-mode voltage of the Gm cell shown in Figure 7 (here the cell called Gm12) when connected to another cell of same type (here the cell called Gm56)

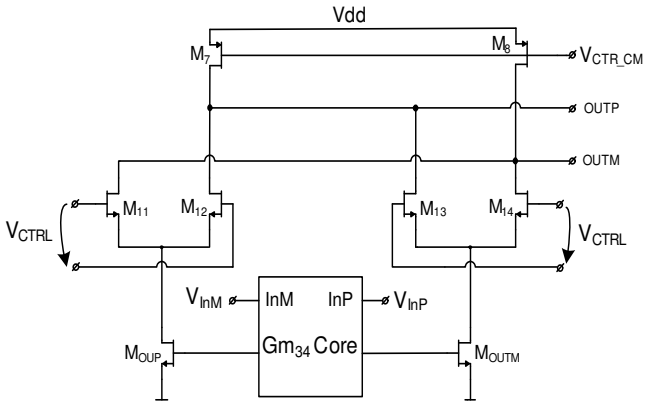

Figure 9. Current steering techniques applied to the Gm cell shown in Figure 7 – here to implement Gm34 and Aii

V. SUMMARY OF SIMULATION RESULTS

The two VGA schematics presented above (Figures 5 & 6 and 8 & 9) have been designed in a standard 0.18um CMOS process, targeting the same set of requirements: to cover the gain range of 0dB to 18dB while handling signals with amplitudes up to $800mV_{pkpkdiff}$ without significant distortions; ensure a bandwidth larger than 30MHz while driving a load of 1pF between each output and GND.

Figures 10 and 11 present the frequency characteristics of the first and second VGA, respectively: for both cases the bandwidth varies very little with the (low-frequency) gain.

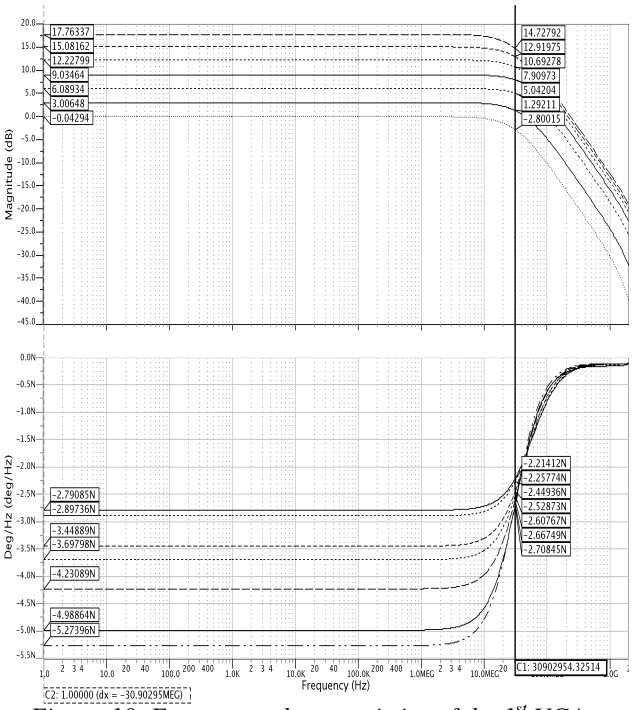

Figure 10. Frequency characteristics of the 1st VGA; top=magnitude; bottom=group delay

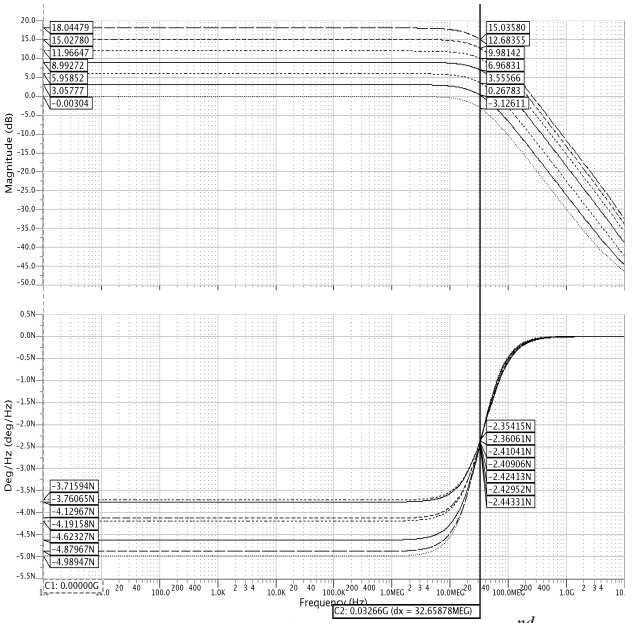

Figure 11. Frequency characteristics of the 2nd VGA

Table 1.Bandwidth and Group Delay variation versus gain

Gain [dB]	BW [MHz]		Δ Group Delay [ns]	
	1st VGA	2nd VGA	1st VGA	2nd VGA
0	31	33	-2.49	-2.44
3	34	44	-2.31	-1.76
6	38	58	-2.096	-1.34
9	42	56	-1.873	-1.38
12	42	46	-1.85	-1.65
15	38	38	-2.05	-2.05
18	32	31	-2.42	-2.61

The bandwidth values for several gain settings are given in Table 1, along with the corresponding group delay variation (calculated as he difference between the group delay value at low-frequency and the value at the -3dB BW.

The Gain-to-V_{CTRL} characteristics of the two VGAs are presented in Figures 12 and 13. One can notice that they are relatively close to the wanted ideal dB-linear curve; the errors can be reduced further by using standard techniques such as pre-distorting V_{CTRL}.

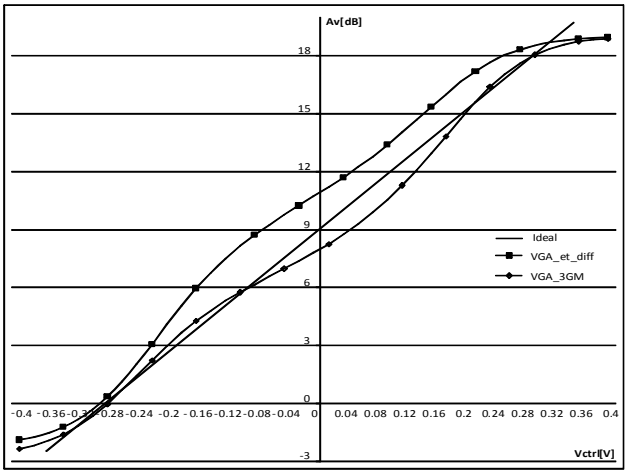

Figure 12. The characteristics "Gain versus control voltage Vctr" for the two VGAs proposed here – with the schematics shown in Figures 5&6 and 8&9

The output voltage that can be handled by the two VGAs while maintaining the THD bellow 1% is given for several gain settings in the first two columns of Table 2. It is worth noting that for both VGAs these values stay within ±10% of their mean value, over the 0dB to 18dB gain range.

The 1dB Output Compression Point values (in $dBV_{pkpkdiff}$) for the same gain settings are given in the last two columns of Table 2. Again, the values stay within a narrow range, one can say that the 1dBOCP is practically constant.

It should be noted that different supply voltages were used: 2.5V for the first VGA (schematic shown in Figures 5 and 6) and 1.8V for the second VGA (schematic shown in Figures 8 and 9).

The power consumptions were also different: 3.7mW for the first VGA and 5.9mW for the second VGA.

Table 2. Maximum output voltage and OCP1dB versus gain

Gain [dB]	Voutmax [mVpkpkdiff] (for THD ≤ 1%)		1dB OCP [dBV_pkpkdiff]	
	1st VGA	2nd VGA	1st VGA	2nd VGA
0	938.06	841.1	0.04	2.01
3	862.94	849.46	-0.21	1.65
6	801.7	853.38	-0.68	1.98
9	802.5	962.24	-0.86	1.69
12	817.04	997.2	-0.81	0.79
15	785.64	1004.36	-0.90	0.55
18	817.96	1041.44	-0.50	0.83

VI. CONCLUSIONS

The trend in nowadays integrated radios is to "minimize" the amount of analog signal processing; the aim is to perform as much of the signal processing as possible in the digital domain, where the design is simpler and more flexible, and can be easily ported from one technology to another, taking full advantage of the continuously shrinking CMOS technologies.

High-performance (bandwidth, resolution and dynamic range) ADCs have been developed in order to quantize the signal as close to antenna as possible. In principle, the analog baseband illustrated in Figure 1 can be removed from the chain if an ADC with high-enough resolution and suitable dynamic range is available. Despite major improvements in ADC performances, such an approach is not possible today and it is unlikely to be a viable option in the near future [8].

Adapting the gain of the RF and analog signal paths in order to absorb most of the input signal amplitude variation remains the most effective solution for optimizing the dynamic range of integrated receivers.

The OFDM signals – which are used intensively in digital radio and TV broadcastings – have a large peak-to-average ratio; also, the decoders are sensitive to large and/or abrupt gain changes. Therefore, it is advantageous to insert a VGA in front of the ADC: the VGA is able to adapt continuously its gain to the signal amplitude, avoiding the transients associated with the step-like modification of the gain performed by the easier-to-design PGAs.

The new VGA architecture proposed in this paper has two significant advantages over the classical structure that makes it better suited for multi-standard radio receivers:
i). the variations of the bandwidth, group delay and linearity-related parameters with the gain setting are relatively small and ii). both the gain range and the bandwidth can be programmed through digital controls.

Two transistor-level implementations of the proposed VGA structure are given in the paper, one using simple differential pairs and the other based on a high-linearity Gm cell. New circuits for controlling the output common-mode

voltage are proposed for both cases; it is worth noting that these circuits do no require the placement of additional circuitry in the differential signal path.

The two VGAs were designed in a standard 0.18um CMOS process. The simulation results presented in the paper show that they cover the gain range of 0dB-18dB while handling signals with amplitudes up to $800mV_{pkpkdiff}$ without significant distortions; they exhibit bandwidths above 30MHz while driving capacitive loads of 1pF between each output and GND. These results validate the designs and prove the potential of the proposed architecture

ACKNOWLEDGEMENT

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APPENDIX 1

The simplified schematic of the second VGA implementation. Among the features not shown here due to space constraints are: the PMOS transistors placed on the top of each output stage for biasing are cascoded, as well as all the constant-current sources that are represented in this schematic by their symbol.