A VLSI IMPLEMENTATION OF A NEW LOW VOLTAGE 5th ORDER DIFFERENTIAL *G_m-C* BESSEL TYPE LOW-PASS FILTER WITH CONSTANT-*G_m* BIASING IN CMOS TECHNOLOGY

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Abstract: In this paper a new low voltage 5th order G_m-C Bessel type low-pass filter (LPF) with constant-G_m biasing, designed using CMOS technology, is presented. The differential LPF is composed of two biquad structures and a first order low-pass filter. The cut-off frequency can be tuned in four steps (42 MHz, 35MHz, 27MHz and 14MHz) by modifying the grounded capacitors values, using digital command logic. In order to maintain the filter transconductance G_m independent of the process, temperature and supply voltage variations, the bias currents used by the proposed structure are made dependent on theses variations, and are given by a constant-G_m biasing source. The proposed structure provides a ±7% corners variation of the cut-off frequency, a dynamic range of 400mV$_{pp(diff)}$, a distortion THD < 1%, and a 12mA current consumption from a 1.8V supply voltage. The simulations performed in 65nm CMOS technology confirm the theoretical results.

Key words: G_m-C filter, biquad, transconductor, OTA, dynamic range, Bessel, CMOS, VLSI.

I. INTRODUCTION

One of a main problems occurring in active filters designing is the fact that the cut-off or centre frequencies are strongly dependent on process, temperature and supply voltage variations [1] – [10].

Another important problem reported in literature is represented by the narrow dynamic range of the input signal for which the circuit works linearly [1] – [13].

In this paper is presented a new low voltage 5th order differential *G_m-C* Bessel type low-pass filter (LPF) with constant-*G_m* biasing, which solves the constraints mentioned above. The LPF has been designed using CMOS technology.

Bessel filters are a variety of linear filters with a maximally flat group delay (linear phase response). They are often used in audio crossover systems. Analog Bessel filters are characterized by almost constant group delay across the entire pass-band, thus preserving the wave shape of filtered signals in the pass-band.

A transfer function **$H(s)$**, at real frequencies, with **$s=j\omega$**, can be written as:

$$H(j\omega) = \left| H(j\omega) \right| \cdot e^{j\theta(\omega)} \qquad (1)$$

where **|$H(j\omega)$| = $G(\omega)$** is the gain-magnitude, or simply the gain, and **$\theta(\omega)$** is the phase.

Phase delay **$Pd(\omega)$** is defined as,

$$Pd(\omega) = -\frac{\theta(\omega)}{\omega} \qquad (2)$$

Group delay **$\tau(\omega)$** is defined as,

$$\tau(\omega) = -\frac{\partial\theta(\omega)}{\partial\omega} \qquad (3)$$

The phase delay **$Pd(\omega)$** from (2) represents the absolute delay, and is of little significance.

The group delay **$\tau(\omega)$** defined in (3) is used as the criterion to evaluate phase nonlinearity.

The group delay is defined as the derivative of the phase with respect to angular frequency and is a measure of the distortion in the signal introduced by phase differences for different frequencies.

A linear phase variation with frequency (over a band of frequencies) implies a constant group delay and no phase distortion in that frequency band.

In order to preserve the integrity of the pulse through a system, it is mandatory that the group delay of the system be constant up to the maximum frequency component of the pulse.

The structure proposed in this paper is attractive for VLSI implementation and offers the possibility of tuning the cut-off frequency and the selectivity, using external biasing currents.

In Section II, the proposed filter topology is presented and analyzed by simulations at the system level. Bode characteristics of the ideal 5th order differential Bessel type LPF and poles distributions in complex plane are shown.

In Section III is presented the proposed transconductor cell with higher dynamic range which is used in 5th order differential Bessel type LPF implementation.

In Section IV the constant-G_m biasing source design is illustrated.

The operation of the proposed structure is presented in Section V by simulations in 65nm CMOS technology.

II. THE 5TH ORDER DIFFERENTIAL G_m-C BESSEL TYPE LOW-PASS FILTER TOPOLOGY

In Fig. 1, the block diagram of the 5th order differential G_m-C Bessel type low-pass filter is shown.

The cut-off frequencies of the 5th order differential G_m-C Bessel type low-pass filter from Fig. 1 can be tuned using different values of the grounded capacitors, in order to obtain the following cut-off frequencies: 42MHz, 35MHz, 27MHz and 14MHz.

To obtain these cut-off frequencies, the poles of the 5th order differential LPF in Bessel approximation need to have the values in Table 1.

Both, the Bode characteristics and poles distribution of the ideal 5th order, Bessel type LPF, for a cut-off frequency of 42MHz are illustrated in Fig. 2 a) and b), respectively.

From Fig. 1, the transfer function of the 5th order differential G_m-C Bessel type low-pass filter can be written:

$$H(s) = \frac{G_m^2/(C_1 C_2)}{s^2 + s\dfrac{G_m}{C_2} + \dfrac{G_m^2}{C_1 C_2}} \cdot \frac{G_m^2/(C_3 C_4)}{s^2 + s\dfrac{G_m}{C_4} + \dfrac{G_m^2}{C_3 C_4}} \cdot \frac{G_m/C_5}{s + \dfrac{G_m}{C_5}} \quad (4)$$
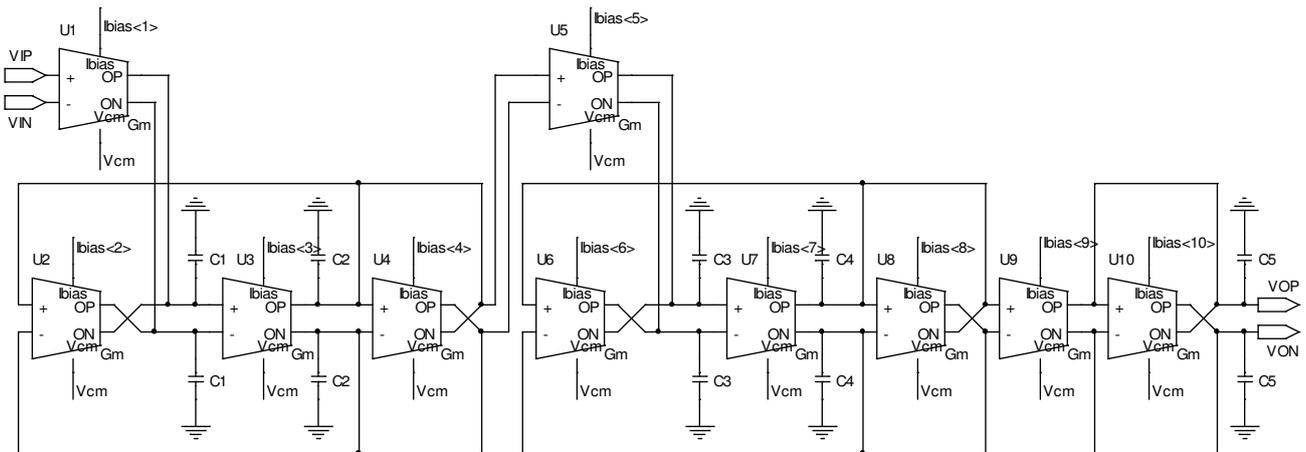

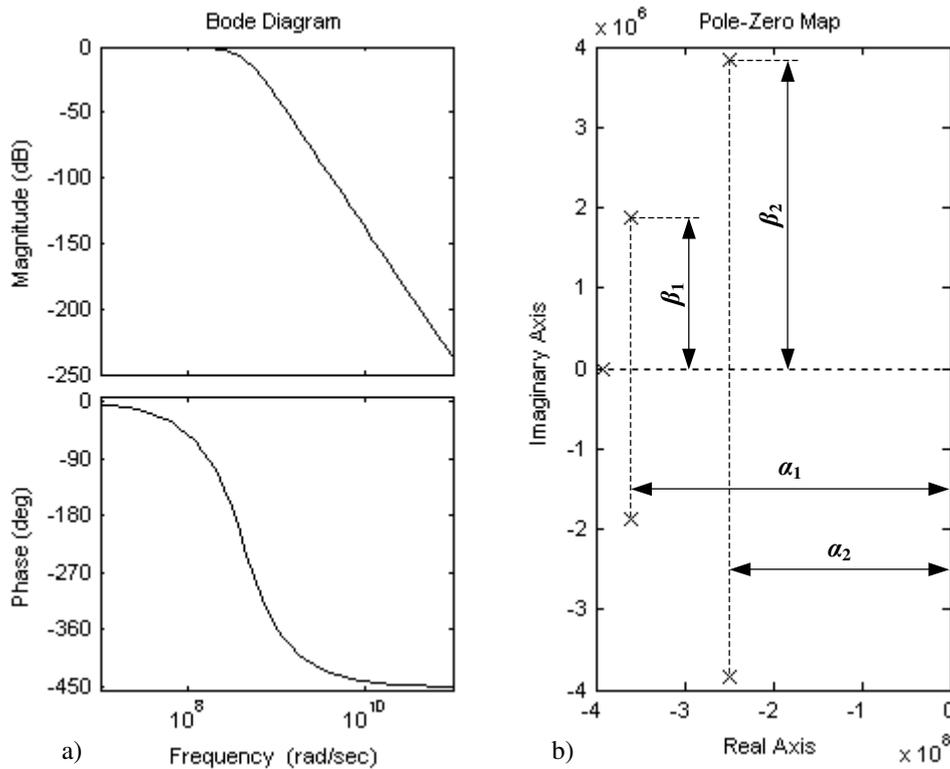*Figure 1. Block diagram of 5th order G_m-C Bessel type low-pass filter*

Figure 2. Bode characteristics of the ideal 5th order Bessel type LPF (a) and poles distribution (b) for a cut-off frequency of 42 MHz

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Table 1. Poles of the 5th order LPF in Bessel approximation depending on cut-off frequencies

Parameter name	Value			
Cut-off frequency (MHz)	14	27	35	42
DC gain	1	1	1	1
Real pole*	-134.491	-261.513	-336.232	-392.270
Intermediate poles*	-123.619±j·64.269	-240.374±j·124.969	-309.053±j·160.675	-360.561±j·187.453
HF poles*	-85.733±j·131.698	-166.706±j·256.083	-214.337±j·329.251	-250.059±j·384.126

*(x10^6 rad/s)

From the poles distribution in complex plane, illustrated in Fig. 2.b), the poles of the 5th order differential G_m-C Bessel type low-pass filter, having the transfer function presented in equation (4), can be deduced as follows:

$$\begin{cases} p_{1,2} = \alpha_1 \pm j\beta_1 \\ p_{3,4} = \alpha_2 \pm j\beta_2 \\ p_5 = \alpha_3 \end{cases} \qquad (5)$$

Using the poles values in Bessel approximation, given by equations (5), in the denominator of LPF transfer function from equation (4), then by terms identification, the grounded capacitor values can be obtained:

$$\begin{cases} C_1 = -\dfrac{2\alpha_1 \cdot G_m}{\alpha_1^2 + \beta_1^2} \\ C_2 = -\dfrac{G_m}{2\alpha_1} \\ C_3 = -\dfrac{2\alpha_2 \cdot G_m}{\alpha_2^2 + \beta_2^2} \\ C_4 = -\dfrac{G_m}{2\alpha_2} \\ C_5 = -\dfrac{G_m}{\alpha_3} \end{cases} \qquad (6)$$

Knowing the poles values of the 5th order differential G_m-C LPF in Bessel approximation, given by (α_1, β_1), (α_2, β_2) and α_3 in equations (5) and Fig. 2.b), and choosing an appropriate value for differential transconductance G_m in Fig. 1 (i.e. $G_m = 1mS$), the values of the grounded capacitors dependent on cut-off frequencies are presented in Table 2. The capacitors used (nMOS in nwell process) are provided by the technology. They are implemented on the base of nMOS transistors, having the capacitance value dependent on the aspect ratio (W/L) of the transistor.

Table 2. Grounded capacitors depending on cut-off frequencies of the 5th order G_m-C Bessel type low-pass filter

C / Freq	C_1 [pF]	C_2 [pF]	C_3 [pF]	C_4 [pF]	C_5 [pF]
42 MHz	4	1.27	2.19	1.84	2.34
35 MHz	4.67	1.48	2.54	2.14	2.72
27 MHz	6.04	1.91	3.29	2.76	3.52
14 MHz	11.66	3.7	6.36	5.34	6.81

The G_m transconductor shown in block diagram from Fig. 1 can be implemented using a differential operational transconductance amplifier (OTA) designed for an extended dynamic range linear operation.

In Section III, the complete analysis of this transconductor is presented.

In order to maintain the filter transconductances, G_m in Fig. 1 independent of process, temperature and supply voltage variations, the bias currents used by the proposed structure have to be dependent of theses variations, and can be obtained by using a constant-G_m biasing source.

In Section IV, the design of this constant-G_m biasing source is presented.

III. IMPLEMENTATION OF THE G_m TRANSCONDUCTOR AT THE CIRCUIT LEVEL

In Fig. 3 is presented the electric scheme of the G_m transconductor.

The proposed G_m transconductor in Fig. 3 is formed by a differential pair implemented with M_1 and M_2 transistors and a common mode feedback (CMFB) loop represented by $M_3 - M_6$ transistors.

The linearity of the proposed transconductor can be sensitively improved by using a topology with M_9 and M_{10} transistors [2].

For the transconductor illustrated in Fig. 3, the classic resistive degeneration has been replaced by MOSFET transistors M_9 and M_{10} operating in deep triode region.

For this structure, M_9 and M_{10} are in deep triode region if $V_{in} = 0$. As the gate voltage of M_1 becomes more positive than the gate voltage of M_2, transistor M_9 stays in the triode region because $V_{D9} = V_{G9} - V_{GS1}$ whereas M_{10} eventually enters the saturation region because its drain voltage rises and its gate and source voltage fall.

Thus, the circuit remains relatively linear even if one degeneration device goes into saturation.

For the widest linear region it is suggested in [9] that:

$$\left(\frac{W}{L}\right)_{1,2} \approx 7 \left(\frac{W}{L}\right)_{9,10} \qquad (7)$$

IV. CONSTANT-G_m BIASING SOURCE DESIGN

For the proposed G_m-C architecture in Fig. 1 it is desirable to bias the transconductor transistors such that their transconductances do not depend on the temperature, process, or supply voltage.

In Fig. 4 a constant-G_m biasing source is presented [2].

If we note with I_{REF} the reference current through the M_1 transistor, the operation of the circuit in Fig. 4 requires that:

$$I_{out} = I_{REF} \qquad (8)$$

because the pMOS transistors M_3 and M_4 are identical size.
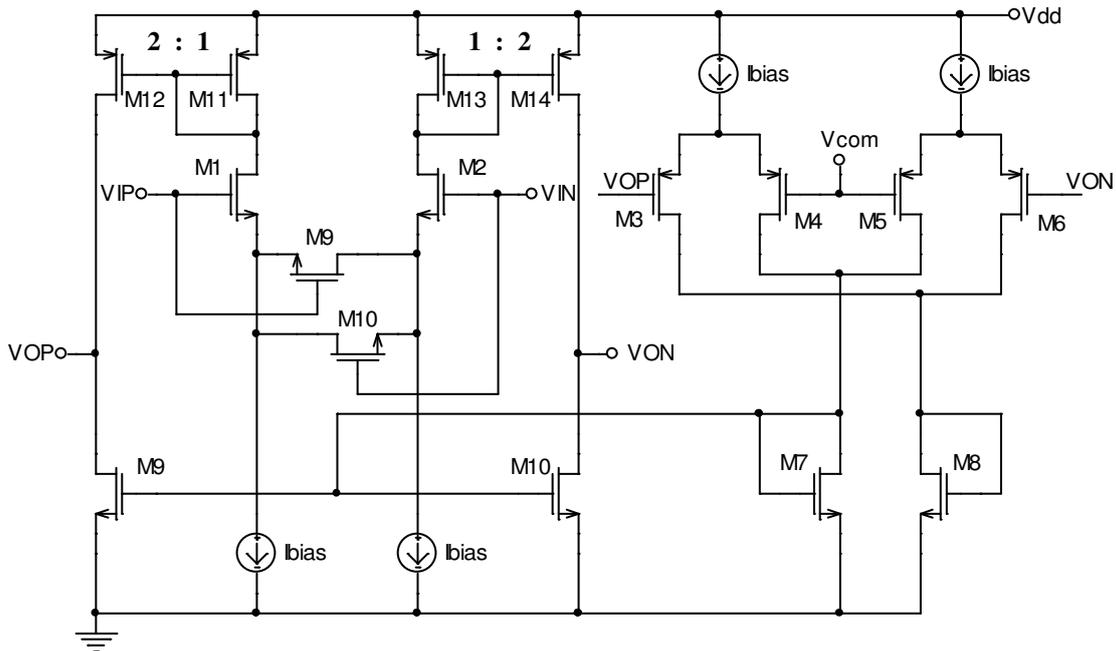
Figure 3. Electric scheme of the transconductor from G_m-C filter

For the circuit in Fig. 4, we can write:

$$V_{GS1} = V_{GS2} + I_{D2}R_S \qquad (9)$$

where V_{GS1} and V_{GS2} are the gate-source voltages of the transistors M_1 and M_2, respectively; I_{D2} is the drain current of M_2 transistor, and equals I_{out}.

The drain currents through M_1 and M_2 transistors can be written as:

$$\begin{cases} I_{D1} = \dfrac{1}{2}\mu_n C_{oc}\left(\dfrac{W}{L}\right)_N (V_{GS1} - V_{TH1})^2 \\[2mm] I_{D2} = \dfrac{1}{2}\mu_n C_{oc} K\left(\dfrac{W}{L}\right)_N (V_{GS2} - V_{TH2})^2 \end{cases} \qquad (10)$$

where K is the ratio between the aspect ratios of the transistors M_2 and M_1.

Using V_{GS1} and V_{GS2} from equations (10) in equation (9), and neglecting body effect, we have:

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2 \qquad (11)$$

As expected, the current is independent of the supply voltage (but still a function of process and temperature).

The assumption $V_{TH1} = V_{TH2}$ introduces some error in the foregoing calculations because the sources of M_1 and M_2 are at different voltages.

The circuit of Fig. 4 exhibits little supply dependence if channel-length modulation is negligible. For this reason, relatively long channels are used for all of the transistors in the circuit.

Thus, the transconductance of M_1 equals:

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_{D1}} \qquad (12)$$

where $I_{D1} = I_{REF} = I_{out}$ is the bias current of M_1 transistor. Using (11) in equation (12), the transconductance of M_1 becomes:

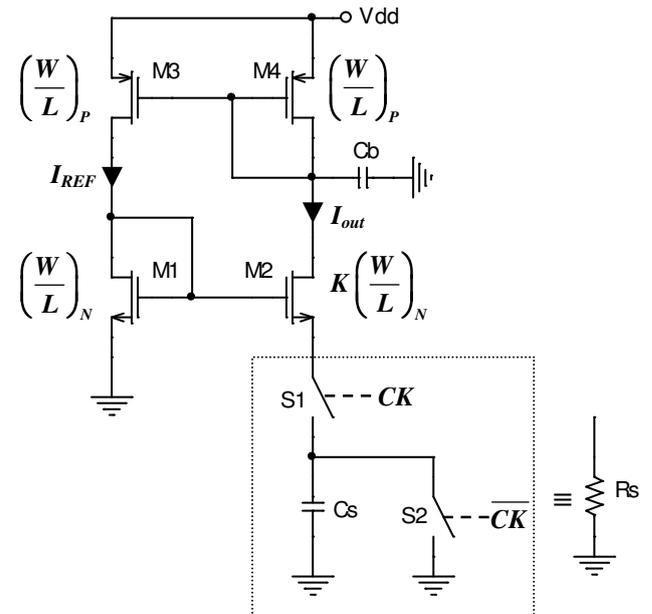$$g_{m1} = \frac{2}{R_S}\left(1 - \frac{1}{\sqrt{K}}\right) \qquad (13)$$

Figure 4. Constant-G_m biasing by means of a switched-capacitor "resistor"

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a value independent of the supply voltage and MOS device parameters.

In reality, the value of R_S in (13) does vary with temperature and process. If the temperature coefficient of the resistor is known, bandgap and proportional to absolute temperature (PTAT) reference generation techniques can be utilized to cancel the temperature dependence. Process variations, however, limit the accuracy with which g_{m1} is defined.

If a precise clock frequency (f_{ck}) is available in the system, the fixed resistor used in a constant-G_m biasing source can be replaced by a switched-capacitor equivalent (Fig. 4) to achieve a higher accuracy.

The value of the equivalent resistor is given by the following equation:

$$R_S = \frac{1}{f_{ck} C_S} \qquad (14)$$

where f_{ck} is the clock frequency and C_S the total capacitance. Capacitor C_B is added to shunt the high-frequency components resulting from switching to ground. Since the absolute value of the capacitor is typically more tightly controlled and since the temperature coefficient of capacitors is much smaller than that of resistors, this technique provides a higher reproducibility in the bias current and transconductance.

In order to obtain the maximum value of the bias current ($I_{bias} = 200\mu A$) for the G_m-C filter from Fig. 1, in the circuit in Fig. 4, according to equation (11), a resistor $R_S = 1k\Omega$ is needed. For this resistor value and using a clock frequency $f_{ck} = 50MHz$, according to equation (14), the value of the total capacitance is $C_S = 20pF$.

An important design problem of the circuit in Fig. 4 is that the ripple provided by the switching cannot be canceled completely.

In order to solve this problem, two identical constant-G_m biasing sources, having the two switched-capacitor resistors commanded with anti-phase clocks are used, in order to diminish the current ripple provided by the switched-capacitor resistor. This idea is shown in Fig. 5.

For this circuit, the output current is twice as high as that in the case illustrated in Fig. 4, and can be written as:

$$I_{out} = \frac{4}{\mu_n C_{ox} (W/L)_N} \cdot \frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \qquad (15)$$

V. SIMULATION RESULTS

The operation of the proposed 5th order differential G_m-C Bessel type low-pass filter is analyzed by simulation in different critical corners, in order to show that its cut-off frequency is independent of process, temperature and supply voltage variations.

The proposed circuit has been analyzed by simulation in a 65nm CMOS technology by using an input signal of $400mV_{pp(diff)}$ and 1.8V supply voltage.

First, the operation of the proposed transconductor cell (G_m-cell) in Fig. 3 is analyzed.

In both Figs. 6 and 7, differential output currents and voltages dependent on input voltage of the G_m-cell, for a unitary voltage gain and for $I_{bias} = 80\mu A$ are shown.

In Fig. 8 is presented the differential transconductance dependent on input voltage for a unitary voltage gain and for $I_{bias} = 80\mu A$. From this dc simulation a value of the differential transconductance $G_m = 1mS$ is obtained. The dynamic range of the input signal for which the circuit transconductor operates linearly is about $400mV_{pp(diff)}$. The dynamic range represents the range values of the input signal for which the transconductance value is constant and independent of the input voltage with an error $\varepsilon \leq 1\%$.

In Fig. 9 the differential voltage gain dependent on the input voltage of the G_m for $I_{bias}=80\mu A$ is presented.
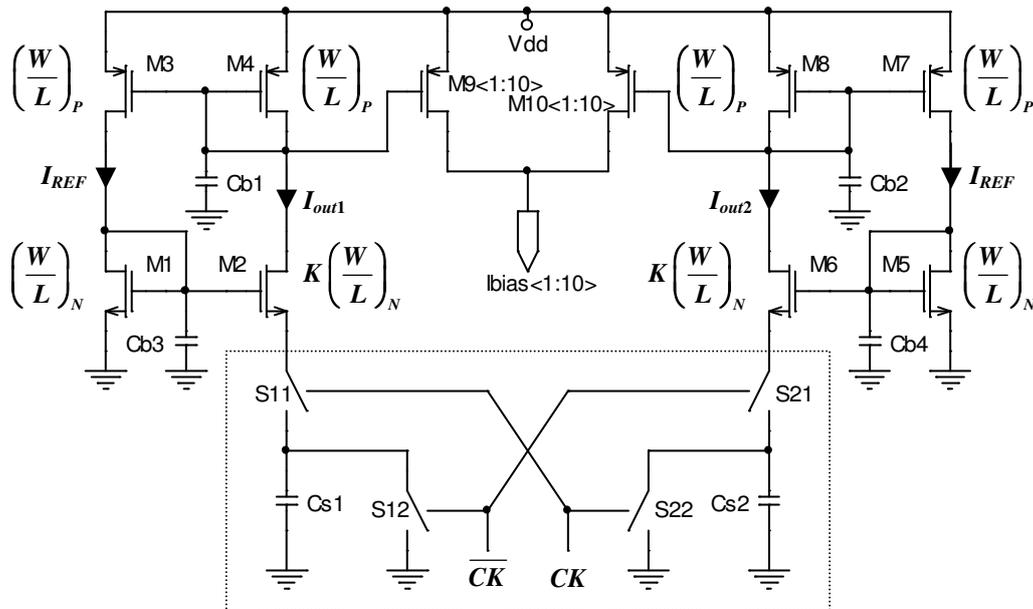

Figure 5. Constant-G_m biasing by means of two identical constant-G_m biasing sources, having the two switched-capacitor resistors commanded with anti-phase clocks
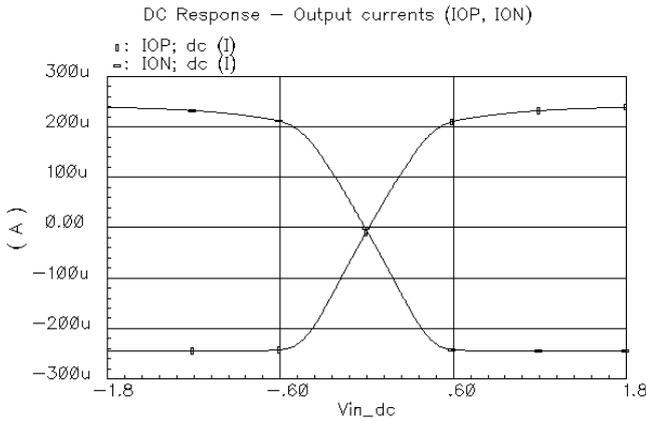
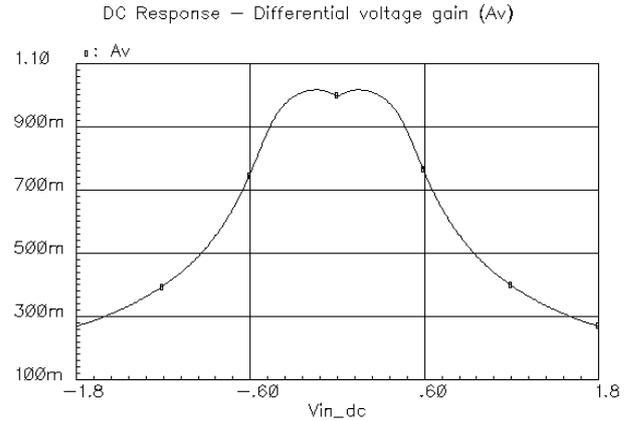*Figure 6. Differential output currents of the G_m-cell for a unitary voltage gain ($I_{bias}=80\mu A$)*

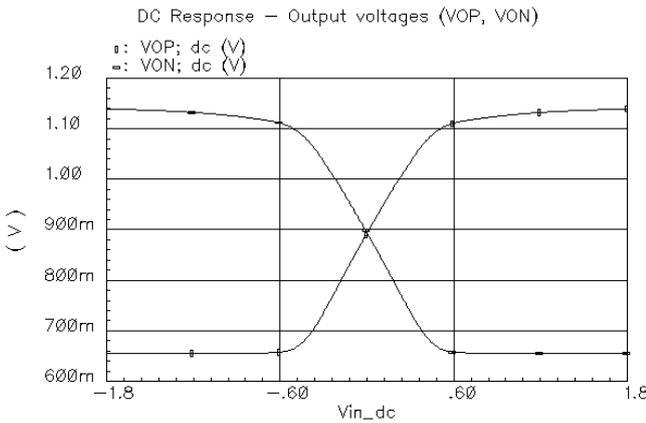*Figure 9. Differential voltage gain of the G_m-cell ($I_{bias}=80\mu A$)*

Figure 7. Differential output voltages of the G_m-cell for a unitary voltage gain ($I_{bias}=80\mu A$)
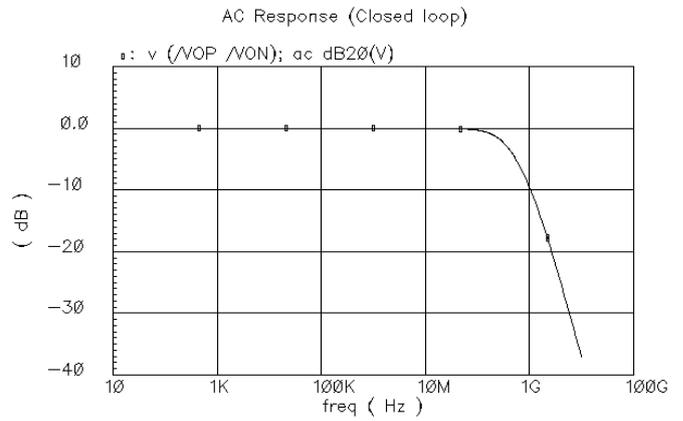

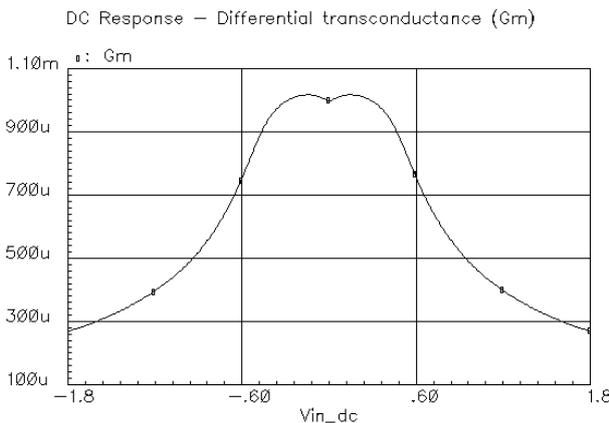*Figure 10. AC frequency response of the G_m-cell in closed loop (unitary voltage gain) ($I_{bias}=80\mu A$)*

Figure 8. Differential transconductance for a unitary voltage gain ($I_{bias}=80\mu A$)
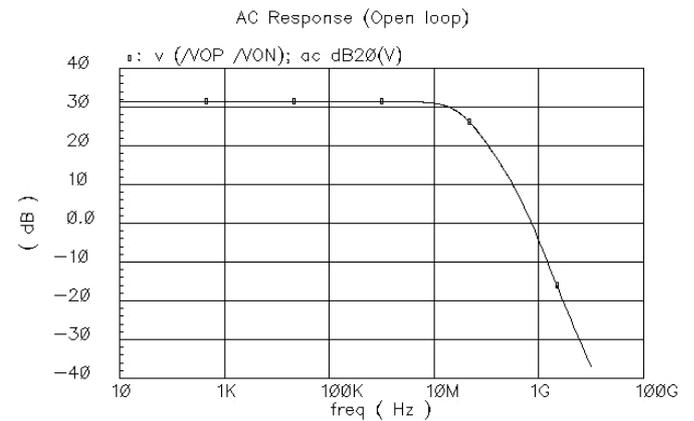

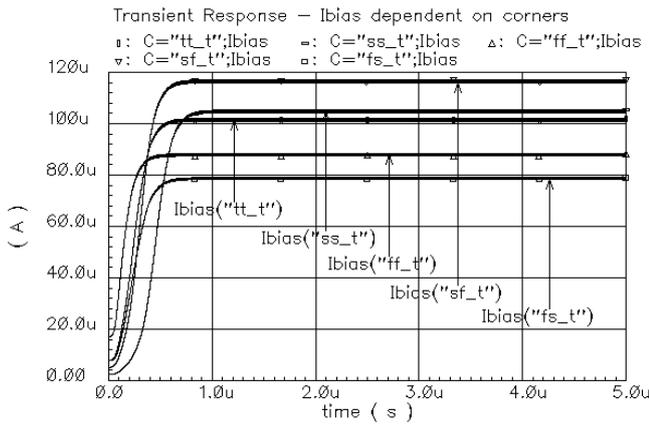*Figure 11. AC frequency response of the G_m-cell in open loop ($I_{bias}=80\mu A$, $R_{load} = 1M\Omega$)*

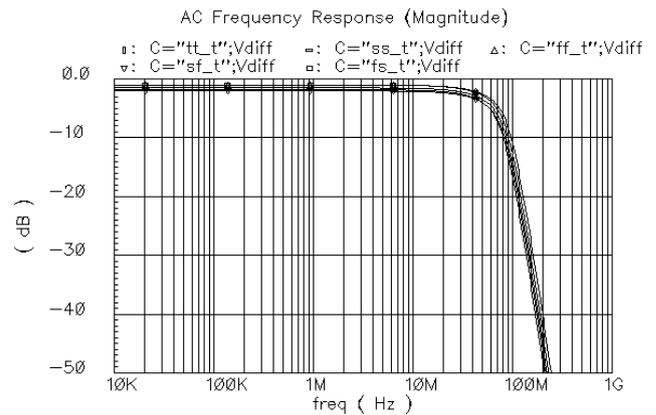*Figure 12. Bias currents I_{bias} depending on corners*

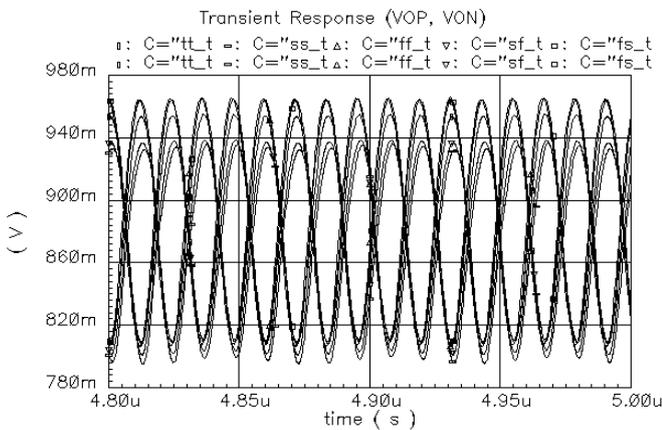*Figure 15. AC frequency response (magnitude) of the proposed LPF depending on corners*

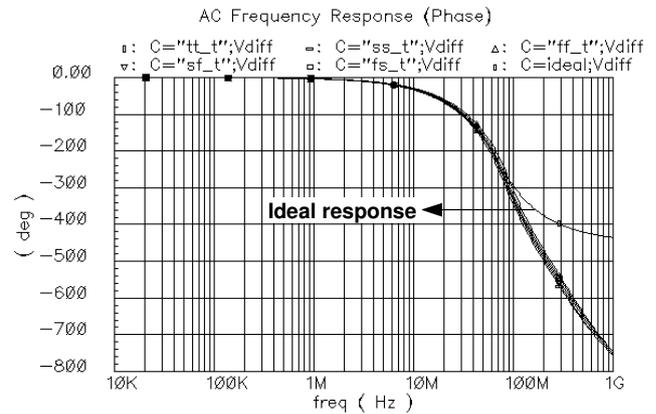*Figure 13. Differential output voltages of the proposed LPF depending on corners*

Figure 16. AC frequency response (phase) of the proposed LPF depending on corners
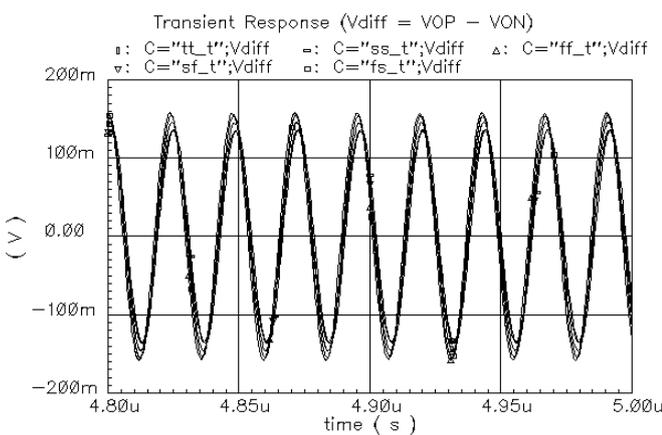

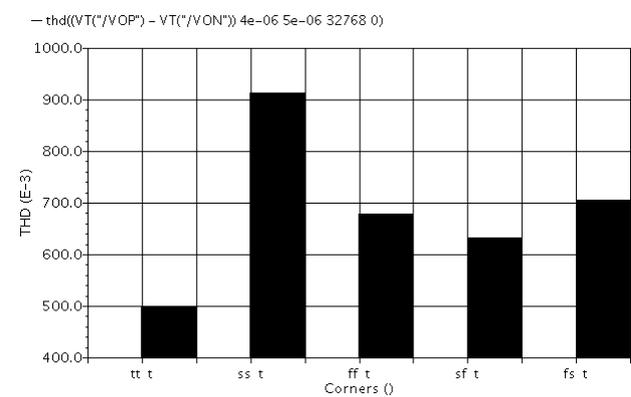*Figure 14. Differential output voltage of the proposed LPF depending on corners*

Figure 17. THD of the differential output voltage of the proposed LPF depending on corners

In Fig. 10 is shown the AC frequency response of the G_m-cell in closed loop operation (unitary voltage gain) for I_{bias}=**80µA**.

In Fig. 11 the AC frequency response of the G_m-cell in open loop for I_{bias}=**80µA** is presented. The gain of the proposed transconductor is about 32dB.

Next, the transient simulation of the proposed 5th order differential G_m-C Bessel type low-pass filter in Fig. 1 with constant-G_m biasing circuit from Fig. 5 is performed in all corners in order to determine the bias currents values dependent on process, temperature and supply voltage variations. These bias currents are presented in Fig. 12 and their values depending on corners are shown in Table 3.

Table 3. Bias currents provided by constant-G_m biasing source in Fig. 5 depending on critical corners

Process, Temperature, Supply voltage	Output current provided by constant-G_m biasing source [µA]
tt_t, 75°, PS=1.8V	101.5
ss_t, 125°, PS=1.62V	104.8
ff_t, 0°, PS=1.98V	87.8
sf_t, 125°, PS=1.62V	116.5
fs_t, 0°, PS=1.98V	78.6

In Fig. 13 are presented the differential output voltages of the proposed LPF in Fig. 1 depending on corners. From these simulations a corners variation of the common-mode voltage between (870 – 910) mV is obtained.

In Fig. 14 the differential output voltage of the proposed LPF in Fig. 1 depending on corners are presented. A very small variation of these waveforms have been obtained.

Next, using the corners dependent bias currents from Table 3, the AC simulation of the 5th order differential G_m-C Bessel type low-pass filter in Fig. 1 is done, using the grounded capacitor values illustrated in Table 2.

In Figs. 15 and 16 the small signal frequency response (magnitude and phase versus frequency) of the proposed 5th order differential G_m-C Bessel type low-pass filter in Fig. 1, for cut-off frequencies of 42MHz are presented by AC simulations performed in all critical corners illustrated in Table 3.

In order to validate the Bessel type characteristics, the Bode characteristics provided by the proposed LPF (shown in Figs. 15 and 16) are compared with the ideal Bode characteristics given by the ideal 5th order differential G_m-C Bessel type low-pass filter (shown in Fig. 2), implemented at the system level. From Figs. 15 and 16 we can see that a magnitude and phase responses of the proposed LPF are very closed to the ideal ones in Fig. 2.a).

According to these simulations results, the 5th order differential G_m-C Bessel type low-pass filter provides a ±7% corners variation of the cut-off frequency.

In Fig. 17, the THD values of the differential output signal of the proposed 5th order differential G_m-C Bessel type low-pass filter in Fig. 1, for a 42MHz cut-off frequency are presented by transient simulations performed in all critical corners. From these simulations a ***THD ≤ 1%*** have been obtained for all corners and cut-off frequencies imposed by design conditions.

The simulations performed in a 65nm CMOS technology confirm the theoretic results.

6. CONCLUDING REMARKS

In this paper a new low voltage 5th order differential G_m-C Bessel type low-pass filter with constant-G_m biasing source has been presented.

The proposed architecture provides a cut-off frequency independent of process, temperature or supply voltage variations. This is done by keeping the filter transconductances G_m independent of these variations.

In order to maintain the filter transconductance G_m independent of the process, temperature and supply voltage variations, the bias currents are provided by two identical constant-G_m biasing sources, having the two switched-capacitor resistors commanded with anti-phase clocks. In this way the current ripple provided by the switched-capacitor resistor can be neglected.

The proposed structure provides a ±7% corners variation of the cut-off frequency, a dynamic range of 400mV$_{pp(diff)}$, distortion THD<1%, and a 12mA current consumption from the 1.8V supply voltage.

The simulations performed in a 65nm CMOS technology confirm the theoretical results.

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