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BANDGAP VOLTAGE REFERENCES BASED ON F-F^{-1} FUNCTIONS

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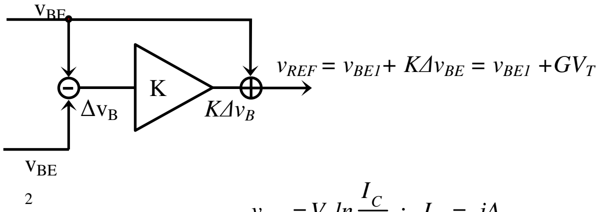
Abstract: We propose in this paper a bandgap voltage reference (BVR) structure based on a class of circuits belonging to ELIN design. F-F^{-1} amplifiers were used for this purpose. They have the advantage of simplicity, a natural nonlinearity compensation and offer possibility to be current controlled or tuned so they do not need resistors as usually bandgap references do. One of the two BVR schematics resulted from the general structure is a simplified variant of a reconfigurable BVR proposed in literature. The second resulted and proposed variant is a new one. Simulations proved the functionality and validity of this general structure and BVR unconventional variants.

Keywords: *Bandgap voltage references, ELIN design, F-F^{1} functions*

I. INTRODUCTION

Bandgap voltage references (BVRs) are among the most important building blocks widely used in integrated circuits. They provide an output voltage that is independent of temperature and power supply. BVRs are needed in many integrated chips such as voltage regulators, data converters, memories, sensors and generally in any power management systems. In a bandgap reference, two voltages having equal but opposite temperature coefficients are added to give the independence of temperature.



$$v_{BE} = V_T ln\frac{I_C}{I_S}\ ;\ \ I_S = jA$$

$$If\ v_{BE} \cong 0.6V\ ;\ \ V_T \cong 26mV\ ;\ \frac{\partial v_{BE}}{\partial \theta} \cong -2\frac{mV}{^{o}C};\ \ \frac{\partial v_{REF}}{\partial \theta} = 0$$

$$\Rightarrow G = 24;$$

$$\Rightarrow v_{REF} \cong 1.2V$$

Figure 1. *Principle block-diagram of a bandgap reference*

Traditionally, one of the term is of v_{BE} type and the other a multiplied ΔV_{BE}. Each of these components is of about 0.6V so that the reference voltage is about 1.2V, close to the bandgap voltage of Silicon [1][2][3]. The principle is shown in *Figure* 1. In CMOS technology, one uses the base-emitter voltage of a diode-connected parasitic vertical BJ transistor formed in p- or n- well.

Other principles are based on MOSFET threshold or gate-source voltage difference across a resistor or using both enhanced and depleted mode MOS transistors or with different gate impurities concentrations[1]. In all of these realizations, the multiplied voltage difference is usually adjusted by trimming the ratio of two resistors. In standard CMOS digital technologies, these resistors could occupy large areas or need an extra mask that increase the cost of fabrication [4]. A circuit configuration without resistors could be a good alternative for a BVR. We present in this paper a general building block for bandgap references that does not need resistors. It is based on the inverse function technique and includes a variant presented in [4] but also opens way to other new circuit configurations. Such a new resulted circuit is presented as an example. In the second section of this paper, the general building block of BVRs without resistors is presented. Section three and four deals with two variants resulted from the building block. The validity of the presented model and derived schematics is proved by simulations. Conclusions and remarks are drawn in section five.

II. A NEW BANDGAP VOLTAGE REFERENCE STRUCTURE

We can notice in *Figure* 1 that two main building blocks are needed: an element which realizes the difference between two v_{BE} type voltages and an amplifier to realize gain G.

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Traditionally, the amplifier is based on an OpAmp with negative feedback and G is adjusted by resistors.

In externally linear internally nonlinear (ELIN) design [5], very popular are nonlinear transconductors described by a nonlinear F function:

$$i_{out} = I \cdot F\left(\frac{v_{in}}{V}\right) \tag{1}$$

where I and V are reference or scaling factors having current and voltage unities respectively. Multipliers, current or voltage controlled amplifiers based only on F and F^{-1} blocks also belong to this design[6]. They have the advantage of simplicity because they do not need extra circuits for linearization. In this way these modules are very useful in VLSI design[6]. In this paper we propose to use such F - F^{-1} amplifiers to implement the BVR model. With this type of amplifiers realized with transconductors, the model from *Figure* 1 could have the general building block in *Figure* 2.

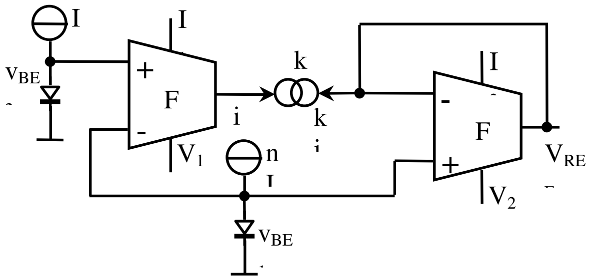


Figure 2. *BVR F-F^{-1} structure*

The difference of the base-emitter voltages of two diode connected transistors having equal areas A_1=A_2 resulting in the same BE saturation curents I_{s1}=I_{s2}, has the form:

$$\Delta v_{BE} = v_{BE1} - v_{BE2} = V_T ln \frac{I_1}{A_1} \cdot \frac{A_2}{I_2} = V_T lnn; \tag{2}$$

This voltage is applied at the input of an F transconductor described by relation (1). The second transconductor is connected to satisfy an inverse function F^{-1} of the form:

$$v_{out} = V \cdot F^{-1}\left(\frac{i_{in}}{I}\right) \tag{3}$$

A current mirror can introduce a gain component k or only contribute to current inversion if this one is needed.

Both building blocks in *Figure* 2 can be described by the following relationships:

$$k \cdot i = I_2 F\left(\frac{v_{BE1} - V_{REF}}{V_2}\right) \tag{4}$$

$$i = I_1 F\left(\frac{v_{BE2} - v_{BE1}}{V_1}\right) \tag{5}$$

Considering the following condition between current scaling factors

$$I_2 = k \cdot I_1 \tag{6}$$

where k is a positive scaling factor.

results in a linear expression for the reference voltage:

$$V_{REF} = v_{BE1} + k\left(v_{BE1} - v_{BE2}\right); \tag{7}$$

$$\text{or } V_{REF} = v_{BE1} + \left(\frac{V_2}{V_1} lnn\right) V_T = v_{BE1} + G \times V_T \tag{8}$$

Relation (7) with requirement (6) is valide for any kind of continuous function F. If for linear functions F and also for some particular nonlinear functions condition (4) is not fulfilled, a linear output may result but, in such cases, extra terms like offsets can appear.

With $dv_{BE} / d\theta \cong -2mV / °C$ and $V_T \cong 26mV$, the condition to have no temperature variations of V_{REF} is $G \cong 24$ [3]. This results also in $V_{REF} \cong 1.2V$.

III. EXAMPLES OF BANDGAP REFERENCES DERIVED FROM THE PROPOSED BUILDING BLOCK DIAGRAM

a) *BVR with source coupled transistor pairs*

Function F can be implemented with a source coupled pMOS transistor pair and the circuit corresponding to the model in *Figure* 2 is drawn in *Figure* 3. In this case transconductor F is described by relation (9) with notations in (10):

$$\frac{i_o}{I} = F\left(\frac{v_{ID}}{V}\right) = \frac{v_{ID}}{V}\sqrt{2 - \left(\frac{v_{ID}}{V}\right)^2}; \quad \left|v_I\right| < \sqrt{2}V \tag{9}$$

$$v_{ID} = v_I^+ - v_I^-; \quad I = I_T; \quad V = \sqrt{\frac{I_T}{\beta}}; \quad \beta = \frac{K_p W}{2L} \tag{10}$$

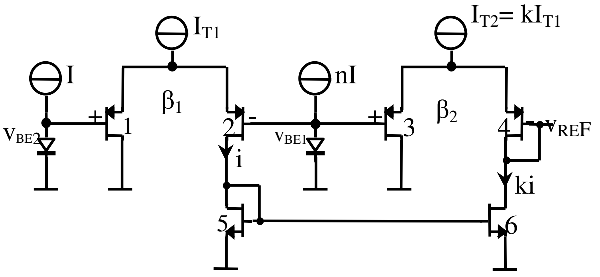


Figure 3. *BVR with source coupled PMOSFET pairs*

Taking into account the output voltage from (8) will result in:

$$v_o = v_{BE1} + \sqrt{\frac{I_{T2}}{\beta_2}\frac{\beta_1}{I_{T1}}} \cdot lnn \cdot V_T \tag{11}$$

only when (6) is fulfilled, that is:

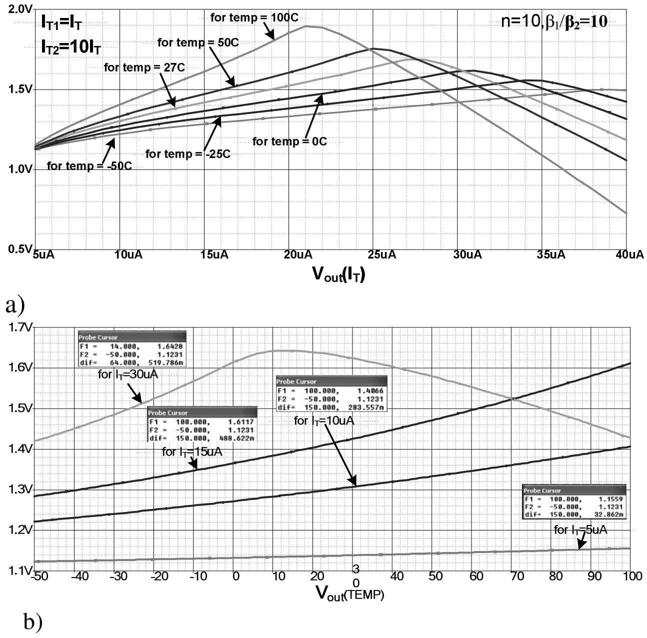
$$I_{T2} = k \cdot I_{T1} \tag{12}$$

Thus, relation (11) becomes

$$v_o = v_{BE1} + \left(\sqrt{k\frac{\beta_1}{\beta_2}lnn}\right)V_T \tag{13}$$

where n is the current ratio of the base-emitter diodes $n = I_{BE1}/I_{BE2}$.

Figure 4. gives some simulations proving the validity of this result



a)

b)

Figure 4. Simulations of circuit from *Figure 3* .

Table 1

I_T[μA]	ΔV_{REF} max[mV]	V_N[V]&27°C	Sensitivity - S[%]
5	32.862	1.138	0.52
10	283.557	1.303	3.92
15	488.622	1.418	6.20
30	519.786	1.629	5.74

To chose an appropriate bias current tail currents have been modified as shown in *Figure* 4a, to illustrate their influence over the output voltage at different temperatures. We could see that the ideal relation (8) was better satisfied for small values. That was also proved in *Figure* 4b where some examples of temperature characteristics are shown. In these examples the reference voltage can be adjusted by I_T at 27°C between 1,138V to 1,629V. Table 1 shows some of the resulted data, the maximum output voltage variation for temperature between -50°C and +100°C and sensitivity for different tail currents $S = \frac{\Delta V_{REF}}{150} x \frac{27}{V_N} x100\%$.

A similar circuit but with asymmetrical transistor pairs was realized by Buck a.o. [4] and can be represented by the above proposed general schematic presented in *Figure* 2.

b) BVR with base coupled composed MOSFET pairs

We propose in this paper a new schematic for a BVR that implements the model in *Figure* 2. Function F is implemented with base-coupled composed CMOS transistor pairs as *Figure* 5 shows.

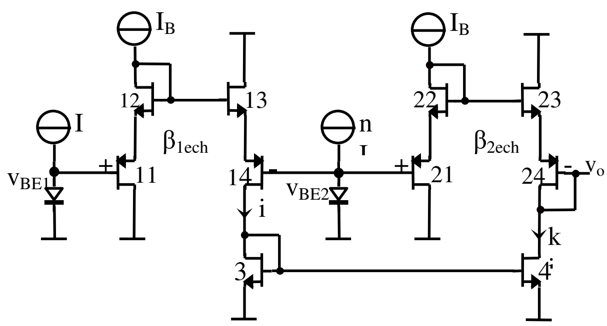


Figure 5. *BVR with base coupled composite CMOSFET pairs*

In this case, function F and its scaling factors will be:

$$i_o = I\left(\frac{v_{ID}}{V}+1\right)^2; \quad I = I_B; \quad V = \sqrt{\frac{I_B}{\beta_{eq}}}; \tag{14}$$

$$\sqrt{\beta_{eq}} = \frac{\sqrt{\beta_p\beta_n}}{\sqrt{\beta_p}+\sqrt{\beta_n}}; \quad \beta = \frac{K_{n,p}W}{2L}; \tag{15}$$

When (6) is fulfilled, relation (8) is valid. Substituting the relations that describe transconductors F, that is (14) and (15), results in:

$$v_o = v_{BE1} + \left(\sqrt{k\frac{\beta_{1eq}}{\beta_{2eq}}lnn}\right)V_T \tag{16}$$

$$\text{with} \qquad I_{B2} = k \cdot I_{B1} \;\; ; \;\; I_{D2} = n \cdot I_{D1} \tag{17}$$

Simulations in *Figure* 6 prove the validity of this schematic.

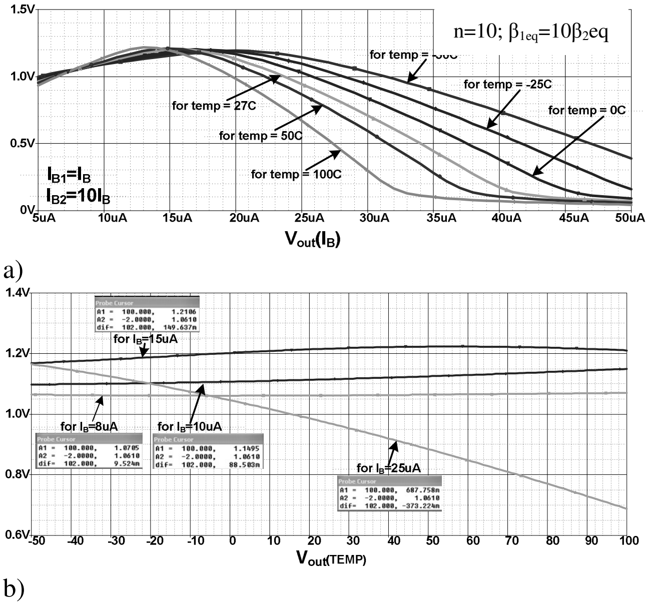


Figure 6.

Table 2

I_B[μA]	ΔV_{REF} max[mV]	V_N[V]&27°C	Sensitivity - S[%]
8	9.52	1.062	0.16
10	88.503	1.115	1.43
15	149.637	1.217	2.213
25	373.224	0.963	6.98

In these simulations one can also notice that the output voltage can be adjusted by bias currents I_B and, unlike the previous schematic, V_{REF} has a smaller thermal variation for a large current domain between 5μA and about 20 μA. Also a smaller dispersion of voltage reference values (in this domain of bias currents) can be noticed.

IV. CONCLUSIONS

A bandgap voltage reference structure was presented. It implements relation $V_{REF} = v_{BE} + GV_T$. The gain G is realized with an F-F^{-1} amplifier. It has the advantage in VLSI implementation because of its simplicity and no need of adjusting resistors. On this base, two nonconventional BVRs derived. The variant with base coupled transistors is a new one, proposed in this paper by the authors. The proposed BVR structure also includes a simplified form of a circuit from literature concerning another type of BVR without resistors.

The advantage of F-F^{-1} design does not consist only in its simplicity but also in the possibility of tuning the output value by bias currents.

In this paper we focused only on proving the validity of the new proposed circuit with its advantages in VLSI design. The next step will go toward parameter optimisation and a sistematic performance evaluation.

REFERENCES

[1] Ch.J.B.Fayomi, G.I. Wirth, H.F. Achigni, A. Matsuzawa:" Sub 1V CMOS Bandgap Reference design techniques: A Survey", *Analog Integrated Circuits Signal Processings* (2010), Volume 62, Number 2, 141-157, DOI: 10.1007/s10470-009-9352-4

[2] X.Guan, X.Wang, A. Wang, B. Zhao: "A 3V 110μW 3.1ppm/°C Curvature-Compensated CMOS Bandgap Reference", *Analog Integrated Circuits and Signal Processing, An International Journal*, DOI: 0.1007/s10470-009-9333-7, 2009

[3] W.M.C. Sansen: *Analog Design Essentials*, Springer, 2008, ISBN-13 978-0-387-25746-4

[4] A.E.Buck, Ch.L.McDonald, S.H.Lewis, T.R.Viswanathan:" A CMOS Bandgap Reference Without Resistors", *IEEE Journal of Solid-State Circuits*, vol 37, No 1, January 2002, 81-84

[5] Y.Tsividis: "Externally Linear, Time Invariant Systems and Their application to Companding Signal Processing", *IEEE Transactions on CSII*, vol44, No 2, Feb. 1997, 65-84

[6] L.Feştilă, L. Szolga, M. Cîrlugea, R. Groza:" Analog Multiplying/Weighting VLSI cells for SVM classifiers", *KES08 International Conferrence* , ISSN 3029743, Zagreb, 2008, ISBN-978-3-540-855675