REVIEW OF CURRENT STRAINED SILICON NANOSCALE MOSFET STRUCTURES

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Abstract: **Improvement in performance of Si- Metal Oxide Semiconductor Field Effect Transistors (MOSFET) through scaling is very difficult due to the several physical phenomenon mainly non classical in nature at nanometer scales. In this paper, an attempt has been made to give a detailed review of strained silicon technology so far developed since its inception. Various biaxial and uniaxial strained (MOSFET) structures have been studied. The advantages, disadvantages, physics and fabrication process of these structures have also been outlined and reviewed critically. The review indicates that this technology is very much required in nanoscale MOSFETs due to its several potential benefits over the conventional bulk technology. The paper also provides the insight of how the use of various techniques such as relaxed SiGe, graded SiGe, strained silicon on insulator (SSOI), silicon germanium on insulator (SGOI) and various other hetero-structures help in providing improved performance.**
Keywords: *Uniaxial strain, Biaxial strain, Mobility, SiGe, strained silicon technology, strained silicon on insulator, Hetero-structures.*

I. INTRODUCTION

As projected by the Moore's law that has governed the production of semiconductor industry for past six decades, the feature size of transistor has been reduced to below 100nm. With such small feature sizes in high volume production and under development, still conventional silicon (Si)- MOSFET technologies are now leading the field of nanotechnology. As the transistor gate length drops to 45 nm and below and the gate oxide thickness drops to 1 nm [1, 2], physical limitations, such as off-state leakage current and reduction in drive currents, make geometric scaling an increasingly challenging task. It is believed that conventional complementary metal oxide semiconductor (CMOS) is reaching its scaling limits and to extend Moore's law to the field of nanoelectronics, new materials and/or new innovations on CMOS structures are needed. One of the approaches is to increase the carrier mobility in the active region of the device by introducing strain. Starting with the 90-nm technology generation, mobility enhancement through uniaxial process-induced-strained Si has emerged as the next scaling vector being widely adopted in logic technologies [3]. Presently with the 65nm logic technology in volume production and 45 nm and 32 nm under development, all featuring strained Si state-of the art technology, Moore law is found to still be valid in the nanoelectronics era for the foreseeable future. The strained silicon technologies are still at research phase and very few commercially viable devices have been produced. Moreover, a combined study of the strained silicon devices and their physics and their suitability at various technology nodes at nanoscale has not been reported yet in the existing literature of strain technology across the wide domain of microelectronic community.

In this paper, various structures of strained silicon MOSFETs which have evolved with time since the inception of strain technology have been studied. These structures have been thoroughly reviewed and their comparative analysis has been done to predict the suitability of various devices at various technology nodes especially at nanometer scales.

II. HISTORY OF STRAINED SILICON TECHNOLOGY

The influence of strain on the mobility of intrinsic silicon was first observed in 1954 by C.S Smith [4]. The origin of strained Si film grown on relaxed SiGe c an be traced to the 1980s [5]. While strain effects were not largely exploited, it was in the early 1990s that the strain was once again revived at Massachusetts Institute of Technology (MIT), USA on process-induced and biaxial strain [5]. In 1992, the first n-channel MOSFET with a strained Si channel exhibiting a 70% higher mobility was demonstrated [6, 7]. The commercial adoption of strain technology was followed in 90 nm technology node by all major semiconductor companies like AMD, Integrated Electronics (Intel), International business machines (IBM). While IBM and AMD adopted strained-Si with their silicon on insulator (SOI) technology, Intel went ahead with strained Si on bulk Si MOSFET [8]. Table 1 shows the important milestone in development of strained silicon technology. It depicts that the first strained Si MOSFET in submicron technology was developed in 1998 subsequent to development of SiGe and strained Si MOSFET. The strained silicon at the 65-nm node and 45 nm were introduced in year 2005 and 2007 respectively [9]. The 32nm technology node features enhanced channel Strain with high-k along with metal-gate transistors.

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Understanding and features of various structures with strained silicon in nanoscale regime is required. This is because every current research deals with a particular structure and a thorough review of all the structures developed so far since the inception of the strained silicon technology is still desired to be done.

Table 1: Milestones in Development of Strained Silicon Technology [13]

S.No.	Milestone	Year
1.	*First investigation of the bandgap of unstrained SiGe alloys*	*1958*
2.	*First Si MOSFET*	*1960*
3.	*Concept of critical thickness for epitaxial strained layers*	*1963*
4.	*First oxidation study of SiGe*	*1971*
5.	*First growth of SiGe strained layers*	*1975*
6.	*First stability calculations of SiGe strained layers*	*1985*
7.	*First measurements of energy bandgap in SiGe strained layers*	*1985*
8.	*First step graded relaxed SiGe substrate*	*1988*
9.	*First SiGe gate CMOS technology*	*1990*
10.	*First SiGe pMOSFET*	*1991*
11.	*First SiGe pMOSFET on SOI*	*1993*
12.	*First strained Si pMOSFET*	*1993*
13.	*First strained Si nMOSFET*	*1994*
14.	*First SiGe pFET on SOS*	*1997*
15.	*First submicron strained Si MOSFET*	*1998*
16.	*First vertical SiGe pFET*	*1998*
17.	*First strained Si CMOS technology*	*2002*
18.	*Strained Silicon at 90nm Technology node [Intel]*	*2003*
19.	*Strained silicon at the 65-nm node provided a 15 to 20 % improvement in drive current compared with the 90-nm node.*	*2005*
20.	*A 45 nm logic technology for the first time incorporates high-k + metal gate transistors.*	*2007*

III. TYPES OF STRESS

Stress produces strain. Stress that shortens an object is called compressive stress while the one that lengthens an object is called tensile stress. Longitudinal tensile strain (strain along the channel, making it longer) allows electrons to move more quickly and smoothly, increasing the drive current and thus improving transistor-switching speed. These methods can be broadly classified into two different categories. These are a) substrate-induced strain introduced globally over the entire substrate in two directions (biaxial) and b) local strain arising from different processing steps or producing strains in some parts of MOSFET in only one direction (uniaxial) [10].

A. Biaxial or Global Strain

Global strain or substrate stain can be induced by doping germanium (Ge) in Si. The larger lattice constant of Ge produces strain in silicon lattice. Si and Ge having a lattice mismatch of about 4.2% can be combined together to form a SiGe alloy, the lattice constant of which lies between those of Si and Ge. Due to the lattice mismatch between Si and Ge atoms, tensile biaxial stress is generated [11].

B. Uniaxial or local Stress

Another approach to develop a strain in the channel is by SiGe deposition on the active regions beside the channel. This approach has been called the local-strain technology. Local strain is incorporated during the transistor fabrication process. The strains induced during transistor processing are typically uniaxial and are incorporated via tensile/compressive capping layers or recessed epitaxial film deposition in the source-drain regions. These processes are generally not universal in their implementation and need to be tailored to a

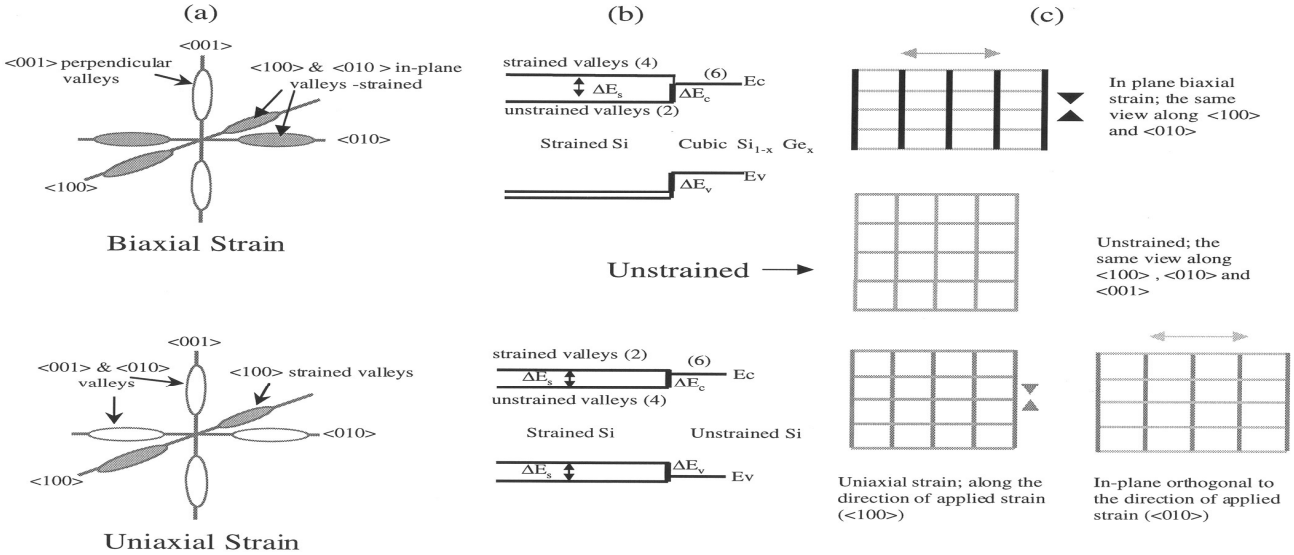


Fig 1: Comparison of biaxial and uniaxial strain [14]

particular transistor integration scheme. Uniaxial strain is caused by depositing tensile silicon nitride capping layer on the MOSFET device structure [12]. This approach is useful for the NMOS devices whereas for PMOS devices, the compressive strains are produced from the SiGe source and drains in the channel. As a result, the channel stress becomes dependent on the polysilicon gate. The lattice mismatch in the hetero-layer compresses the silicon lattice, which consequently compresses the device channel. Even the introduction of germanium in the source and drain of the MOSFET causes uniaxial strain in the direction parallel to the channel [15].

C. Comparison of Uniaxial and Biaxial Strain Physics.

Fig 1 shows the comparison of uniaxial and biaxial strain. The strain is a very useful parameter in devices as carrier mobility significantly increases by altering the band structure at the channel. The alteration of band structure in the channel layer provides lower effective mass and also suppresses intervalley scattering which is a prime cause of enhancement of carrier mobility and the drive current. The conduction band splitting has been shown in Fig.1. Each energy level of silicon is composed of six equal energy valleys in three dimensions. In inversion layers, these six valleys are split into two fold out of plane valleys located at the k_z axes (001) direction and four fold in-plane valleys in k_x (010) direction and k_y axes (100) direction. The electrons in all these conduction valleys have transverse mass (m_t =0.19m_0) and longitudinal mass (m_l = 0.916m_0). Clearly $m_l > m_t$ .In the two fold valleys, the electrons have transverse mass parallel to the MOSFET Si/SiO_2 interface and longitudinal mass perpendicular to the interface. On the other hand, in four fold valleys, the electrons have transverse mass perpendicular to the MOSFET Si/SiO_2 interface and longitudinal mass parallel to the interface. When a tensile strain parallel to the MOS interface (100) is applied (biaxial strain along k_x and k_y), the Δ_2 valleys and Δ_4 valleys are split up into lower and higher energy valleys. This band alteration gives an alternate lower site for electrons to reside i.e. Δ_2 valleys. The transverse effective mass of electrons in the lower energy valleys Δ_2 is lesser than the Δ_4 valleys in the direction parallel to the interface suitable for the flow of electrons from the source to drain. Due to this, the electron mobility increases [16]. Besides this, the inter-valley phonon scattering between the lower and upper states is suppressed due to the strain induced larger energy difference. As per the publication by Mark Bohr, Intel has used uniaxial strain technique to enhance mobility at 90nm, 65nm and 45nm technology nodes [17].

Another difference is that the uniaxial strain is applied to individual devices will change with feature size whereas biaxial strain are applied at the wafer level do not change with device dimensions. This approach is easier to model, as the strain level remains the same for devices with different dimensions and does not change as design shrinks. According to development at Freescale Semiconductor, externally applied strain is less useful as the pitch drops, making biaxially strained-silicon on insulator (sSOI) structures more appealing [18]. Fig 2 clearly depicts the reduction in mobility in unstrained

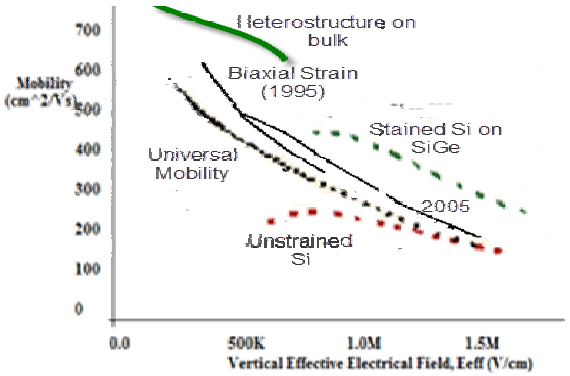


Fig 2: Comparison of Mobility with various Stained Si techniques and Unstrained Si.

silicon MOSFET in sub 100nm regime and the enhanced mobility incase of various strained silicon techniques. Biaxial strain enhances the mobility by 1.8 times as depicted Rim et al [19-21].

IV. UNIAXIAL STRAINED MOSFET STRUCTURE

As already discussed, uniaxial strain is generated by local structural elements near the channel region. It is also referred as process-induced strain (PIS). Electron and hole mobilities respond to stresses in different ways. Therefore, to improve both the electron mobility in n-channel MOSFETs (NMOS) and the hole mobility in p-channel MOSFETs (PMOS), different approaches for strain inducement in the p and n-channel transistor is needed.

One way of introducing uniaxial stress is with a help of thermal mismatch stress, which occurs when two materials with different coefficients of thermal expansion are heated, they expand/contract at different rates. During thermal processing, thin film materials like polysilicon, SiO_2, silicon nitride expand and contract at different rates compared to the silicon substrate according to their thermal expansion coefficients [22]. This enhances electron mobility, thereby improving NMOS performance as shown in Fig 3(a).

The PMOS performance is enhanced by using selective SiGe layer as source/drain regions. The lattice mismatch in the hetero-layer compresses the silicon lattice, which consequently compresses the device channel as shown in Fig 3(b). These transistor structures introduced first at Intel's 90nm CMOS node. SiGe film embedded into source/drain SiGe film deposited by selective epitaxy induces large uniaxial compressive strain in channel. This strain leads to dramatic hole mobility enhancement [23].

V. BIAXIAL STRAINED MOSFET STRUCTURES

A. SiGe MOSFET

The global strain or biaxial strain on wafer level is mostly induced by the epitaxial growth of SiGe and Si layers. The lattice parameter of SiGe alloys increases with Ge concentration, the tensile strain is induced in a

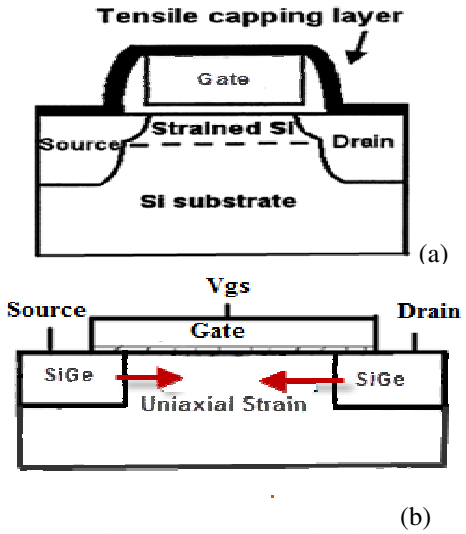


Fig 3: Uniaxial strain at 90nm Technology node a) for NMOS (b) for PMOS

silicon layer epitaxially grown on top of the SiGe. The gradual increase of the germanium content in the silicon is called as graded silicon it causes relaxation in the SiGe layer [24]. This structure has been given in Fig 4. The introduction of Ge in Si substrates causes strain in the substrate and increases the mobility of carriers in silicon, but the problem is that the oxide of SiGe cannot be grown easily. This is because the SiGe decomposes at higher temperatures of oxidation and SiO_2 is formed instead of $SiGeO_2$. Oxidation of SiGe yields a low quality dielectric layer since the oxygen reacts preferentially with Si, leaving un-reacted excess Ge near the oxide interface. This is the so called "snow-ploughing" effect [25]. The snow-ploughing of Ge also has deleterious effects in device isolation contributing to leakage current in the device for strained Si MOSFETs. So, the SiGe substrate cannot be used alone for the purpose. Second problem is that SiGe layers grown on a Si substrate exhibit changes in the valence band only. The structure is only favorable for enhancing hole mobility.

B. Strained Si MOSFET

In order to enhance mobility for both electrons and holes, conduction and valence band changes are required which is not possible in SiGe structure discussed above. The second structure is shown in Fig 5. In this, the silicon crystal is grown over strained and finally relaxed SiGe substrate using deposition techniques in the pseudo-morphed fashion i.e. same underlying morphology (features) to be continued in the above grown silicon. The strain in the SiGe continues in the silicon. This is called strained silicon technology The silicon oxide can be easily grown over the strained silicon without much difficulty. This produces novel properties i.e. enhanced drain currents with lesser effects of inversion layer quantization and enhanced carrier mobility. Given the difficulty in creating SiGe single crystal substrates, the strained-Si top layer, upon which the transistor will be built, is grown on the relaxed-SiGe layer, which is termed as "virtual substrate"[26].

C. Strained SiGe on Insulator Device Structure

The third novel structure for strained silicon

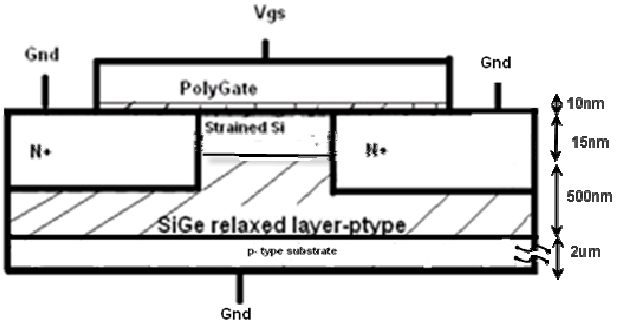


Fig 5: Cross-sectional view of biaxially strained-Si–SiGe bulk-Si MOSFET

technology which came in year 2003 proposed by MIT, USA for 65nm technology node is the strained SiGe on insulator device structure is shown in Fig 6 [27]. It is a multilayer substrate device consisting of a lowly doped silicon substrate, a SiGe buffer, buried oxide, relaxed SiGe layer and a strained silicon thin layer over the top called as cap layer. This technology is a mixture of silicon on insulator and strained silicon technology.

In strained Si on insulator (SSOI) structures, the relaxed SiGe on insulator layer serves as a template for inducing tensile strain in the silicon layer. The SSOI structure has a number of advantages. It eliminates issues associated with SiGe during MOSFET processing, such as Ge up diffusion and enhanced diffusions of n-type dopants in SiGe.

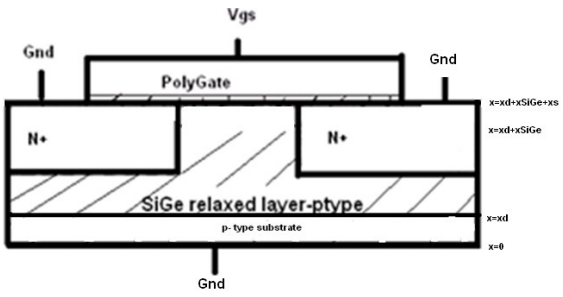


Fig 4 : Silicon Germanium MOSFET

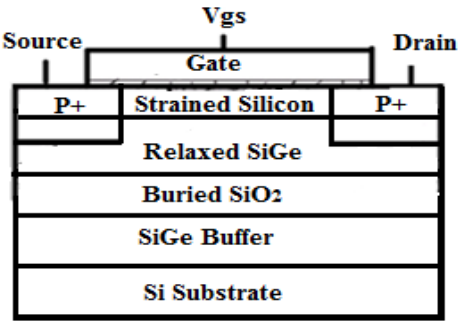


Fig 6: Schematic of SSGOI MOSFET

D. Germanium-free SSOI

A novel Ge free SSOI structure that does not include a relaxed SiGe layer as shown in Fig 7, has been presented by Amber Wave Systems Corporation [28]. The relaxed SiGe layer has been removed because it adds to the total thickness of the semiconductor structure, making it difficult to consistently achieve the target thicknesses required for fully depleted SSOI device fabrication.

Thus, it becomes advantageous to eliminate the relaxed SiGe layer from SSOI structures targeted at fully depleted technologies. Germanium-free SSOI also eliminates undesirable qualities of Ge such as thermal instability and contamination by Ge diffusion during high temperature processes.

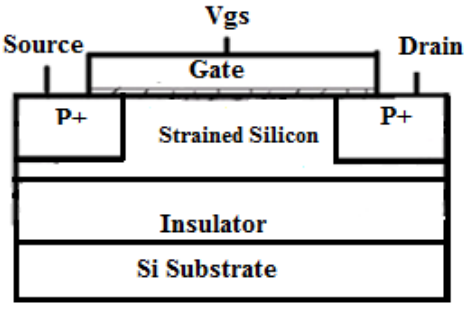


Fig. 7: Ge Free SSOI

E. Hetero-structure MOSFET

The final structure in current practice is the dual channel hetero-structures. High mobility strained-Si CMOS on relaxed SiGe virtual substrates has been

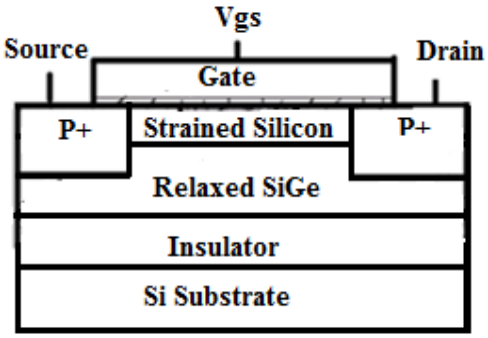


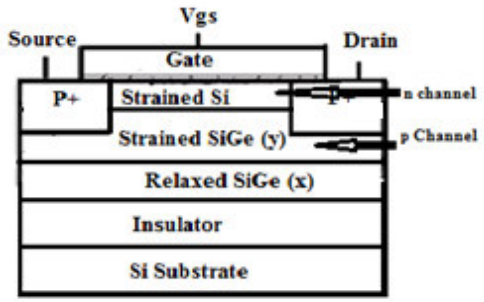
Fig 8: Single-channel Heterostructure

demonstrated for the 65 nm technology node by MIT, Microsystems Technology Laboratories [29]. Strained-SOI MOSFETs, with either a relaxed SiGe-on-insulator (SGOI) substrate or a strained-Si-on-insulator (SSOI) substrate [30], combine the benefits of two complementary technologies: a high mobility strained-Si channel and SOI architecture. In such a structure, as shown schematically in Fig 8, the strained-Si, grown on a relaxed- SiGe layer is a single-channel hetero-structures. It serves as both an electron and a hole channel under n-MOSFET and p-MOSFET operation, respectively.

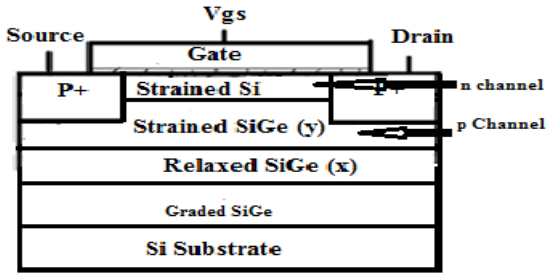
To boost hole mobility significantly, which is of great interest for CMOS applications, one solution is to introduce a compressively strained-SiGe channel into the structure to serve as a hole channel, a structure referred to as `dual-channel hetero-structure' (DH) in the literature [31, 32]. The schematic diagram in Fig 9(a) shows such a dual-channel strained-Si/strained-SiGe hetero-structure on relaxed-SGOI: a compressively strained-SiGe layer for the hole channel and a strained-Si layer for the electron channel, both grown on a relaxed- SiGe -on-insulator substrate which has low-to-medium Ge content [32]. In dual channel structures, the first SiGe layer is very thin and the interface between the buried oxide and the first SiGe layer is loose, the stress balance between the first and the second SiGe layers can lead to the tensile strain in the first SiGe layer and the resulting higher strain in strained Si layer. For comparison, Fig 9(b) shows a corresponding dual-channel strained-Si/strained-SiGe hetero-structure on a bulk-SiGe virtual substrate. The compressively strained-SiGe channel can provide much higher hole mobility enhancement than the strained-Si channel, making it possible for holes to have equal or higher mobility enhancement than electrons.

F. Fabrication of SSOI substrates

SSOI substrates can also be fabricated such that the strained-Si lies directly on the insulating substrate, with no underlying relaxed-SiGe layer. Separation by implanted oxygen (SIMOX) [33] is a popular technique



(a) Dual-channel strained-Si/strained-SiGe hetero-structure on relaxed-SGOI



(b) Dual-channel strained-Si/strained-SiGe hetero-structure on a bulk-SiGe virtual substrate.

Fig 9 (a) and (b): Dual Channel Hetero-structures [34]

for SOI fabrication, but unfortunately, is only applicable to SGOI fabrication for low Ge mole fractions (up to 18%). Wafer bonding is another technique for fabricating SGOI or SSOI, involving the bonding of wafers with SiGe films to insulating substrates. Table 2 gives the brief comparison of various biaxial strained silicon structure discussed so far.

A few widely employed techniques exist for accomplishing layer transfer of a thin film of material onto any desired substrate (fig 10): (a) back-side grinding, (b) grind and etchback, and (c) delamination via implantation. In these methods, a final polishing step is usually employed to smooth and thin the transferred layer. Huang et al. [35] used Smart-Cut to transfer relaxed-SiGe onto oxidized Si substrates. The defect density in the film is very low, the electrical properties are excellent, and the BOX quality is comparable with that of the original thermal oxide.

Table 2: Comparison of Various Biaxial Strained-Si Structures

S.No	Structure	Feature
1.	Substrate Strain	Causes tensile strain in channel, Enhances electron mobility only.
2.	Stained Si on Insulator (SSOI)	Combines strained Si and SOI.SOI advantages i.e. no latch-up and no leakage between devices, enhanced speed performance, low-power consumption.
3.	Ge free Silicon Germanium on Insulator (SGOI)	Germanium-free SSOI eliminates undesirable qualities of Ge i.e. thermal instability and contamination by Ge diffusion during high temperature processes.
4.	Dual channel Heterostructures on Bulk (DHOB)	Both electron and hole mobility enhancement
5.	Dual channel Heterostructures on insulator (DHOI)	Dual channel, electron and hole mobility enhancement, potential to scale the thickness into ultra thin regime, minimizes SCEs.

G. Supercritical Strained Silicon Technology

As discussed in previous sections strained-Si/SGOI have led to encouraging demonstrations of MOSFET mobility and current drive enhancement, but the presence of SiGe in the device region (above the buried oxide) leads to significant process integration challenges. Amber Wave Systems Corporation demonstrated the supercritical SSOI. In bulk strained-Si/SiGe it was essential to keep film thickness below the critical thickness for the onset of strain relaxation in order to avoid formation of misfit dislocations at the strained-Si/SiGe interface [36]. However, it was shown that even when critical thickness is exceeded by a factor of approximately 3 in SSOI MOSFETs, no source-to-drain leakage occurs. The explanation for this surprising result is that the misfit dislocations which appear for thickness less than critical thickness are not present in the final SSOI wafer, since the strained-Si/SiGe interface has been removed [37]. In addition, MOS mobility measurements for this supercritical film show no loss of enhancement compared to thinner films on bulk strained-Si/SiGe.

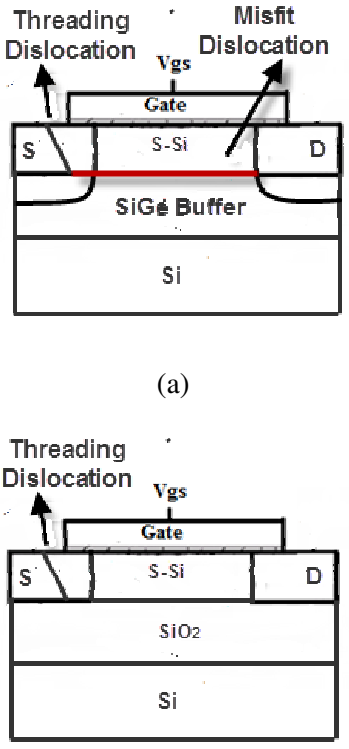


Fig 10 (a) Misfit dislocations are present at strained-Si/SiGe Interface (b) SSOI structure depicts misfit dislocations are absent from SSOI, since the strained-Si/SiGe interface is no longer present.

HOT (fig 11) composed of regions of Si (001) and Si (110), including tensilely strained Si (110). This provides a material that is both flexible and transferable, and suitable for high-performance CMOS.

TABLE 3 Reported biaxial and uniaxial structures implemented by various manufacturer [38].

S.No.	L_g (nm)	Manufacturer	Strain Type
1.	150	Freescale/ TSMC/ SOITEC/IBM	Biaxial on SOI
2.	140	Intel	Global
3.	67	IBM	Global
4.	60	TSMC	Global
5.	45	Intel	Local
6.	40	Toshiba	Global

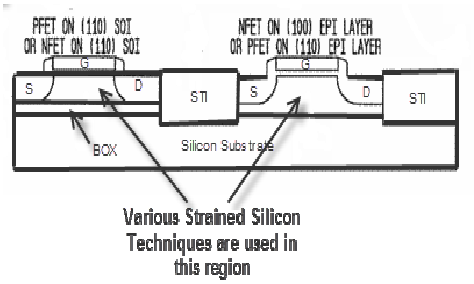


Fig 11: A schematic cross-section illustrating a basic structure of hybrid orientation technology (HOT) [39]

VI. CONCLUSION

This paper gives the review of strained silicon technology. The uniaxial and biaxial structures proposed by both industry and academia via literature and patents have been reviewed. The main structures under biaxial category are relaxed SiGe, graded SiGe, strained SOI, SGOI and other various hetero-structures help in providing improved performance. On the other hand, the uniaxial technology is simple to implement and has already been used at sub 90nm technology, the main issue is it is non-uniform, the strain to individual devices will change with feature size on the other hand biaxial strain is pitch independent. Moreover, researchers have proposed the biaxial strain solution provided by SSOI as the key material for solving the integration issues raised at 45nm and below. It can be concluded from the paper review that dual channel hetero-structures on insulator (DHOI) technology has a potential to scale down MOSFET further towards nanoscale regime. Combining the advantages of SOI and strained silicon is the way to minimize process complexity, while achieving the performance gain in keeping with Moore's Law.

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