

A THREE LEVEL VOLTAGE INVERTER USED FOR AN INDUCTION MOTOR CONTROL

Nicoleta Roxana BUZATU, Dimitrie ALEXA, Georgian Alexandru LAZAR, Dan BUTNICU, Oana Loredana BUZATU, Razvan VIERIU
Technical University "Gheorghe Asachi" of Iasi, Bd. Carol I, nr 11, RO - 700506 Iasi, Romania
rbuzatu@etc.tuiasi.ro, lazara@etc.tuiasi.ro

Abstract: Advances in power electronics technology allowed the wide investigation of multilevel converters that provide higher power with less harmonic components, compared to the two - level structure. Among this family of converters, the three - level neutral – point - clamped (NPC) converter is widely used in medium voltage applications. This paper presents a three - level Neutral – Point - Clamped inverter using space vector pulse width modulation (SVPWM) for induction motor control.

Keywords: Three - level voltage inverter, neutral-point-clamped (NPC), induction motor, speed control.

I. INTRODUCTION

The multilevel converters were born with the specific aim to overcome the voltage limit of semiconductor devices. The main idea of multilevel converters is to connect more devices in series and clamp the voltages between their pins. The differences among this type of structures derive from how the clamping is done. Multi – level converters gained mainstream use due to a very good total harmonic distortion (THD) factor. The employment of fast switching devices (MOS transistors) led to a series of low and medium converters, which almost do not require an output filter anymore.

There are several other advantages of the multilevel approach when compared to traditional (two – level) power conversion. Firstly, the smaller voltage steps lead to the generation of higher power quality waveforms and also reduce the dv/dt stresses on the load. Secondly, the semiconductor devices are in a series – type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Thirdly, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses. One drawback of multilevel power conversion is the larger number of semiconductor switches required, which increases the complexity of the converter. The first multilevel converter can be attributed to R. H. Baker and L. H. Bannister, who patented the cascade H - bridge in 1975. In 1980 Baker patented the diode - clamped topology which is still the most used nowadays. In 1992, T. A. Meynard and H. Foch patented the flying – capacitor architecture. In the same year, S. Osagawara, J. Takagali, H. Akagi and A. Nabae proposed a new approach: they Three different topologies have been proposed for

considered a standard Current Source Inverter (CSI) and increased the number of current levels instead of voltage ones. From 1992 onwards, the research on multilevel converters both perfected original topologies and invented new ones, suitable for new and uncommon applications. Considering the state of the art in this technology field, it can be asserted the maximum power limit has been reached. This fact derives both from standards and from economic reasons. Considering land traction industrial applications, standards limit the maximum voltage of each battery banks at 96 V for safety reasons. On the other hand, standards do not impose this limit to road vehicles, but the market does. The semiconductor switches usually used in this kind of applications are MOSFET's rated at 150 V, because of the smaller costs involved. Hence, even if the limit on the voltage is not imposed by an actual law, it is still present in road transport applications too.

The most common configuration of multilevel converters is the neutral point clamped voltage source inverter structure (VSI – NPC) which is widely used in medium voltage drives for rolling mills, marine, and traction applications [1]. The cascaded topology is generally employed in voltage industrial drives, electric vehicles, and grid connection of photovoltaic cell generation systems [2].

To control multilevel converters, pulse width modulation (PWM) strategies are the most effective, especially space vector pulse width modulation (SVPWM), which has a lower total harmonic distortion (THD) [3]. Although more complex than PWM, SVPWM is preferred as it reduces the power losses by limiting the minimum pulse width [3], [4].

II. SYSTEM DESCRIPTION

A. Space Vector Pulse Width Modulation

Multilevel inverters: diode – clamped (neutral – clamped)

[5]; capacitor – clamped (flying capacitors) [6] – [8]; and cascaded multi – cell with separate DC sources [7], [8] – [10]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space – vector modulation (SVM).

The structure of the three – level inverter is shown in Figure 1. Each branch of the inverter contains 4 MOSFET transistors anti - parallel connected and two neutral clamping diodes. The point ‘N’ should have a constant potential as referred to point ‘G’ (the negative pin of the DC voltage supply) and equal to E/2. Point ‘N’ is taken as reference for evaluating the output voltage of the converter. The functioning principle is depicted in Table 1. The three - level voltage inverter outputs three - level voltages (-E/2, 0, E/2) depending on the DC - bus voltage E and the variable state C_i , where ‘i’ is the phase indicator (i = a, b, c). S_{i1} , S_{i2} , S_{i2}' , S_{i1}' are the switches of one leg, and V_{iN} is the phase – to - fictive middle point voltage. In order to obtain the desired three - level voltages, the converter must ensure complementarities between the pairs of switches: (S_{i1} , S_{i2}') and (S_{i2} , S_{i1}').

The inverter output voltage can be represented by a two - dimensional (α , β) voltage space vectors, defined as:

$$\vec{u}(t) = \frac{2}{3} \left[u_{aN}(t) + \vec{a} u_{bN}(t) + \vec{a}^{-2} u_{cN}(t) \right] \quad (1)$$

$$\vec{u}(t) = u_{\alpha}(t) + j u_{\beta}(t) \quad (2)$$

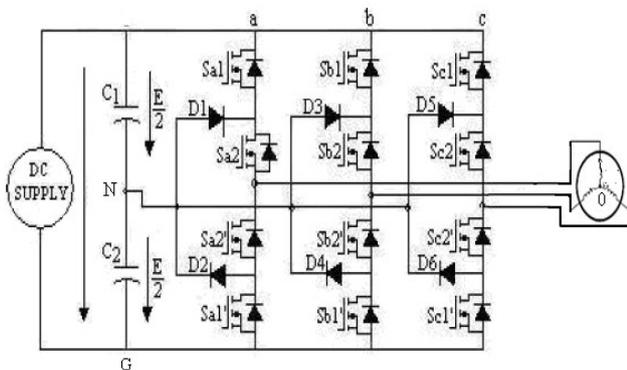


Figure 1. Configuration of three – level voltage inverter

$$\vec{\alpha} = e^{j\frac{2p}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \quad (3)$$

where: $u_{\alpha}(t)$, $u_{\beta}(t)$ are the real and imaginary components of the space voltage vector in complex notation, u_{aN} , u_{bN} , u_{cN} : inverter output phase voltages between terminals a, b, c and N (Figure 1), and $\vec{\alpha}$ is a complex operator.

Table 1. Switching states of a three – level inverter

Switching state	C_i	S_{i1}	S_{i2}	S_{i2}'	S_{i1}'	V_{iG}	V_{iN}
2	1	1	1	0	0	E	E/2
1	0	0	1	1	0	E/2	0
0	-1	0	0	1	1	0	-E/2

The inverter output phase voltages u_a , u_b and u_c are transformed to α and β variables according to the following axis coordinate transformation:

$$\begin{bmatrix} u_{\alpha} \\ u_{\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (4)$$

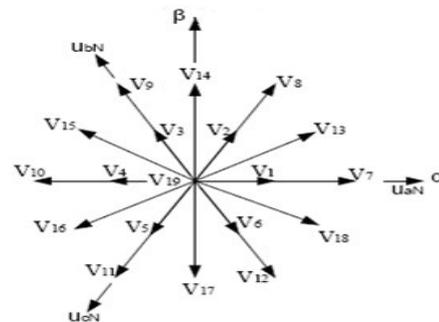


Figure 2. Space voltage vector of a three – level inverter

Table 2 shows the three switching states of an inverter’s bridge. The three - level inverter has twenty seven (3^3) switching states. Using equation (4), the inverter voltage vector for each switching state can be calculated. The inverter voltage vectors and their switching states are shown in Figure 2. According to their magnitude, the voltage vectors are divided into four groups: the zero voltage vector (ZVV) V_{19} , the small voltage vectors (SVV) $V_1 - V_6$, the middle voltage vectors (MVV) $V_{13} - V_{18}$ and the large voltage vectors (LVV) $V_7 - V_{12}$. The Null Point (NP) voltage control (point (N) in Figure 1) is usually achieved by selecting proper redundant switching states from the SVV, so that the charging effect diminishes the discharging effect of the capacitors during one fundamental period. The ZVV and LVV do not affect the N point voltage, while the MVV increase or decrease the N point voltage according to the load condition.

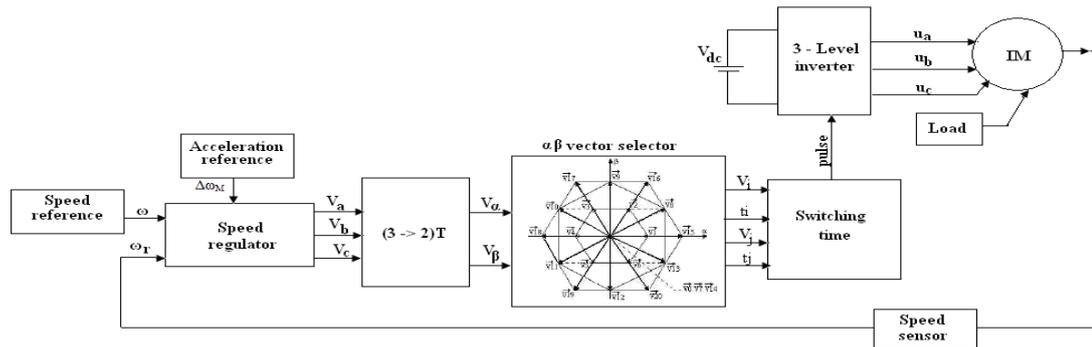


Figure 3. The operating principle of an electric drive controlled through SPWM

Table 2. Switching state of each voltage vector

Vector	Switching state	Vector	Switching state
V ₁	211/100	V ₁₁	002
V ₂	221/110	V ₁₂	202
V ₃	121/010	V ₁₃	210
V ₄	122/011	V ₁₄	120
V ₅	112/001	V ₁₅	021
V ₆	212/101	V ₁₆	012
V ₇	200	V ₁₇	102
V ₈	220	V ₁₈	201
V ₉	020	V ₁₉	000/111/22
V ₁₀	022		2

B. The control system

The operating principle of a variable speed electric drive controlled through the space vector modulation is illustrated in Figure 3. The Speed Regulator block is presented in Figure 4. This block ensures the scalar control of the induction machine, by maintaining the ratio V/f at a constant level. The speed reference signal ω is compared to the rotation speed of the rotor ω_r and a proportional integrative (PI) block computes the necessary difference $\Delta\omega$. In order to avoid the operation in the unstable region of torque – slip frequency curves, which would produce overcurrent issues, a saturation block is inserted after the PI block. The saturation value performed by this block is the minimum slip value which does not exceed the maximum torque, according the motor slip – torque characteristic. The slip ($\Delta\omega$) is added to the speed of the rotor (ω_r), thus obtaining the speed with which the stator has to be supplied (ω_s). Since the constant voltage/frequency control condition is satisfied through the V/f block, the stator flux remains constant, which guarantees the motor’s torque – slip frequency proportionality. Due to the limitation of the slip frequency command ($\Delta\omega$), the motor will not pull out either under rapid speed command changes or under load torque changes. Rapid speed reduction results in a negative

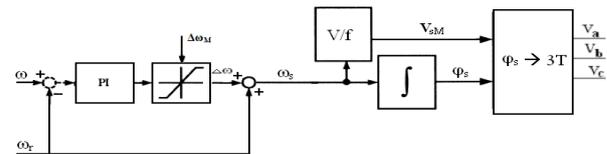


Figure 4. Speed Regulator block

slip command and the motor goes into braking. The integrator ensures the necessary information for computing the phases of the stator’s voltages v_a , v_b and v_c generated by the $\phi_s \rightarrow 3T$ block. The speed regulator block outputs the reference sinusoidal voltages system used for the inverter vectorial control. The three phases are transformed into a bi-phased system with the help of the $(3 \rightarrow 2)T$ block, which is described by equation (4). The $\alpha\beta$ vector sector is used to find the sector of the (α, β) plane in which the plane is divided into six different sectors spaced by 60° . The switching time block is used to compute the switching time for each voltage vector, which enables the inverter’s switches. The three – level inverter supplies the asynchronous motor.

III. SIMULATION RESULTS

The main parameters of the induction motor and three – level voltage inverter used in the Matlab simulations are depicted in Table 3.

Table 3. Simulation parameters

Parameter	Value
Output power	$P_N = 4 \text{ kW}$
Stator resistance	$R_s = 1.405 \ \Omega$
Rotor resistance	$R_r = 1.395 \ \Omega$
Stator and rotor inductance	$L_s = L_r = 0.006 \text{ H}$
Number of pole pairs	$p = 2$
Motor inertia	$J = 0.013 \text{ Kgm}^2$
Magnetizing inductance	$L_m = 0.1722 \text{ H}$
V/f = const	$V/f = 3.2$
DC- bus voltage	$E = 500 \text{ V}$

The main results, concerning the advantage of the SVPWM application, are represented in Figures 5, 6 and 7. Figure 5 depicts the phase – to – neutral voltage for each phase of the inverter phased with 120° .

Figure 6 illustrates the phase – to – ground point voltage V_{ag} corresponding to: $V_{ag} = E \rightarrow 500$ V (stage 2), $V_{ag} = E/2 \rightarrow 250$ V (Stage 1) and $V_{ag} = 0$ V (stage 0).

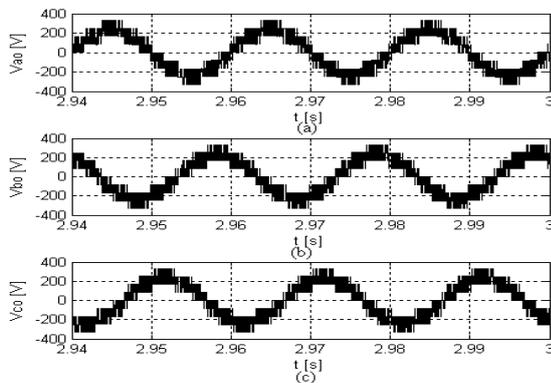


Figure 5. Outputs of the multilevel inverter

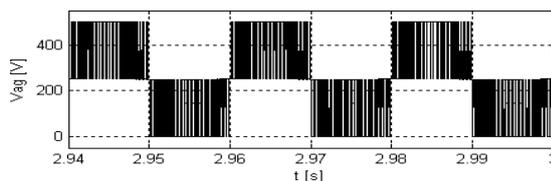


Figure 6. Power converter line-to-ground PWM output voltage

Figure 7 presents a dynamic evolution of the motor. Due to the limitation block from the Speed Regulator, Figure 4, the motor speed variation (dashed line) is not a step one as it is generated by the speed reference block from Figure 3 (continuous line). The motor speed increases and decreases almost linearly. Electromagnetic torques depicted in Figure 7b.

IV. CONCLUSIONS

This paper implements a vectorial controlled three level inverter, which drives an induction motor. The control of the speed of the electrical motor is done through ensuring a constant V/f ratio, which leads also to a constant stator flux. Even though this method does not provide remarkable dynamic performances, this approach is both simple and robust. Due to the use of the slip saturation control the presented motor drive system can be used in applications where both speed and motor acceleration are restricted. A possible application would be an electric train or other electrical vehicle. Along its trajectory, the user may combine speed and acceleration restrictions through the “speed reference block” (ω_M) and through “acceleration reference block” ($\Delta\omega_M$), respectively (Figure 3). As a result, it can be utilized in numerous industrial applications, where requirements related to the dynamic properties of drive control are of secondary importance. This is especially the

case wherever no rapid motor speed change is needed and where there are no sudden load torque changes.

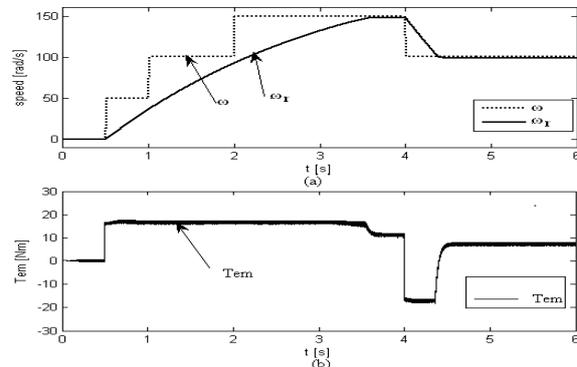


Figure 7. a) Variation of the speed; b) Waveform of the electromagnetic torque

REFERENCES

- [1] T Brückner, D. G. Holmes, “Optimal Pulse-Width Modulation for Three- Level Inverters”. *IEEE TRANS. Power Electron.*, Vol. 20, No. 1, 82-89 January 2005.
- [2] C. Loh, D. G. Holmes, T. A. Lipo, “Implementation and Control of Distributed PWM Cascaded Multilevel Inverters With Minimal Harmonic Distortion and Common-Mode Voltage”. *IEEE TRANS. Power Electron.*, Vol. 20, No. 1, 90-99 January 2005.
- [3] H Lee, D-H Kim, D-S Hyun. “Carrier Based SVPWM Method for Multi-Level system with reduced HDF”. *In the thirty-fifth IEEE Annual Meeting and World Conferences on Industrial Applications of Electrical Energy CD-Rom proceedings.*
- [4] P.F Seixas, M.a Severo Mendes, P Donoso Garcia. “An Algebraic PWM Method for Three-Level Voltage Source Inverter”. *In the thirty-fifth IEEE Annual Meeting and World Conferences on Industrial Applications of Electrical Energy CD-Rom proceedings.*
- [5] A.Nabae, I. Takahashi, and H. Akagi, “A new neutral-point clamped PWM inverter,” *IEEE Trans. Ind. Applicat.*, vol. IA-17, pp. 518–523, Sept./Oct. 1981.
- [6] J. S. Lai and F. Z. Peng, “Multilevel converters—A new breed of power converters”, *IEEE Trans. Ind. Applicat.*, vol. 32 pp. 509–517, May/June 1996.
- [7] T. A. Meynard and H. Foch, “Multi-level choppers for high voltage applications,” *Eur. Power Electron. Drives J.*, vol. 2, no. 1, pp41, Mar. 1992.
- [8] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, “Comparison of multilevel inverters for static var compensation,” *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1994, pp. 921–928.
- [9] P. Hammond, “A new approach to enhance power quality for medium voltage ac drives,” *IEEE Trans. Ind. Applicat.*, vol. 33, pp. 202-208, Jan/Feb. 1997.
- [10] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, “A new medium voltage PWM inverter topology for adjustable speed drives,” *in Conf. Rec. IEEE-IAS Annu. Meeting*, St. Louis, MO, pp. 1416-1423, Oct. 1998.