COMPARATIVE ANALYSIS OF THREE VERSIONS OF A CAPACITOR-LESS LDO STRUCTURE THAT SUPPLIES A RAIL-TO-RAIL VCO

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Abstract: This paper presents three circuit implementations of a low-dropout voltage regulator (LDO) structure that supplies a rail-to-rail voltage controlled oscillator (VCO) operating at 2.5GHz. The LDOs comprise only a small decoupling capacitor that can be integrated but they are still able to deal with the large and fast variations of the supply current required by the VCO. For a fair and direct comparison, all three LDO versions use the same pass transistor and are designed to maintain the output voltage ripple at the same level. Two symmetrical OTAs – one optimized for low-power consumption and the other for higher-bandwidth and lower noise – and one folded-cascode OTA optimized for low noise were employed successively to implement the error amplifier within the LDO. The comparison focuses on the effect the LDOs have on the phase noise of the VCO they supply. It was found that the VCO phase noise can be improved by reducing the level of high-frequency noise on the VCO supply line, caused by the LDOs.

Keywords: *Capacitor-less LDO, Error amplifiers, SoC*

I. INTRODUCTION

The low-dropout regulator (LDO) is a linear voltage regulator that employs a PNP or PMOS transistor as the series control element – that is, the pass transistor connected between the input and output. This way, the LDO can maintain normal operation even when the voltage difference between input and output drops to relatively low values – down to hundreds of mV.

Besides providing suitable voltage levels LDOs are used to separate the supply lines of different blocks, to prevent/reduce noise coupling and leakage. A typical LDO employs a large – therefore external – decoupling capacitor at its output for both energy reservoir for fast load transients and frequency compensation [1]. However, when more LDOs are to be used – as is the case of system-on-chip (SoC) designs - this approach requires a large number of pins, which is not always acceptable. Therefore, alternative LDO topologies have been developed, which do not require external decoupling capacitor – called hereafter "capacitor-less" LDOs, although some of them continue to require an output capacitor, but small enough to be fully integrable.

Common shortcomings of these "capacitor-less" designs are poor response to fast variations of the output current and the need of additional active control circuitry. Several solutions have been reported in the literature: in [2] a damping-factor-control compensation was employed, in [3] a fast settling time was achieved by using a common-gate amplifier and a direct dynamic charging technique and in [4] a dynamic gain adjusting mechanism was employed.

After analyzing several solutions proposed in the literature we decided that the one best suited to our application – supplying a 2.5GHz rail-to-rail VCO, which imposes very large and fast variations of the supply current – was the structure presented in Figure 1 [5]. This LDO is similar to the typical LDO topology shown in [1] except it has an additional active compensation network around the PMOS pass transistor, formed by a current amplifier and the compensation capacitor Cf. Thus, the decoupling capacitor, Cout, has a low enough value to be integrated on chip.

Reference [5] employs a symmetrical OTA to implement the EA, but without describing the reasons that topology was chosen; also, no analysis was shown regarding the relationship between the EA parameters and the performance of the entire LDO. This paper is a step towards filling this gap: first, it discusses the effect increasing the main EA parameter, the gain-bandwidth product (GBW), has on the LDO parameters; then it analyses the effect of changing the EA topology, while maintain its GBW.

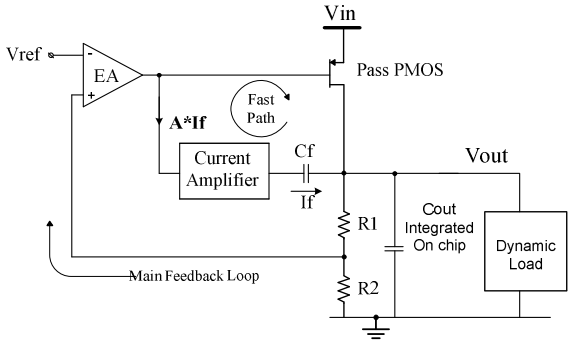

Figure 1: The LDO topology proposed in [5]; Cout has a value low enough to be integrated on-chip.

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For this purpose, the LDO topology shown in Figure 1 was implemented in three versions, which are described in some detail in the followings. For a fair and direct comparison, all three versions use the same pass transistor and drive the same load; also, the voltage ripple at the LDO output is maintained at about the same level. The comparison focuses on the effect the LDOs have on the phase noise of the VCO they supply. Of course, the standard LDO parameters
(the current consumption, load and line regulation, PSRR and, most importantly, the output noise) are also monitored.

The paper is organized as follows: Section II discusses the first two implementation cases: both employ the same symmetrical OTA for the EA, but with different GBW values. The third LDO version is presented in Section III: a folded-cascode OTA was used for the EA there. Section IV presents briefly the load – a rail-to-rail VCO operating at 2.5GHz. The main simulation results are discussed in Section V. Conclusions are drawn in the last Section.

II. TRANSISTOR-LEVEL IMPLEMENTATION OF TWO LDOs WITH SYMMETRICAL EA

A. LDO description

The LDO topology proposed in [5] is presented in Figure 1; it is similar to a conventional LDO such as the one discussed in [1], except it has an additional compensation network around the PMOS pass transistor and it is formed by a feedback capacitor, Cf, and a current amplifier. In a conventional LDO the transient response bottleneck is the large gate capacitance of the pass transistor. For low dropout the pass transistor needs to be large; depending on the current passing through, its gate capacitance can be in the order of pF/tens of pF. The charging and discharging of such a large capacitance is the main factor that determines the transient response of the LDO, much more than the gain-bandwidth of the main loop.

The additional compensation network shown in Figure 1 provides a fast feedback path in order to improve the transient response; it forms an internal negative feedback loop with a much wider bandwidth than the overall LDO bandwidth. In order to respond fast enough to load variations a sensing mechanism with high bandwidth is needed; theoretically this can be achieved by a capacitor. However, connecting the capacitor between the gate and drain of the pass transistor will have an effect only if its capacitance is greater than the gate-drain capacitance.

Another problem is that by doing so, the capacitor will create a feed forward path to the output, degrading the phase margin. The current amplifier solves both problems: first by amplifying the capacitor seen at the gate and second by blocking the feed forward signal path. The amount of current supplied by the sensing capacitor can now be amplified, improving the charging/discharging time of the pass PMOS gate capacitance. The compensation circuitry can be implemented by a current amplifier and a compensation capacitor, Cf, as shown in Figure 2.

In this arrangement both the LDO stability and its fast transient response are ensured even for low values of the

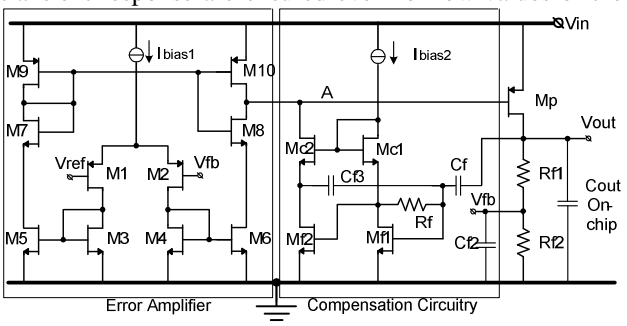


Figure 2: Circuit implementation of the LDO topology shown in Figure1, based on a symmetrical Error Amplifier.

output capacitor, Cout. Therefore, it can be integrated on-chip, saving a pin and an external capacitor.

B. EA description

Figure 2 shows a transistor-level implementation of the LDO structure which is similar to the circuit presented in [5]. The error amplifier is implemented by using a symmetrical OTA: the input stage is formed by transistors M1, M2 which convert the differential input voltage into a circular current signal; this is taken in by three current mirrors (M4-M6, M3-M5 and M9-M10) which convert it into a single ended output current, available at node A. The input stage inherently symmetrical topology results in no/reduced systematic input offset voltage.

C. Current amplifier description

The input stage of the current amplifier is formed by the transistor M_{f1} in common source connection, around which the resistor Rf closes a feedback loop; this way both the input and output nodes of this stage have low impedance, suitable to current input and high-frequency operation. The second stage formed by M_{f2} and its cascode, M_{c2}, converts the voltage delivered by the first stage back into current, injected into node A, i.e. the output of the error amplifier. The cascodes M_{c1} and M_{c2} help reduce the difference of the drain-source voltages of M_{f1} and M_{f2}, thus reducing the offset of this circuit. The input stage is biased by the constant current source, Ibias2, while the second stage is biased via M10. As the later also sources current to the EA output stage its current drive has to be far larger than the current sunk from node A by transistor M6. This can be achieved by making M10 larger than M9; another possibility is to also make M5 larger than M6.

Besides Cf there are two more capacitors, Cf2 and Cf3, which help improve the AC stability.

D. Implementation of two LDOs with symmetrical EA

The first implementation of the LDO shown in Figure 2 was optimized for low-power consumption, while ensuring

that the output voltage ripple remains within the required limits. In this case the GBW of the main feedback loop - closed around the EA - has a fairly low value, 4MHz.

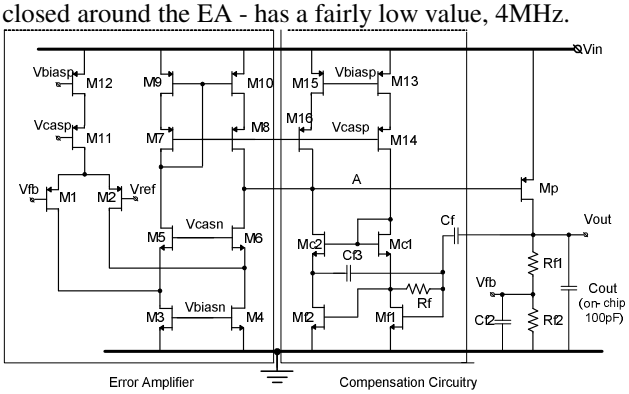


Figure 3: Circuit implementation of the LDO topology shown in Figure1, with a Folded-Cascode Error Amplifier

In order to assess the impact of the GBW over the LDO performance a second version was designed, for which the GBW was doubled. This involved increasing the current consumption and re-sizing both the compensation circuitry and the EA; noise reduction was also targeted.

Transistor sizes for the two implementations of the LDO with symmetrical EA, designed in a standard 0.18um CMOS process are given in Table 1, in columns 2 and 3. Resistors Rf1 and Rf2 have same values for all three LDO discussed here, 10kΩ and 20kΩ, respectively.

III. LDO WITH FOLDED-CASCODE ERROR AMP.

A. Brief description of the LDO with folded-cascode EA

Figure 3 shows the schematic of the third implementtation of the LDO topology shown in Figure 1: here a folded-cascode OTA was used to realize the EA.

Table 1. Transistor sizes for the LDO implementations based on Figure 2 (columns 2 & 3) and Figure3 (column 4)

Component name	Symmetrical EA low-power	Symmetrical EA larger GBW	Folded Cascode EA
	W(μm)/L(μm)	W(μm)/L(μm)	W(μm)/L(μm)
Mp	800/0.5	800/0.5	800/0.5
M1, M2	50/2	50/2	80/0.5
M3, M4,	4/2	4/2	40/2
M5	16/2	8/2	28/1
M6	8/2	8/2	28/1
M7	10/2	10/2	16/0.5
M8	5/2	10/2	16/0.5
M9	4/2	16/2	16/0.5
M10	28/2	80/2	16/0.5
M11, M12	-	-	16/0.5
M13, M15	-	-	24/0.5
M14, M16	-	-	80/0.5
Mf1	10/0.7	40/0.7	5/0.7
Mf2	20/0.7	40/0.7	5/0.7
Mc1	8/1	8/1	25/1
Mc2	16/1	8/1	25/1
Cf	4pF	2pF	4pF
Cf2	110fF	110fF	110fF
Cf3	6pF	1pF	2pF
Rf	15kΩ	3kΩ	10kΩ

Another difference is that both the input and the second stages of the compensation circuit are biased independently of the EA, by the cascaded current sources M13-M14 and M15-M16.

This circuit was designed to obtain the same output voltage ripple as the two LDOs discussed in the previous Section; also, the GBW of the main loop has the same value as the first LDO implementation, based on Figure 2. This allows us to study the impact the EA topology has on the entire LDO. Transistor sizes for this version, designed in the same 0.18um process, are given in the last column of Table 1.

B. Noise analysis of the capacitor-less LDO

Figure 4 presents a simplified equivalent circuit used to analyze the noise of the LDO shown in Figure 3.

Notation $\overline{dv}$ or $\overline{i_{out}^2}|_{DeviceA}$ represents the spectral density of the squared noise voltage or current source that models the noise of Device A.

By using standard circuit analysis [6], [7], [8] one can obtain the total voltage noise at the LDO output:

$$\begin{aligned}\overline{dv_{out\_LDO}^2} &= \overline{dv_{EA}^2}\cdot\left(1+\frac{R_1}{R_2}\right)^2 + \overline{dv_p^2}\cdot g_{mMp}^2\left[r_{dsp}\,\|\,(R_1+R_2)\right]^2 + \overline{dv_{R_1}^2} \\ &+ \overline{dv_{R_2}^2}\cdot\left(\frac{R_1}{R_2}\right)^2 + \overline{dv_{f1}^2}\cdot\left(\frac{g_{mMf1}}{g_{mM6}}g_{mMf2}R_X g_{mMp}R_{out}\right)^2 \\ &+ \overline{dv_{f2}^2}\cdot\left(g_{mMf2}R_X g_{mMp}R_{out}\right)^2 + \overline{dv_{Rf}^2}\cdot\left(\frac{g_{mMf1}}{g_{mM6}}g_{mMf2}R_X g_{mMp}R_{out}\right)^2 \\ &+ \left(\overline{di_{c1}^2}+\overline{di_{c2}^2}+\overline{di_{14}^2}+\overline{di_{16}^2}\right)\cdot R_X^2\left(g_{mMp}R_{out}\right)^2 \\ &+ \overline{dv_{13}^2}\cdot\left(g_{mM13}R_X g_{mMp}R_{out}\right)^2 + \overline{dv_{15}^2}\cdot\left(g_{mM15}R_X g_{mMp}R_{out}\right)^2\end{aligned} \quad (1)$$

where:

$$R_X = \underbrace{g_{m8}r_{ds8}r_{ds10}\,\|\,g_{m6}r_{ds6}r_{ds4}}_{\text{Error Amplifier Rout}}\,\|\,g_{m16}r_{ds16}r_{ds15}\,\|\,g_{mc2}r_{dsc2}r_{dsf2}$$

and $R_{out} = r_{dsp}\,\|\,(R_1+R_2)$ (2)

This analysis can be easily extended to the LDO shown in Figure 2, leading to the same conclusion: transistors Mf1 and Mf2 are significant contributors to the LDO noise, as their noise is conveyed to the LDO output with a large gain.

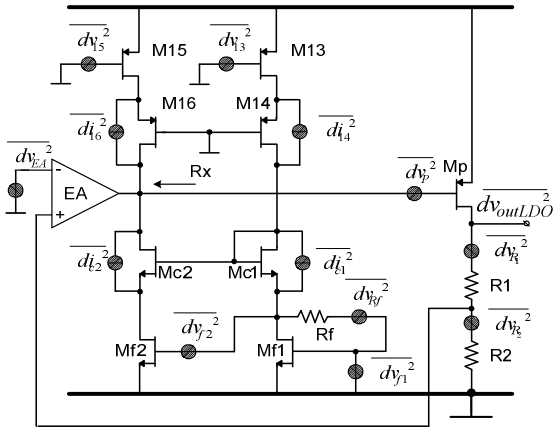


Figure 4: Equivalent circuit for noise analysis of the LDO implementation shown in Figure 3

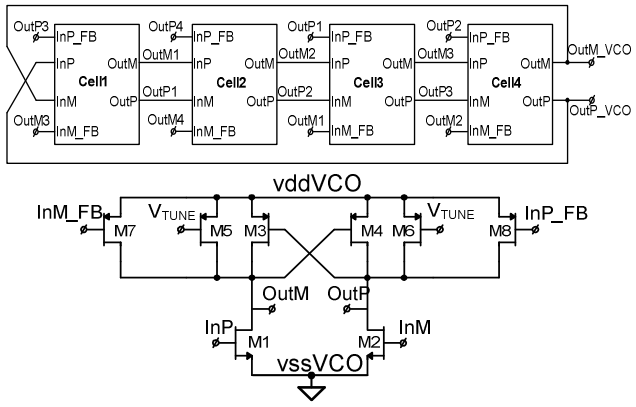


Figure 5. a). Block diagram of the rail-to-rail ring VCO supplied by the LDOs; b). Schematic of the delay-cell in a).

IV. BRIEF DESCRIPTION OF THE LOAD

A. Rail-to-Rail VCO

The purpose of the LDOs described here is to supply the rail-to-rail VCO shown in Figure 5. a), which operates at 2.5GHz. The VCO comprises four delay-cells connected in a multiple feedback topology; Figure 5. b) presents the schematic of the delay cell: it is build around the quasi differential input stage M1 and M2 and the cross-coupled latch formed by M3 and M4; M7 and M8 form the inputs for the secondary oscillator loop; the oscillating frequency is controlled by V_{TUNE} via M5 and M6 [9].

Quite often in practical circuits the main contributor to the VCO phase noise degradation is not the delay cell but the LDO which drives the VCO supply line. One needs to consider both the electrical noise generated by the LDO and the voltage supply ripple - the voltage variations due to the abrupt changes in the current the LDO has to accommodate when driving the rail-to-rail VCO. In our case, the VCO supply current varies between (almost) zero and 50mA.

As mentioned in the introduction, all three LDOs studied here were designed so that the voltage supply ripple has the same amplitude; this way the analysis can concentrate only on one aspect that is the electrical noise at the LDO output.

V. SIMULATION RESULTS

The main simulation testbench is shown in Figure 6: the LDOs under test are provided with a reference voltage and drive the rail-to-rail VCO shown in Figure 5.

All the results presented in this section were obtained by running Spectre simulations using Virtuoso Analog Design Environment (ADE-L) for all three LDO implementations.

A. The loop gain of the main control loop

Figure 7 presents the loop gain amplitude and phase characteristics with the VCO turned off – that is, the worst case situation with respect to the LDO stability, because with effectively no load the loop-gain is at maximum. All three LDOs are stable, but the phase margin (PM) of the symmetrical OTA with large GBW is fairly small, 29 dgr.

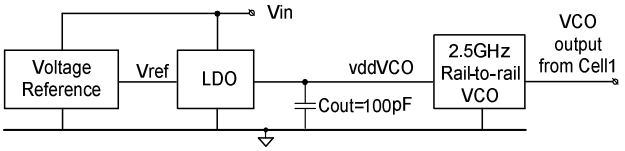


Figure 6: Test bench for the analyzed LDOs.

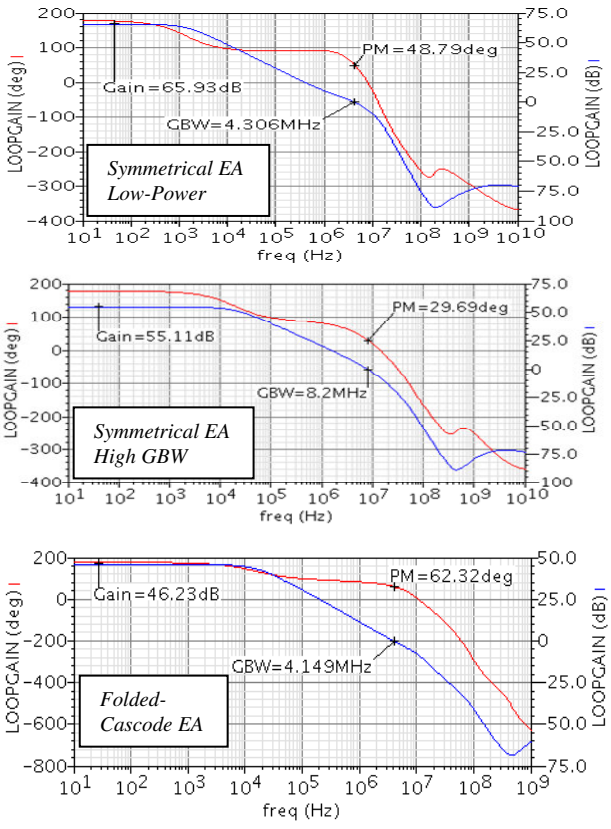


Figure 7: The loop gain frequency characteristics of the three LDO implementations, with the load turned off.

B. Standard LDO parameters

Figure 8 presents the PSRR of the three LDOs; al low frequency the LDO with folded-cascode EA achieves better PSRR than the first two LDOs but at 2.5GHz (the VCO frequency) the PSRR value is around -40dB for all LDOs. For ease of comparison of the PSRR parameter, multiple markers are placed in Figure 8 at key points of interest.

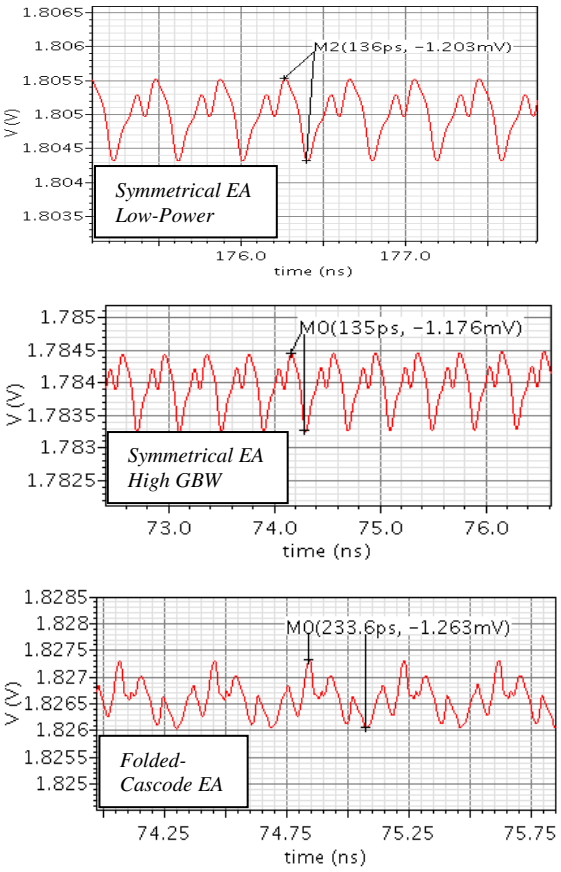
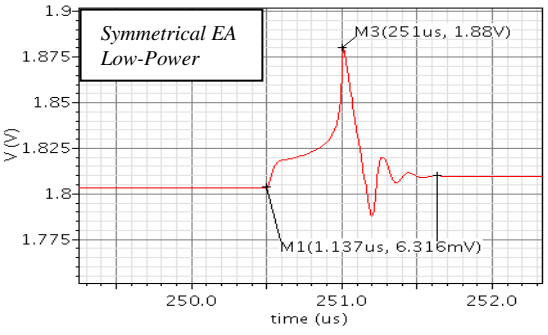


Figure 9: Ripple of the LDO output voltages when supplying the rail-to-rail VCO running at 2.5GHz



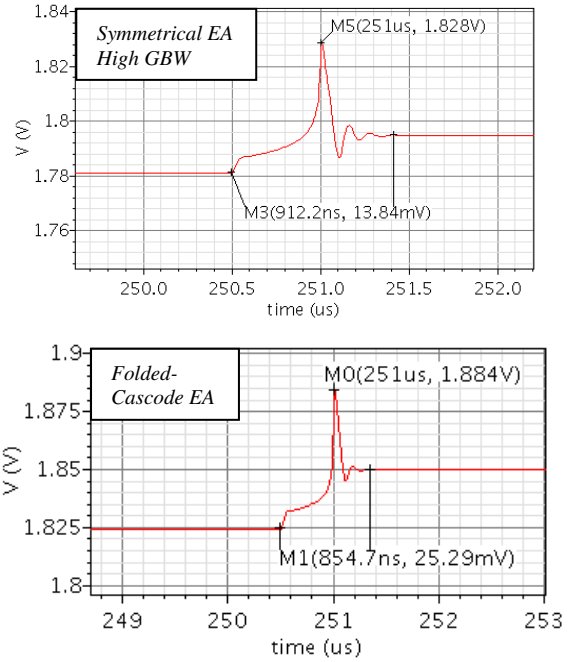


Figure 10: Load regulation and Settling time of the three LDOs; Iload was increased from 0 to 50mA in 500ns.

Figure 9 presents the variation of the LDO output voltage caused by the large variation of the supply current drawn by the rail-to-rail VCO running at 2.5GHz: note that for all three LDO implementations the voltage ripple is about 1.2mV, although only a small (100pF) internal capacitor is connected at the LDO output.

The load regulation of the LDOs, presented in Figure 10, was measured with the VCO replaced by a pulse current source, so that the load current can be varied between 50uA and 50mA with a 500ns rise time. Best result was obtained with the LDO employing the low power symmetrical EA: the output voltage varied only by 6mV. The other two LDO implementations showed significantly poorer load regulation.

Figure 10 also shows that the settling time is about the same for the three LDOs: around 1u. Note that the settling time of the LDO proposed in [5] is 15us.

C. LDO noise and VCO phase noise

Table 2 lists the first five noise contributors for the three LDO implementations.

Table 2: Top five contributors to the LDO output noise

Symmetrical EA Low-Power		**Symmetrical EA High-GBW**		**Folded-Cascode EA**	
Device	***%***	***Device***	***%***	***Device***	***%***
Mf1	34.8	M3	30.5	Mf2	44.9
M3	34.5	Mf1, Mf2	24.3	Mf1	44.7
Mf2	17	M5	15.6	M3, M4	3
M5	8.5	M4	1.3	M11, M12	0.5
M1, M2	0.9	M6	0.7	M9, M10	0.3

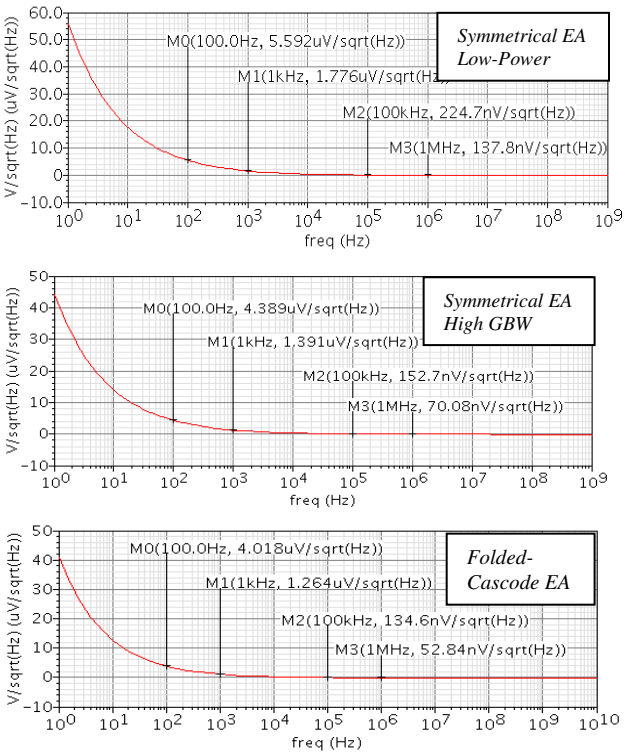


Figure 11: LDO output noise for a load current of 25mA

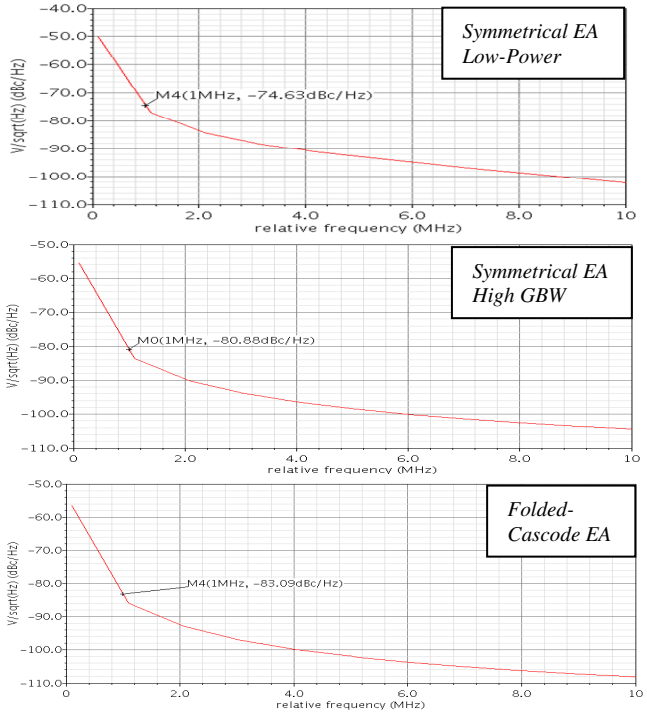


Figure 12: VCO phase noise when supplied by the three LDOs analyzed here

As predicted by the theoretical analysis in Section III.B the main transistors in the compensation network, Mf1 and Mf2 in both Figures 2 and 3, are major noise contributors. Other major contributors are transistors within current mirrors in the signal path of the EA.

Figure 11 presents the noise spectra at the output of the three LDOs analyzed here; as expected, the folded-cascode error amplifier presents the lowest noise, followed by the symmetrical EA with higher GBW (and power consumption) while the largest noise is recorded at the output of the LDO implemented with the low power symmetrical EA.

Note that the spot noise at 100Hz is about the same, around 4.5μV/√Hz. This is due to the fact that the flicker noise, dominant at low frequencies, is determined only by the transistors area and process parameters which are the same for all three LDOs.

At high frequencies the dominant factor is the thermal noise - which in general depends on the biasing current.

Table 3: Top five contributors to the VCO phase noise

Symmetrical EA Low-Power		**Symmetrical EA High-GBW**		**Folded-Cascode EA**	
Device	***%***	***Device***	***%***	***Device***	***%***
M3	31	M3	21.6	Mf1, Mf2	27.3
Mf1	20	Mf1, Mf2	15.8	M1*, M2* Delay Cell 2	3.5
Mf2	10	M5	10.1	M3, M4	1.8
M5	7.3	M1*, M2 Delay Cell 2	2.5	M1*, M2* Delay Cell 4	1.3
M1, M2	3.5	M1*, M2 Delay Cell 4	1.1	M1*, M2* Delay Cell 3	1.1

Table 4: Summary of simulation results

Name	[5]	Symm. EA, low power	Symm. EA, high GBW	Folded Cascode
Year	2007	This work	This work	This work
CMOS [μm]	0.35	0.18	0.18	0.18
Supply Voltage [V]	3	3.3 - 5	3.2 - 5	2.8 - 5
Output Voltage [V]	2.8	1.8	1.8	1.8
Iout_max [mA]	50	50	50	50
Iquiescent [μA]	65	85	280	240
Ibias_EA [μA]	NA	4	60	100
Settling Time [μs]	15	1.1	0.91	0.85
Line regulation [mV/V]	NA	10	10	0.49
Load regulation [mV/mA]	NA	0.11	0.27	0.5
PSRR (@ 1kHz) [dB]	-57	-40	-40	-62
GBW of main loop [MHz]	0.22	4.3	8.2	4.1
EA noise [μV/√Hz] *@ 100Hz **@ 100kHz	~4* ~0.5**	1.75* 0.13**	1.78* 0.64**	0.13* 0.02**
Output noise [μV/√Hz] *@ 100Hz **@ 100kHz	4.6* 0.6**	5.59* 0.22**	4.38* 0.15**	4* 0.13**
Phase noise @ 1MHz [dBc/Hz]	NA	-74	-80	-83

The lowest spot noise at 1MHz – but it has the highest current consumption, around 100uA; the second-lowest noise is given by the high-GBW symmetrical EA, which consumes around 60uA, while the low-power symmetrical EA is the noisiest but only burns 4uA. However, the overall power consumption of the LDOs is not as widely spread – see row seven in Table 4.

Figure 12 presents the phase noise of the VCO shown in Figure 5, when supplied by the three LDOs under discussion.

There is a clear correlation between the results shown in Figs. 11 and 12: the noisier the EA, the worst the VCO phase noise performance. In fact, the distance between the VCO phase noise values at 1MHz and the distance between the spot noise of the LDOs at 1MHz match almost dB-for-dB. Table 3 lists the top five noise contributors of the VCO. A summary of simulation results for the three LDOs is given in Table 4.

VI. CONCLUSIONS

This paper presents three implementations of an LDO structure that requires only a small, integrable, decoupling capacitor, but is able to drive dynamic loads, which impose large and fast variations of the supplied current. The LDO structure is similar to the conventional LDO topology, except it has an additional compensation network around the pass transistor that ensures the fast charge/discharge of the gate capacitance of the pass transistor during transients.

This LDO structure was selected from the many "capacitor-less" solutions proposed in the literature as the best suited to supply a rail-to-rail VCO operating at 2.5GHz, with the supply current varying abruptly between 50uA and 50mA. The main requirements were to maintain the ripple of the output voltage bellow 1.5mV and minimize the impact the LDO had on the VCO Phase Noise.

First, a circuit implementation close to the one reported in the literature was analyzed: it used a symmetrical OTA as the EA of the LDO. Two versions of this circuit were designed in a standard 0.18um CMOS process: one optimized for low power consumption and the other for higher GBW and lower noise.

The third implementation of the LDO structure used a folded-cascode EA; it was designed to provide the same output voltage ripple as the previous two LDOs; also, the GBW of the main loop had the same value as the first LDO implementation. The noise at the LDO output was reduced. The pass transistor had the same size for all three LDOs.

The analysis focused on the effect the LDOs have on the phase noise of the VCO they supply. No correlation between the GBW of the control loop and the VCO phase noise was found. Instead, a direct link was found between the high-frequency noise spot noise at the LDO output and the VCO phase noise.

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