32x32 PARALLEL ANALOG ARCHITECTURE FOR IMAGE PROCESSING USING LOG DOMAIN ACTIVE PIXEL

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Abstract: In this paper the transistor level simulation of a 32x32 analog parallel architecture of Cellular Neural Network (CNN) type able to perform spatial filtering operations is reported. The circuit level implementation is obtained by the log-domain mapping of the linear equations describing the CNN by using MOS transistors biased in weak inversion. The spatial filter is simulated in a 340nm CMOS technology. In the last part of the paper several examples of image processing operations like smoothing and edge detection using a chessboard type input image are presented.

Keywords: *spatial filtering, log-domain, image processing, smoothing, edge detection.*

I. INTRODUCTION

The dynamics of analog parallel architectures [1-17] has been proved to be useful for image spatial linear or nonlinear filtering applications. For piecewise linear cells working in the central linear part of their characteristics such parallel architectures can be described by a system of coupled linear differential equations, which can be solved using the decoupling techniques reported in [15-17]. The implementation of such CNN's can be based on voltage controlled current sources. By implementing each voltage controlled current sources with operational transconductor amplifiers (OTAs), a low resolution spatial filter was realized and reported in [18]. However, the great amount of pixel level power consumption was the main inconvenience of OTA implementation [18-20].

In this paper the log-domain mapping of linear equations has been used for operating in current mode with low power consumption while preserving the overall linearity (input-state-output for non-autonomous systems, respectively state-output for the autonomous ones) [21].

By log-domain mapping of the linear differential system equations, a nonlinear differential system of equations is obtained. The associated circuit can be implemented using MOS transistors biased in weak inversion. Thus, low power high resolution spatial filters can be obtained [21, 22].

By expanding the one-dimensional network reported in [22], a 2D system capable to perform elementary operations of image filtering has been obtained.

The resolution of the proposed filter is 32x32 pixels. Figure 1 presents the architecture of an active pixel, considering that each one is connected with one or two nearest neighbors. Thus, the differential linear equation which corresponds to (i, j) node has the form:

$$C\frac{dx_{i,j}(t)}{dt} = A_{lf2}x_{i-2,j} + A_{lf1}x_{i-1,j} - A_0x_{i,j} + A_{rg1}x_{i+1,j} + A_{rg2}x_{i+2,j} + A_{up2}x_{i,j+2} + A_{up1}x_{i,j+1} + A_{dw1}x_{i,j-1} + A_{dw2}x_{i,j-2}, \quad \forall i,j = 0..M\text{-}1 \quad (1)$$

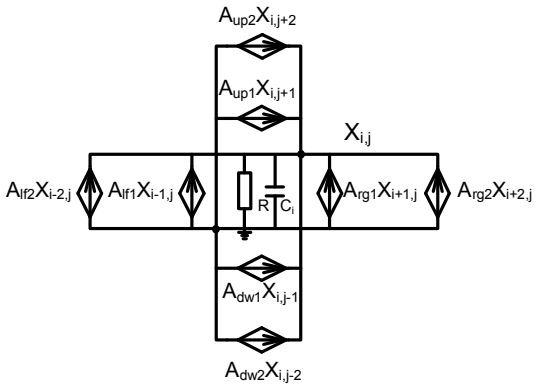

Figure 1. 2D network architecture

Depending on the values of the template parameters, the 2D spatial filter, simulated at system level with voltage controlled current sources as well as at transistor level in log-domain, can be configured to realize low-pass, high-pass, stop-band and band-pass filtering operations.

The most used elementary operations in image processing are *smoothing* and *edges extraction*. The input image is provided by the imager and is loaded as initial conditions of the cell capacitors. The smoothing operation can be made by low-pass filtering.

The most important effect of this type of spatial filtering besides *blurring* is *noise cancellation*. Moreover, *edges extraction* can be realized by high-pass filtering.

Digital processors realize the above operations with a much higher amount of power, time and area consumption. The configurable analog filter proposed is optimized to perform real time filtering, using minimum power consumption.

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II. LOG-DOMAIN MAPPING OF LINEAR STATE EQUATIONS OF A 2D AUTONOMOUS SYSTEM

In the following, the log-domain design of the 2D linear spatial filter will be described. The log-domain mapping of a linear autonomous system is based on the theory of non-autonomous ones [20]. The autonomous system is described by a set of state equations as follows:

$$\begin{cases} \dot{X} = AX \\ Y = CX \end{cases} \quad (2)$$

where "X" is an M^2 column state vector, "A" is the M^2xM^2 state transition matrix and "C" the output matrix relating the state to the output "Y" .

In the case of a log-domain circuit version, the state-output overall linearity is preserved. Suppose that we are dealing with a homogeneous network, $A_{lf1}=A_{rg1}=A_{up1}=A_{dw1}=A_1$; $A_{lf2}=A_{rg2}=A_{up2}=A_{dw2}=A_2$, with ring boundary conditions. In this case equation (1) becomes:

$$C\frac{dx_{i,j}(t)}{dt} = A_2(x_{i-2,j} + x_{i+2,j} + x_{i,j-2} + x_{i,j+2}) + A_1(x_{i-1,j} + x_{i+1,j} + x_{i,j-1} + x_{i,j+1}) - A_0 x_{i,j},\ \forall i,j = 0..M\text{-}1 \quad (3)$$

In the above linear system for the discussed architecture, "$x_{i,j}(t)$" has the significance of voltage.

Applying the log-domain mapping of the linear state-output systems [20], the following change of variable can be used:

$$x_{i,j}(t) = I_S e^{\alpha v_{x,ij}(t)} \quad (4)$$

Hence, from now on "$x_{i,j}(t)$" will be considered as a current. Moreover the notations $x_{i,j}(t)=x(i,j)$ and $v_{x,ij}(t)=v_x(i,j)$ will be used. Since x(i,j) should be positive for any t>0, an offset for avoiding static convergence problems [20, 21] is introduced:

$$x(i,j) = I_S e^{\alpha v_x(i,j)} - I_S \quad (5)$$

Applying the above change of variable the state equations (3) can be written as follows so that they will have an acceptable DC solution [21]:

$$CI_S\alpha \dot{v}_x(i,j)e^{\alpha v_x(i,j)} = A_2 I_S(e^{\alpha v_x(i-2,j)} + e^{\alpha v_x(i+2,j)} + e^{\alpha v_x(i,j-2)} + e^{\alpha v_x(i,j+2)}) + A_1 I_S(e^{\alpha v_x(i-1,j)} + e^{\alpha v_x(i+1,j)} + e^{\alpha v_x(i,j-1)} + e^{\alpha v_x(i,j+1)}) - A_0 I_S e^{\alpha v_x(i,j)} - I_S(4A_1 + 4A_2 - A_0) \quad (6)$$

Dividing the nodal equation (5) by $e^{\alpha v_x(i)}$ and using the notations:

$$C_x = CI_S\alpha$$
$$x_{offset} = I_S(4A_1 + 4A_1 - A_0) = I_{X_0}$$
$$A_1 I_S = I_{A_1};\ A_2 I_S = I_{A_2};\ A_0 I_S = I_{A_0}$$

the new (i,j) state equation takes the form :

$$C_x \dot{v}_x(i,j) = coupling - I_{X_0} e^{-\alpha v_x(i,j)} \quad (7)$$

where

$$coupling = I_{A_2}(e^{\alpha(v_x(i-2,j)-v_x(i,j))} + e^{\alpha(v_x(i+2,j)-v_x(i,j))} + e^{\alpha(v_x(i,j-2)-v_x(i,j))} + e^{\alpha(v_x(i,j+2)-v_x(i,j))}) + I_{A_1}(e^{\alpha(v_x(i-1,j)-v_x(i,j))} + e^{\alpha(v_x(i+1,j)-v_x(i,j))} + e^{\alpha(v_x(i,j-1)-v_x(i,j))} + e^{\alpha(v_x(i,j+1)-v_x(i,j))}) - I_{A_0}$$

The above equation represents Kirchhoff II law for cell (i,j): the current through the capacitance $C_x(i,j)$ is equal with the sum of the currents sourced by the exponential voltage controlled current sources. The so called "coupling" term represents the influence of the neighboring cells on the cell (i,j). Each term from "coupling" has the meaning of a non-linear equivalent, in logarithmic domain, of the voltage controlled current sources, while $I_{X_0}e^{-\alpha v_x(i,j)}$ term defines a non-linear conductance.

III. CIRCUIT IMPLEMENTATION

From the structural point of view, an active pixel obtained by the non-linear mapping of the linear state equations of an autonomous system, contains two non-linear conductances, eight exponentially voltage controlled current sources, and one DC current source, as shown in Figure 2.

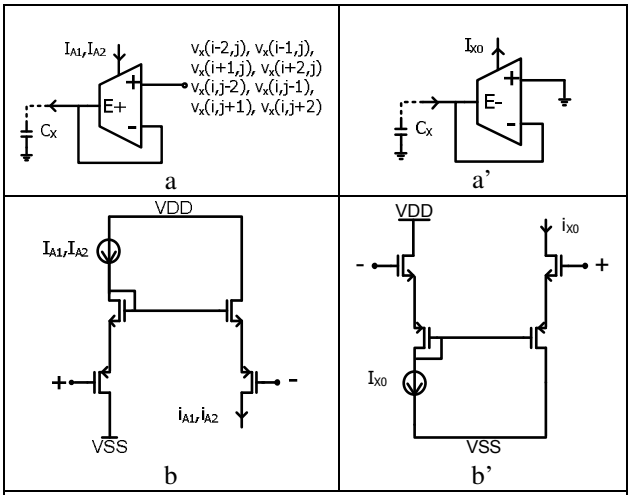


Figure 2. ***a)*** *Exponential voltage controlled current sources, which pushes current into a capacitive load;* ***a')*** *exponential voltage controlled current sources, which pulls out current from a capacitive load;* ***b)*** *CMOS transistor implementation of the non-linear positive voltage controlled current sources;* ***b')*** *CMOS transistor implementation of the non-linear negative voltage controlled current sources*

The nonlinear sources at system level in Figure 2 a, a', and at transistor level in Figure 2 b, b', have three current inputs (I_{A1}, I_{A2}, I_{X0}) and two voltage inputs (v_+, v_-).

Taking into account the previous observations, the schematic of a logarithmic active pixel can be easily deduced from equation (7) and is presented in Figure 3.

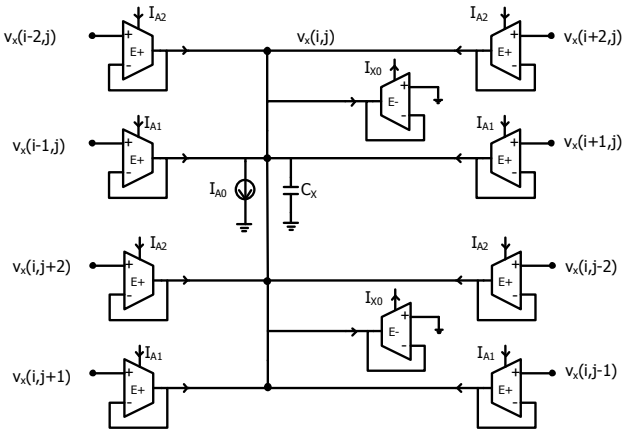


Figure 3. Log-domain 2D pixel structure

The above structure implements a high-pass filter (HPF) for $v_x(i-2,j)= v_x(i+2,j)= v_x(i,j-2)= v_x(i,j+2)=0$ and $v_x(i-1,j)= v_x(i+1,j)= v_x(i,j-1)= v_x(i,j+1)\neq 0$ and a band-pass filter (BPF) for $v_x(i-2,j)= v_x(i+2,j)= v_x(i,j-2)= v_x(i,j+2)\neq 0$ and $v_x(i-1,j)= v_x(i+1,j)= v_x(i,j-1)= v_x(i,j+1)=0$.

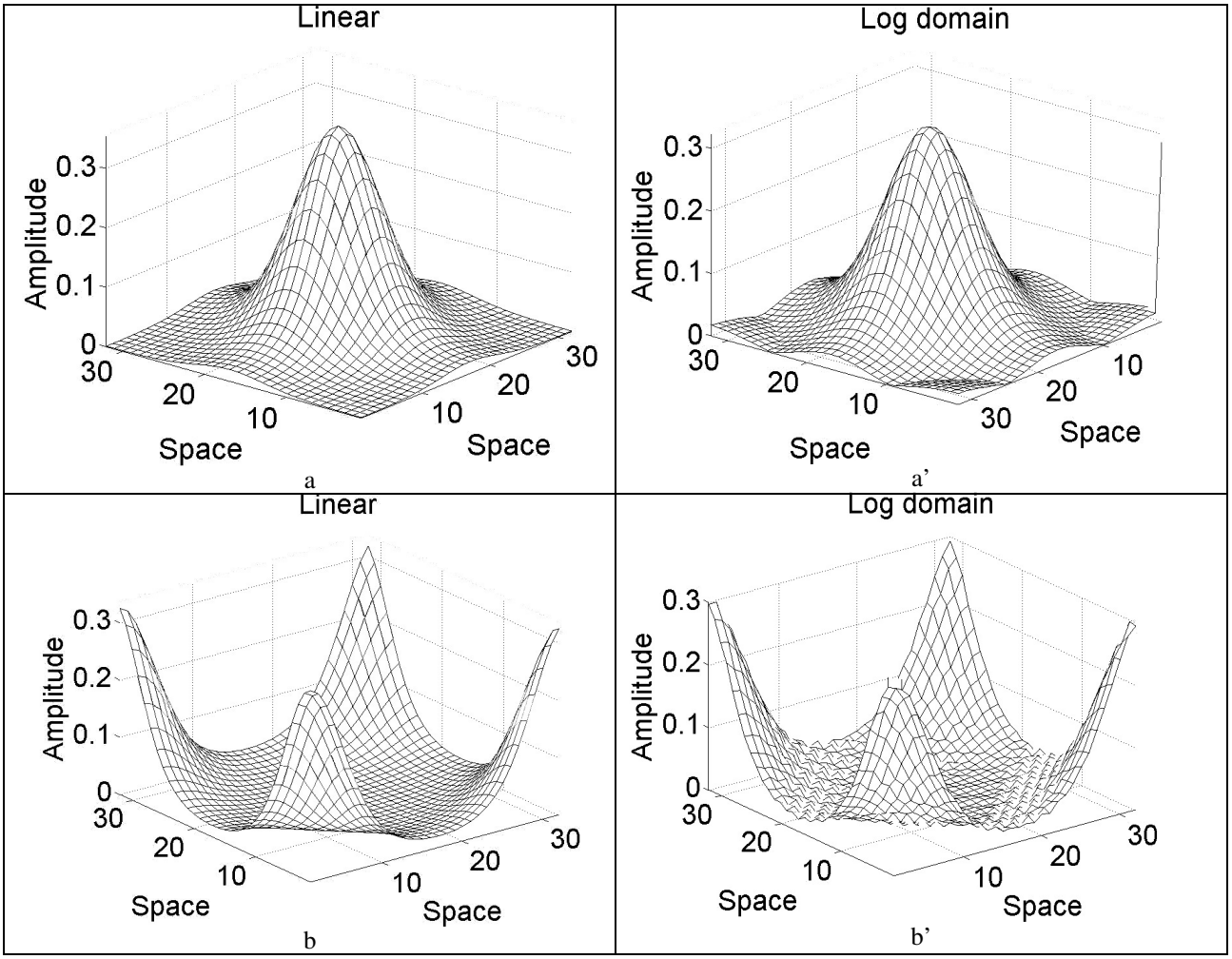
The topology for the log-domain active pixel for a low-pass filter (LPF) and stop-band filter (SBF) can be easily obtained by multiplying equation (7) by -1, which is equivalent at the circuit level presented in Figure 3, with changing the "E+" current sources with "E-" ones.

In the design of the non-linear voltage controlled current sources, a special care has to be taken regarding the transistors aspect ration, meaning that their widths should be as short as possible to minimize the parasitic capacitance, and the load capacitance must be larger than the equivalent parasitic capacitance in each node of the network; otherwise, the system will not fit the dynamic described by the mapping equations. On the other hand, the canal length must be long enough to enhance linearity and compensate the variations of the threshold voltage which are significantly affected by process parameter variations and mismatch when the MOS transistor is biased in weak inversion.

The pixel level current consumption for the 2D network, for any of the four possible configurations, is about 9nA; hence, the current consumption for the entire 32x32 spatial filter is about 9,2uA. The circuit is supplied by a +/-900mV DC voltage.

IV. SIMULATION RESULTS

In the following, we will compare the frequency characteristics for the ideal linear filters and the log-domain transistor level ones, both configured to perform all kinds of filtering operations.



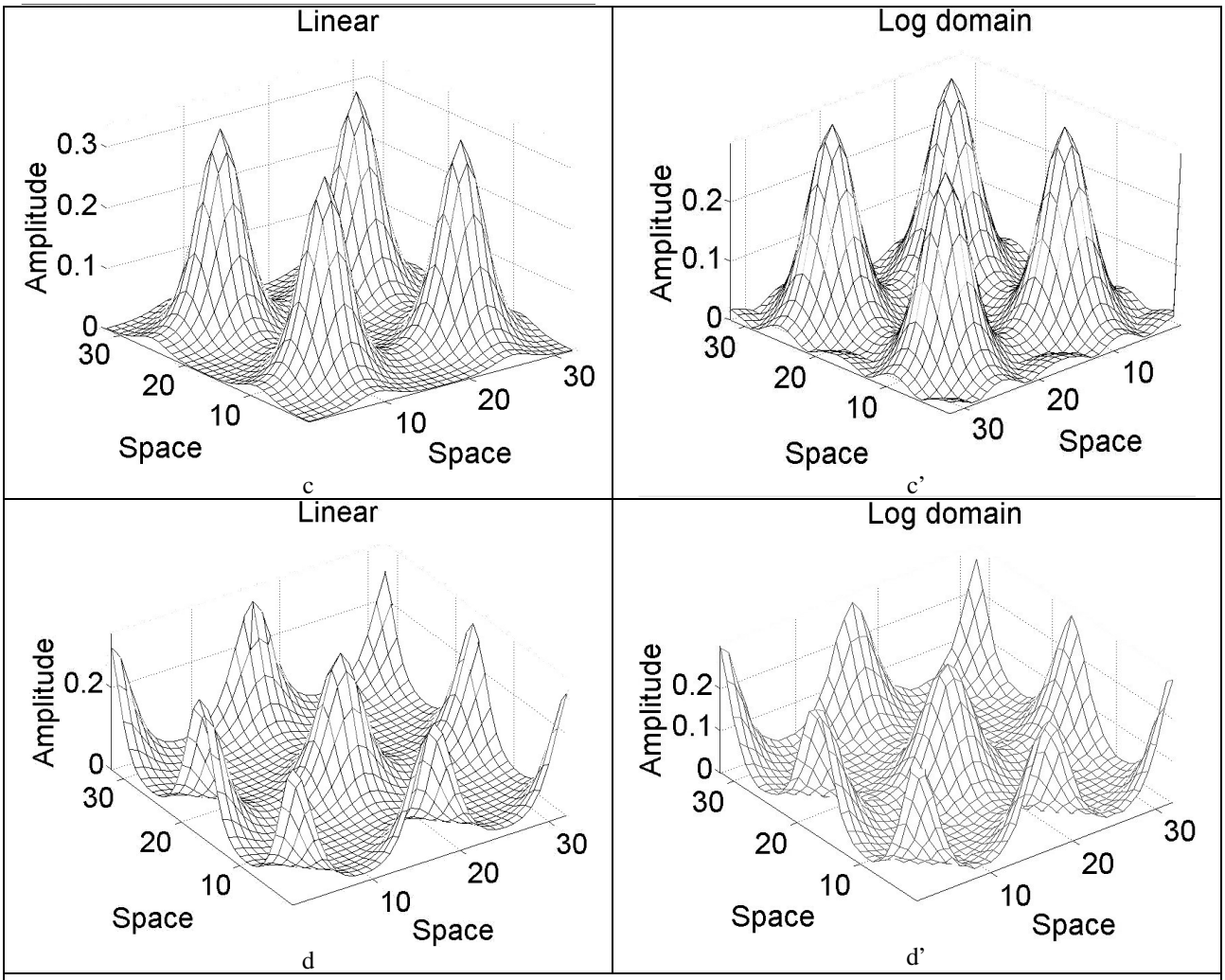


Figure 4. ***a,b,c,d)*** *spatial frequency characteristics of the linear ideal spatial filter;* ***a',b',c',d')*** *spatial frequency characteristics of the log-domain transistor level spatial filter;* ***a,a')*** *HPF;PSNR around 42dB;* ***b,b')*** *LPF; PSNR around 24dB;* ***c,c')*** *BPF; PSNR around 40dB;* ***d,d')*** *SBF; PSNR around 24dB*

For the sake of simplicity, we will consider the A_0 term equal to zero. The spatial frequency characteristics can be read from Figure 4 by keeping only the [0..15; 0..15] spatial modes. The spatial frequency characteristics presented in Figure 4 were obtained by seeding both the ideal and the transistor level networks with a 20mV spatial impulse initial condition. The dynamics of both filters were "frozen" at 140us.

The table below shows the template parameters values for different kinds of spatial filtering for both networks.

Filter type	Freq. characteristic	Implementation type					
		Log-domain transistor level filter				Ideal filter	
		Filter coefficients					
		I_{X0}	I_{A0}	I_{A1}	I_{A2}	A_1	A_2
FTS	Fig. 4a/a'	2nA	0	1nA	0	1nS	0
FTB	Fig. 4c/c'	2nA	0	0	1nA	0	1nS
FTJ	Fig. 4b/b'	2nA	0	1nA	0	-1nS	0
FOB	Fig. 4d/d'	2nA	0	0	1nA	0	-1nS

As a practical application of the proposed spatial filter, we illustrate the *smoothing* and *edges extraction* operations. Both networks were loaded with the same 32x32 pixels chessboard type input imagine, as shown in Figure 5.

As it was discussed above, for edges extraction, both networks were set to have a high-pass behavior. The results presented in Figure 6b, b' were read after 43us.
Hence, the filters parameters suitable to process a smoothed version of the input image by a low-pass filtering, can be picked from the above table. Also the dynamics of both systems were "frozen" at 43us.

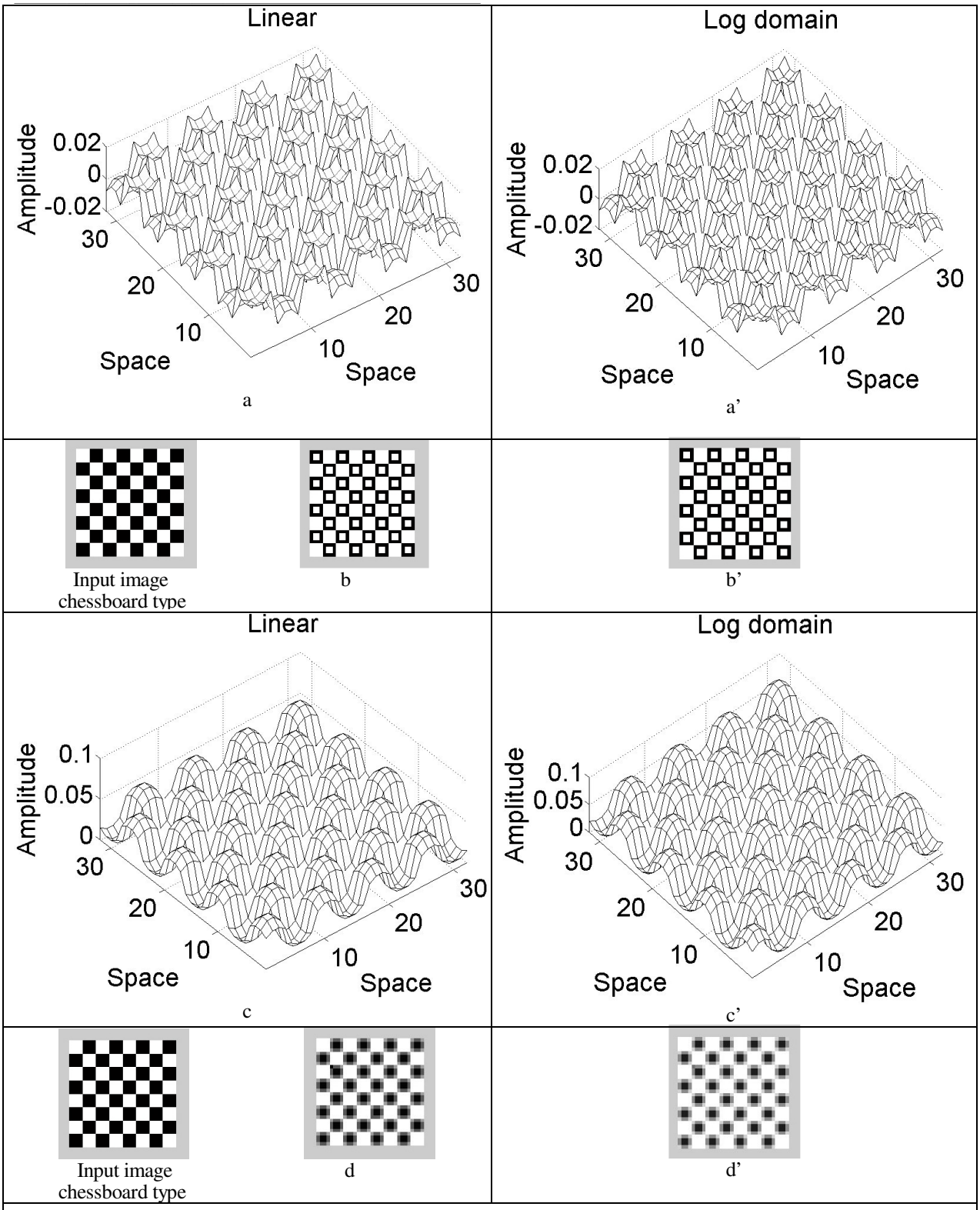


Figure 5. ***a,a')*** *the map of voltage values of each pixel, after 43us, both filters being high-pass configured; the PSNR obtained for these two high-pass filtred versions is around 20dB;* ***b,b')*** *edges extraction from chessboard image, after 43us (2D view); the PSNR obtained for these two high-pass filtred versions is around 30dB;* ***c,c')*** *the map of voltage values of each pixel, after 43us, both filters being low-pass configured;* ***d,d')*** *smoothed image obtained with both filters, after 43us (2D view).*

Figures 6a, b, c, d were obtained with ideal linear filters and 6a', b', c', d' with log-domain transistor level filters.

V. CONCLUSION

In this paper an implementation at system level and log-domain transistor level of a 32x32 spatial filter based on a CNN analog parallel architecture was presented. The nonlinear equations obtained by the log-domain mapping of the linear ones, were implemented with MOS transistors biased in weak inversion.

The simulations results showed that both kinds of filter exhibit the same behavior. Although the initial states loaded on the capacitance of each cell are nonlinearly processed, the whole filter preserves the input-output overall linearity.

The advantages of the proposed filter concern area (the log-domain cells need less silicon area) and power consumption (a log-domain cell consumes roughly less than 1% of a standard cell).

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REFERENCES

[1] L. O. Chua, L. Yang, "Cellular Neural Networks: Theory", IEEE Trans. Circuits Syst., vol. 35, no 10, pp. 1257-1272, October 1988.

[2] L. O. Chua, L. Yang, "Cellular Neural; Networks: Applications", IEEE Trans. Circuits Syst., vol. 35, no 10, pp 1273-1290, October 1988.

[3] T. Roska, J. Vanderwalle, Cellular Neural Networks, John Wiley & Sons, 1993.

[4] K. R. Crounse, L. O. Chua, "Methods for image processing and pattern formation in Cellular Neural Networks: A Tutorial", ", IEEE Trans. Circuits Syst, vol.42, no. 10, pp. 583-601, October 1995.

[5] L. O. Chua, M. Hasler, G. S. Moschytz and J. Neirynck, "Autonomous Cellular Neural Networks: A Unified Paradigm for Pattern Formation and Active Wave Propagation, IEEE Trans. Circuits Syst, vol. 42, pp. 559-577, October 1995.

[6] K. R. Crounse, L. O. Chua – "Methods for Image Processing and Pattern Formation in Cellular Neural Networks – A Tutorial", IEEE Transactions on Circuits and Systems, Special Issue on Nonlinear Waves, Patterns and Spatio-Temporal Chaos in Dynamic Arrays, vol. 42, number 10, pp. 583-601, October 1995.

[7] T. Roska, L. O. Chua, "On a Framework of Complexity of Computation on Flows Implemented on the CNN Universal Machine" Technical Report, DNS-15-1995, Computer and Automation Institute, Budapest,.

[8] T. Roska, L. O. Chua, D. Wolf, T. Kozek, R. Tetzlaff, F. Puffer, "Simulating Nonlinear Waves and Partial Differential Equations via CNN – Part I: Basic Technique", IEEE Trans. Circuits Syst. I, vol.42, pp. 807-815, October 1995.

[9] A. Zarandy, T. Roska – "CNN Template Design Strategies and Fault Tolerant CNN Template Design – A Survey", Proc. of the European Conference on Circuit Theory and Design, ECCTD, pp 178-201, Budapest, 1997.

[10] B. E. Shi, "Gabor-type filtering in space and time with cellular neural networks", IEEE Trans.on Circuits and Syst., Vol. 45, No. 2, February 1998.

[11] Bing J. Sheu. Kwang-Bo Cho, Wayene C Young, "Integration of Sensor/Processor under Cellular Neural Networks Paradigm for Multimedia Applications", Proceedings of the Fifth IEEE International Workshop on Cellular Neural Networks and Their Applications, 14-17 April 1998, pp 45-49, London, UK.

[12] M. Frasca, P. Arena, L. Fortuna. Bio-Inspired Emergent Control Of Locomotion Systems. World Scientific Series on Nonlinear Science, Series A - Vol. 48, 2004.

[13] P. Arena, L. Fortuna, M. Frasca and G. Sicurella. An Adaptive, Self-Organizing Dynamical System for Hierarchical Control of Bio-Inspired Locomotion. IEEE Transactions On Systems, Man, And Cybernetics Part B: Cybernetics, 34, No. 4, pp. 1823–1837, 2004.

[14] L. Gora□, L. O. Chua, D. M. W. Leenaerts, "Turing Patterns in CNN's-Part I: Once Over Lightly", IEEE Trans. Circuits Syst, vol.42, pp. 602-611, October 1995.

[15] L. Goraş, L. O. Chua, "Turing Patterns in CNN's - Part II: Equations and Behaviors", IEEE Trans. Circuits Syst, vol.42, pp. 612-626, October 1995.

[16] L. Goraş, "On Pattern Formation in Cellular Neural Networks", NATO Advanced Research Workshop, Siena, Italy, 22-24 October, 2002; published in V. Piuri , M. Gori , S. Ablameyko and L. Goras, (editors) "Limitations and Future Trends in Neural Computation", Volume 186 NATO Science Series: Computer & Systems Sciences;

[17] L. Gora□, "Spatio temporal dynamics in analog parallel architectures", The Second International Symposium on Electrical and Electronics Engineering – ISEEE-2008, Galati, Romania

[18] L. Gora□, I. Alecsandrescu, I. Vornicu, "Spatial filtering using linear analog parallel architesctures ", International Symposiunm on Signals, Circuits and Systems ISSCS, Ia□i, Romania, Vol 2, pp. 409-412, 2009

[19] I. Vornicu, "CMOS technology implementation of analog parallel architectures used in spatial filtering", Workshop ISSCS, Ia□i Romania (communicated), 2009

[20] I. Vornicu, "Mapping of linear differential equations in logarithmic domain", Workshop ISSCS, Ia□i, Romania (communicated), 2009

[21] A. Rodriguez – Vazquez, T. Serrano – Gotarredona, "On the design of second order dynamics reaction-diffusion CNNs", Journal of VLSI Signal Processing 23, 351-371, 1999

[22] L. Goras, I. Vornicu, "Log domain implementation of a class of analog parallel architectures" International Semiconductor Conference (CAS), Vol. 2, pp. 499-502, 2009