AN EXPERIMENTAL ANALYSIS OF SIGNAL REFLECTIONS ON PRINTED CIRCUIT BOARD TRANSMISSION LINES

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Abstract: Signal reflections for several digital integrated circuit families are experimentally analyzed by using high-speed time domain measurements. Four test setups are designed and fabricated - the interconnect lines have different geometrical parameters. The signals that are transmitted on the line are measured using a high-performance digital oscilloscope. Each board is successively equipped with ICs from the analyzed families. Simulation results are presented in comparison with experimental results. It is shown that the circuit model must be in accordance with the manufacturer specifications in order to obtain valid simulation results.

Keywords: *signal reflections, microstrip, transmission line, time domain measurement.*

I. INTRODUCTION

The explosion of the information technology has led to the necessity of developing high performance structures that ensure reliable high-speed data transmission. In these conditions, signal integrity analysis plays an important role in the high-speed design process to guarantee the correct operation of electrical systems. Design engineers must consider two aspects: 1) the timing, which depends on the delay caused by the transmission line length through which the signal must propagate, and 2) the quality of the signal - the shape of the waveform when the threshold is reached. Signal waveform distortions can have different causes: reflections, crosstalk, power/ground noise [6]. The purpose of this paper is to analyze the distortions caused by reflections. Reflection is a well-known transmission line effect caused mainly by impedance mismatch (stubs, vias and other discontinuities on the transmission media, driver/load impedance). Since the signals travel through all kinds of interconnections inside a system, any electrical impact happening at the source end, along the path, or at the receiving end, will have great effects on the signal timing and quality [6]. Due to signal reflections the time delay increases and overshoot, undershoot and ringing are also produced.

In this paper, signal reflections at PCB level are analyzed. Four PCBs were designed and equipped with digital ICs from different families. The circuit consists of a driver and a receiver connected by a transmission line (Figure 1). The length of the t-line is chosen in the range of tens of centimeters to be able to illustrate the propagation delay. The digital ICs were chosen from families that have switching times in the range of nanoseconds. At PCB level there are different types of interconnects: microstrip, stripline, embedded stripline and others. For this study, the microstrip line was chosen as the electrical path that conducts the signal.

The factors that could generate reflections were reduced as much as possible. There are no vias or stubs on the transmission line. No other trace is routed in the vicinity of the analyzed t-line. Several decoupling capacitors are mounted to reduce the power/ground bounce. The ground plane, that together with the trace forms the microstrip structure, minimizes also the reflections. In the paper it is also illustrated that choosing the appropriate termination scheme minimizes reflection noise.

Besides the practical measurements, simulations with a SPICE type circuit simulator were also performed. Some of the results that were obtained are presented in section IV.

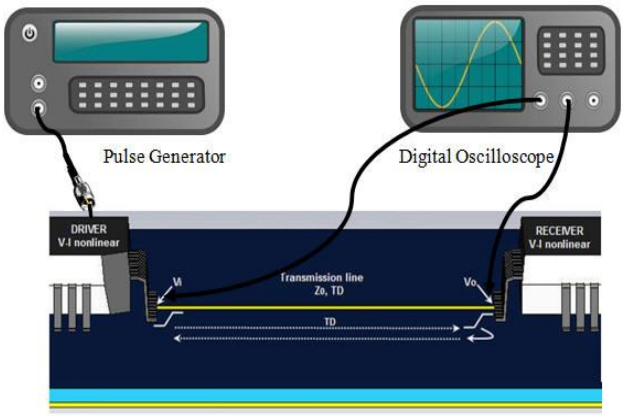

Figure 1. Measuring the signal reflection.

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II. HARDWARE SETUP

The measurement setup is shown in Figure 1, where the signal from the pulse generator is applied to the input pin of a driver IC. The output pin is connected to the receiver IC through a transmission line – microstrip. The relative dielectric constant of the 1.5748mm thick dielectric medium is 5.4. The thickness of the Copper layer is 35µm. Using a digital oscilloscope the waveforms at the extremities of the line are recorded. The electrical diagram corresponding to this hardware setup is presented in Figure 2.

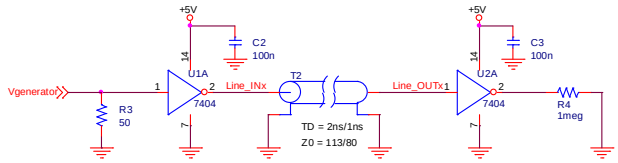

Figure 2. Measuring the signal reflection.

For each family, the signal from the generator was first applied to the input of one gate having the output connected to a load resistor (100MΩ or the value indicated in the datasheet), as shown in Figure 3. This was done in order to check if the PSpice model is built in accordance with the gate switching characteristics given by the manufacturer.

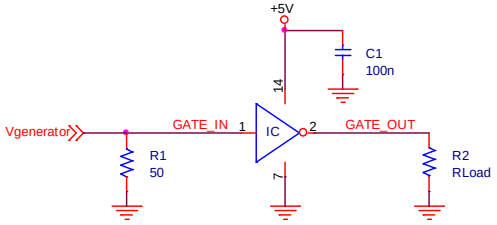

Figure 3. Determination of the switching characteristics.

Figure 4 shows the layout design of the setup that was analyzed.

Table 1 presents the geometrical parameters of the four microstrip lines (w-width of the track, L –length of the track) and the corresponding calculated electrical parameters that were used in the simulations (Z_0 – characteristic impedance, TD – propagation delay).

The most widely accepted microstrip line equations come from H. Sobol [1]. They appear in Motorola application note AN-548A and many other sources.

$$Z_0 = \frac{377h}{\sqrt{\varepsilon_r} w_{eff}\left[1+1.735(\varepsilon_r)^{-0.0724}\left(\frac{w_{eff}}{h}\right)^{-0.836}\right]} \quad (1)$$

$$w_{eff} = w + \frac{t}{\pi}\left[\ln\left(\frac{2h}{t}\right) + 1\right] \quad (2)$$

The propagation delay is computed according to formula:

$$TD = 3.334 \cdot \sqrt{0.475 \cdot \varepsilon_r + 0.67}[ns/m] \quad (3)$$

Table 1. Parameters of the four setups.

Setup	w[mm]	L[cm]	Z_0[Ω]	TD[ns]
1	0.3	35	113	2
2	0.9	35	80	2
3	0.3	17.5	113	1
4	0.9	17.5	80	1

As signal generator, a Hewlett Packard 8082A Pulse Generator was used. This instrument produces pulses in the range 0.5 to 5V at repetition rates up to 250MHz. Pulse-width is variable from 2ns to 5ms with transition times controllable from 5ms all the way down to less than 1ns. It can function as a pulse shaper to control the amplitude and transition times of pulses applied to the input of the ICs. Of particular importance when working with very fast circuits, the pulse generator presents a well-matched source impedance to external 50Ω circuits (less than 2% reflection with pulse amplitudes up to 4V).

The 50Ω output was connected through a coaxial cable to the input of the ICs. For impedance matching of this transmission line, a 50Ω resistor was connected to ground on the PCB (R3 and R1 in Figure 2 and Figure 3 respectively).

Figure 5 presents the oscilloscope used for the measurements. It is a high performance device from ROHDE&SCHWARZ, an oscilloscope with a high-speed ASIC and a digital trigger that is so fast, it detects critical signal details that are missed by other oscilloscopes.

R&S®RTO1024 digital oscilloscope has 2 GHz bandwidth, 10Gsample/s sampling rate, a high-speed ASIC, deep waveform acquisition memory and a single-core A/D converter. The A/D converter with a high number of effective bits (ENOB > 7) ensures high vertical resolution. The low-noise front-end makes precise measurements possible even at the lowest vertical setting. Hardware-accelerated analysis displays measurement results instantly on the screen. The digital trigger system reduces trigger jitter to a minimum.

The user interface includes many functions, one of which is the samples averaging. For all the measurements

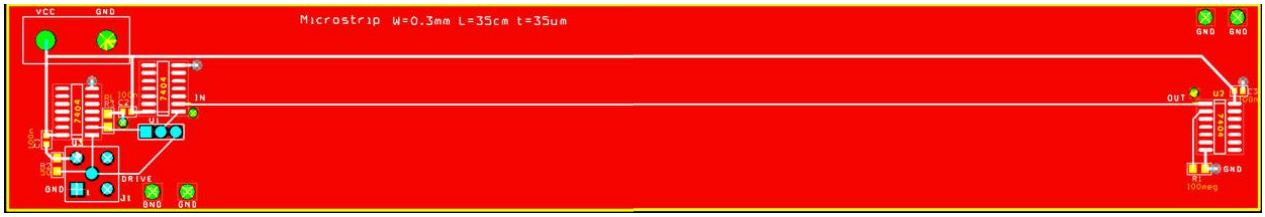

Figure 4. Layout design for board 1.

a 64-sample averaging was applied. Besides the mathematical functions available, the oscilloscope is capable of measuring the minimum and maximum levels of the signals, low and high levels, rising/falling times, positive/negative overshoot and many more. For all the waveforms that were recorded, these parameters were measured and can be seen in the results section.

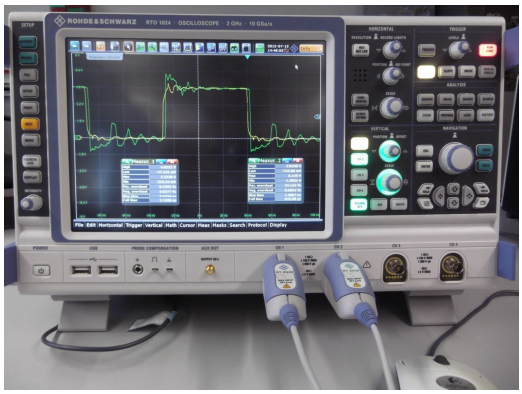

Figure 5. R&S®RTO1024 digital oscilloscope.

The perfect complement for this oscilloscope are the Rohde&Schwarz high-performance active probes. The active probes that were used (R&S®RT-ZS30 - active single-ended probe) are designed for measuring high-frequency signals (typically > 100MHz) and offer an optimum combination of bandwidth (3GHz) and input impedance and sensitivity (2.5mV). They have an input impedance of 1MΩ to minimize loading of the signal source's operating point. The large vertical dynamic range prevents signal distortion, even at high frequencies (e.g. 16V (Vpp) at 1GHz) [2]. The probes have a very short connection to reference ground, this increasing the quality of the measurements. As one could observe in the Figure 4, there are no stubs added in the layout. There is a via to ground in the close vicinity of each pin where the measurements had to be performed. In this way, the setup that was proposed for analysis is not influenced, and the signals transmitted on the line do not face additional reflections, due to stubs.

III. SIMULATION SETUP

Figures 6 and 7 present the setup used in the PSpice simulation. The 0.8pF capacitors simulate the influence of the probes over the measurements. The 2GHz low-pass filter and the 50Ω resistors represent the input of the oscilloscope. As mentioned before, the first measurement was done in order to determine the switching characteristics of the analyzed IC family in case the output is left in open circuit or connected to a load resistor. The signals that were recorded are the ones from the points indicated in the figure, namely GATE_IN (yellow trace in all figures) and GATE_OUT (green trace in all figures). Then, four sets of measurements and simulations were performed for each IC family to determine the effect of the different transmission lines over the integrity of the signals. The measurements were done on the output and input pin of the ICs connected to the transmission line – Line_IN and Line_OUT.

IV. RESULTS

The four PCBs with different microstrip interconnect structures were used to analyze the signal reflections in case the driver and receiver circuits belong to the logical families: TTL, Schottky TTL, High-speed CMOS, Advanced CMOS, Low-power Schottky TTL, Fast TTL family, Advanced high-speed CMOS.

This section presents some of the results obtained by experimental measurements and PSpice simulations.

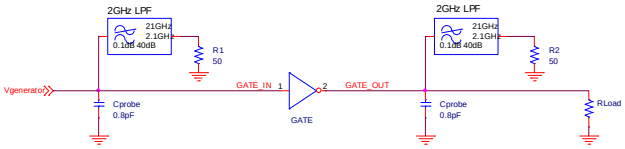

Figure 6. PSpice setup for switching characteristics.

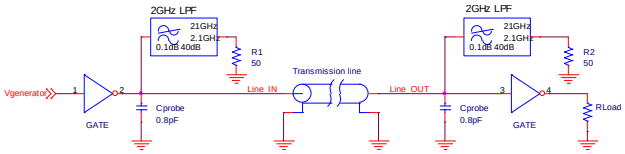

Figure 7. PSpice setup for signal reflections.

TTL family

For the TTL family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	4.75	5	5.25
VOH [V]	2.4	3.4	
VOL [V]		0.2	0.4
Rise time [ns]		12	22
Fall time [ns]		8	15

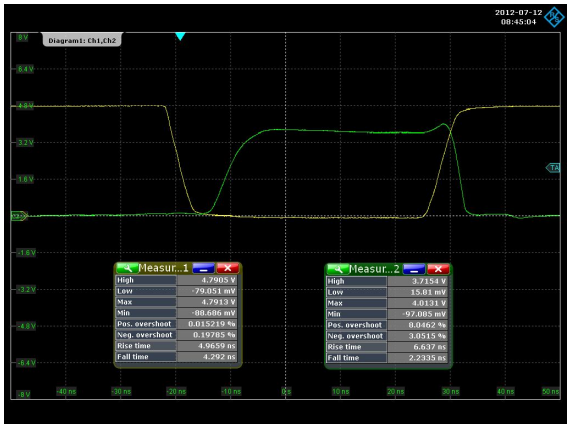

Figure 8. Experimental results.

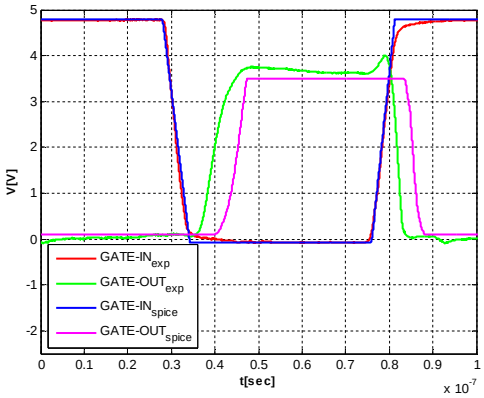

Figure 9. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	3.715	3.50026
VOL [V]	15.81m	89.99508m
Rise time [ns]	6.637	4.69351
Fall time [ns]	2.2335	2.75707

One can observe that in reality, the gate does not switch as slow as indicated in the datasheet, but also not as fast as it does in the simulation (see the rise time in the table above). Also the high and low voltage levels are different. These are two of the reasons the results obtained by PSpice simulation and experimental measurements are expected to be different.

Setup 1:

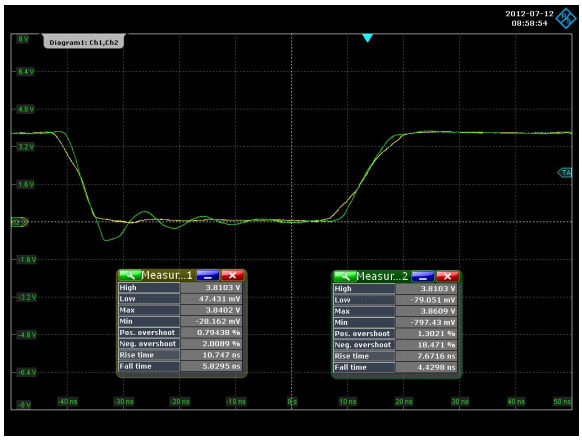

Figure 10. Experimental results obtained for board 1

	Experiment	Simulation
Rise time IN [ns]	10.747	8.88391
Rise time OUT [ns]	7.6716	5.61567
Fall time IN [ns]	5.8295	3.28193
Fall time OUT [ns]	4.4298	1.8148
Max level IN [V]	3.84	3.49387
Max level OUT [V]	3.86	3.49317
Min level IN [V]	-28.162m	38.35822m
Min level OUT [V]	-797.43m	-816.98394m

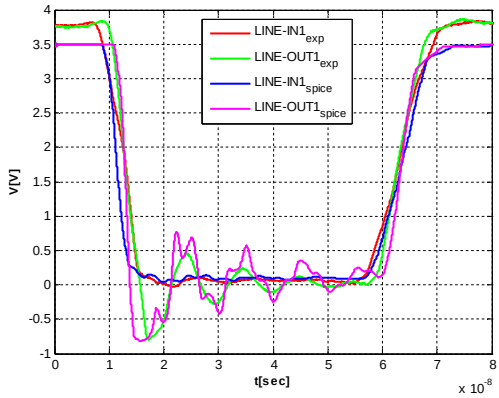

Figure 11. Experimental vs. simulation results.

Setup 2:

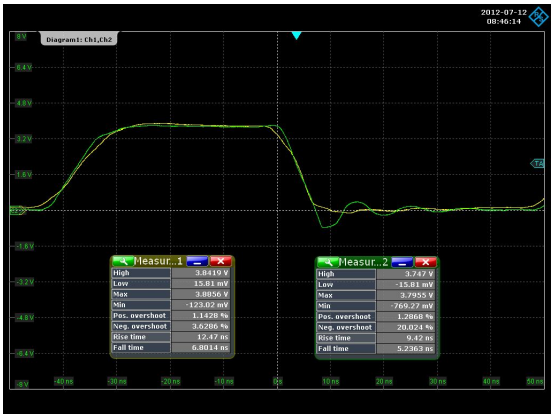

Figure 12. Experimental results obtained for board 2.

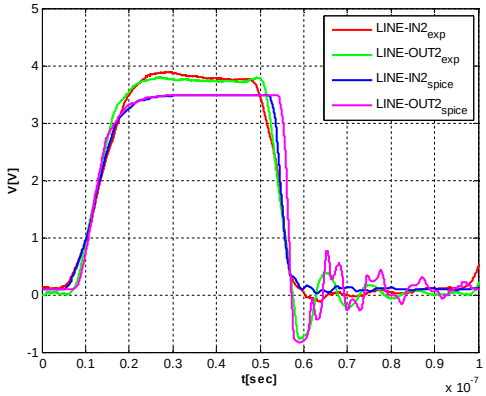

Figure 13. Experimental vs. simulation results

	Experiment	Simulation
Rise time IN [ns]	12.47	10.96626
Rise time OUT [ns]	9.42	8.94642
Fall time IN [ns]	6.8014	3.34659
Fall time OUT [ns]	5.2363	1.89043
Max level IN [V]	3.8856	3.49516
Max level OUT [V]	3.7955	3.49183
Min level IN [V]	-123.02m	17.02896m
Min level OUT [V]	-769.27m	-832.12548m

The first observation is that in the second case, when Z_0 is smaller, both the driver and the receiver switch slower. The falling/rising times measured for the experimental and simulation results increase, but have different values due to the fact the high and low level are not identical.

Schottky TTL family

For the Schottky TTL family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	4.75	5	5.25
VOH [V]	2.7	3.4	
VOL [V]		0.2	0.5
Rise time [ns]		3	4.5
Fall time [ns]		3	5

In the case of this family, a 330Ω load resistor was connected at the output of the gate. Without this resistor, the GATE_OUT signal was not in the range indicated by the manufacturer.

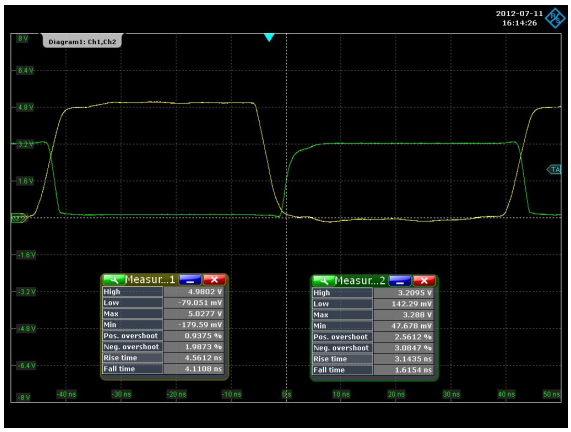

Figure 14. Experimental results.

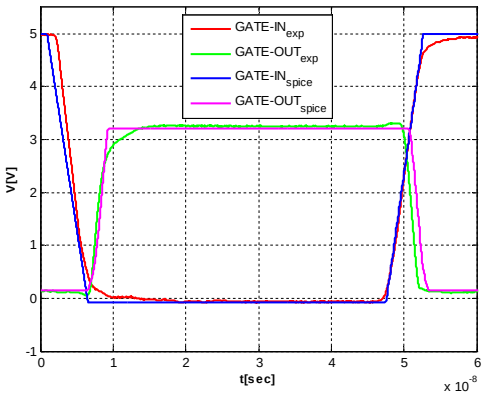

Figure 15. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	3.2095	3.20545
VOL [V]	142.29m	144.52766m
Rise time [ns]	3.1435	1.84627
Fall time [ns]	1.6154	1.76628

Again, the gate switches faster in the simulation than in reality. In the experimental measurement one can observe that the rise time has a typical value, only the fall time is smaller than expected. The voltage levels are in the expected range too.

The following figures present the results obtain with the second setup. It can be observed that the voltage levels and the rising time have similar values, but the falling time is much smaller in simulation. Also, the signal settles faster than in the real case.

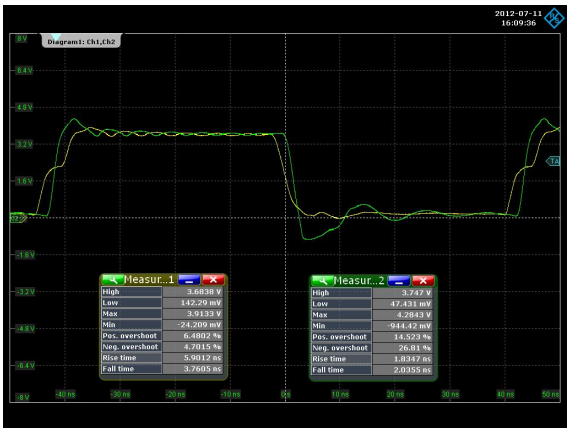

Figure 16. Experimental results obtained for board 2.

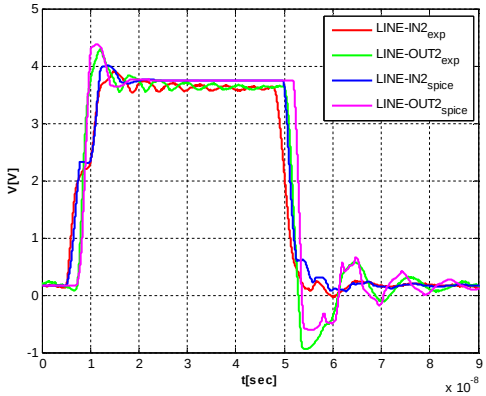

Figure 17. Experimental vs. simulation results.

	Experiment	Simulation
Rise time IN [ns]	5.9012	5.54312
Rise time OUT [ns]	1.8347	1.59841
Fall time IN [ns]	3.7605	0.933
Fall time OUT [ns]	2.0355	0.886
Max level IN [V]	3.9133	4.00621
Max level OUT [V]	4.2843	4.37134
Min level IN [V]	-24.209m	68.64465m
Min level OUT [V]	-944.42m	-604.58213m

High-speed CMOS family

For the HCMOS family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	2		6
VOH [V]	4.4	5	
VOL [V]		0.001	0.1
Rise time [ns]		8	19
Fall time [ns]		8	19

Figure 18. Experimental results.

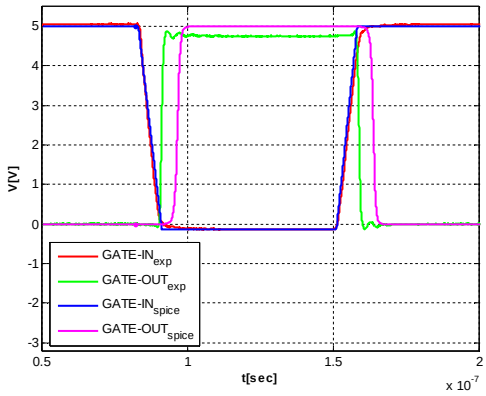

Figure 19. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	5.0435	4.99745
VOL [V]	-47.43m	2.22181m
Rise time [ns]	1.1063	2.21593
Fall time [ns]	1.1305	1.42392

One can observe that both in reality and simulation, the gate switches much faster than expected (1-2ns compared to 6-8ns). The voltage levels are in the expected range. For the setup 3, the following results were obtained. It can be observed that the signal settles faster than in the real case and the undershoot is smaller in the simulation. The overshoot has similar values.

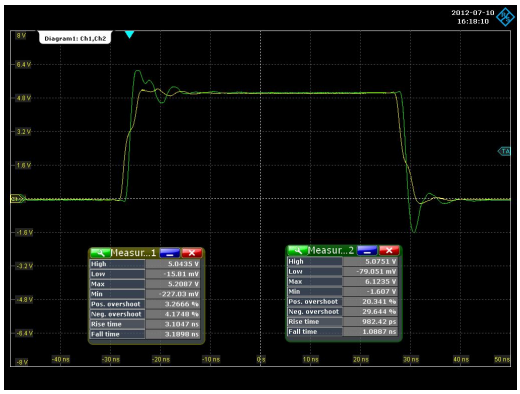

Figure 20. Experimental results obtained for board 3.

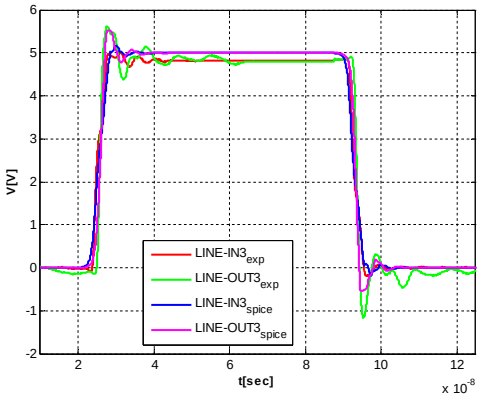

Figure 21. Experimental vs. simulation results.

	Experiment	Simulation
Rise time IN [ns]	3.1047	4.07752
Rise time OUT [ns]	0.98242	2.23873
Fall time IN [ns]	3.1898	3.84849
Fall time OUT [ns]	1.0887	1.95381
Max level IN [V]	5.2087	5.16935
Max level OUT [V]	5.59235	5.52048
Min level IN [V]	-227.03m	-182.86496m
Min level OUT [V]	-1.06	-536.86625m

Advanced CMOS family

For the ACMOS family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	2		6
VOH [V]	4.4	5	
VOL [V]		0.001	0.1
Rise time [ns]	1	4	7.5
Fall time [ns]	1	3.5	7

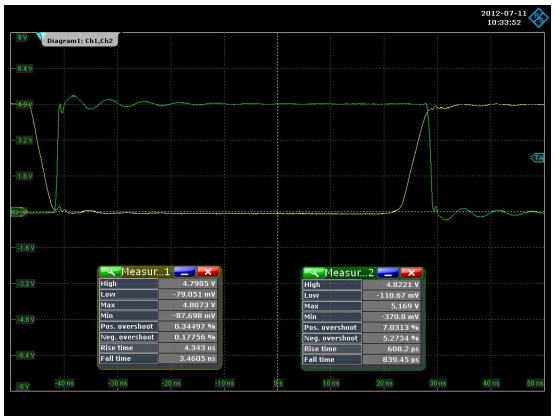

Figure 22. Experimental results.

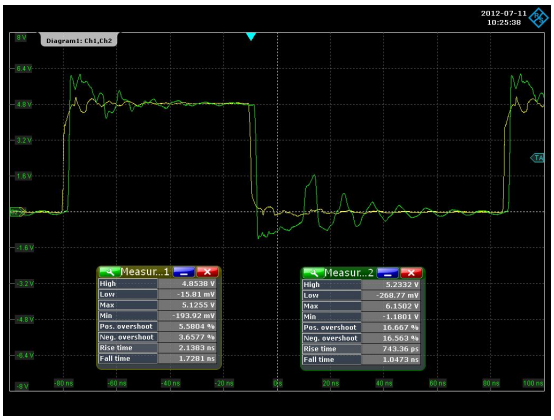

Figure 24. Experimental results obtained for board 1.

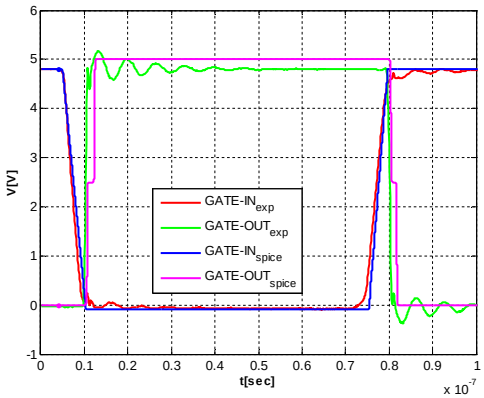

Figure 23. Experimental vs. simulation results.

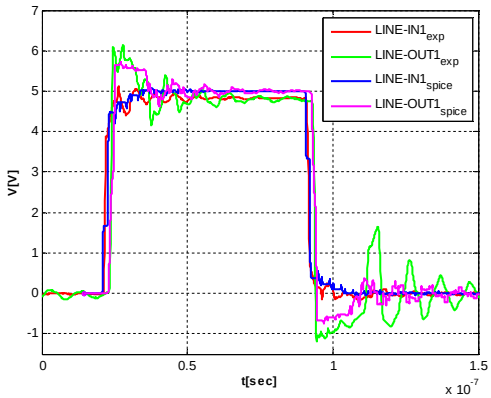

Figure 25. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	4.8221	4.99935
VOL [V]	-110.67m	466.56714u
Rise time [ns]	0.6082	1.80697n
Fall time [ns]	0.83945	1.40394n

One can observe that in reality, the gate switches faster than 1ns (minimum transition time given in the datasheet). The transition times obtained in the simulation are in the range indicated by the manufacturer. The voltage levels are also in the range, but it can be observed that even when there is no transmission line involved, the driver output oscillates. This effect is missed in the simulator. If the circuits are mounted on board 1, the oscillations measured at the receiver side of the t-line are much higher than the ones indicated by the simulator.

	Experiment	Simulation
Rise time IN [ns]	2.1383	4.51797n
Rise time OUT [ns]	0.74336	1.81952n
Fall time IN [ns]	1.7281	1.69079n
Fall time OUT [ns]	1.0473	1.42926n
Max level IN [V]	5.1255	5.07837
Max level OUT [V]	6.1502	5.71422
Min level IN [V]	-193.92m	-59.49155m
Min level OUT [V]	-1.1801	-731.63122m

Low-power Schottky TTL family

For the LS family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	4.75	5	5.25
VOH [V]	2.7	3.4	
VOL [V]		0.25	0.5
Rise time [ns]		9	15
Fall time [ns]		10	15

In the case of this family, a 2kΩ load resistor was connected at the output of the gate. Without this resistor, the GATE_OUT signal was not in the range indicated by the manufacturer.

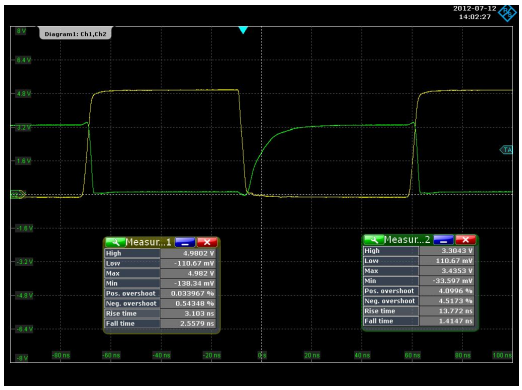

Figure 26. Experimental results.

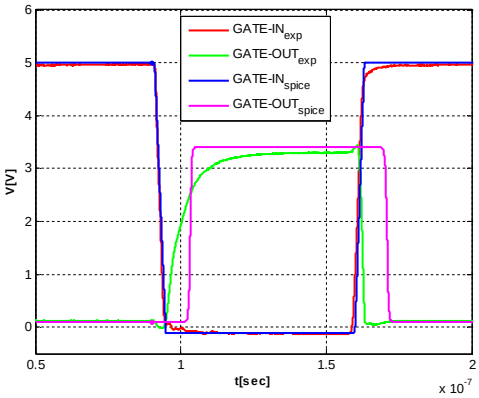

Figure 27. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	3.3043	3.41346
VOL [V]	110.67m	99.66522m
Rise time [ns]	13.772	1.14316
Fall time [ns]	1.4147	0.848908

One can observe that in the real case the switching from L-to-H is slow, as indicated in the datasheet, but the switching from H-to-L is much faster than expected (1.4ns compared to 10ns). The simulation results show that the model implemented in PSpice corresponds to a gate that switches very fast from L-to-H (848ps!!!). This is the main reason the results obtained by simulation and experiment do not match in the case of this IC family. The voltage levels are in the expected range.

For all setups, the results obtained in the simulation present high oscillations when switching from L-to-H. These high oscillations are due to the high dV/dt. In the case of the other transition, the results show good agreement.

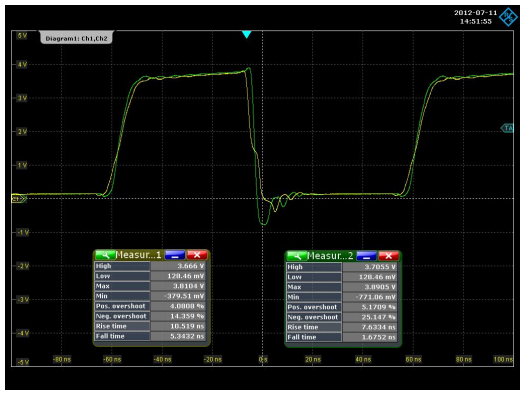

Figure 28. Experimental results obtained for board 1.

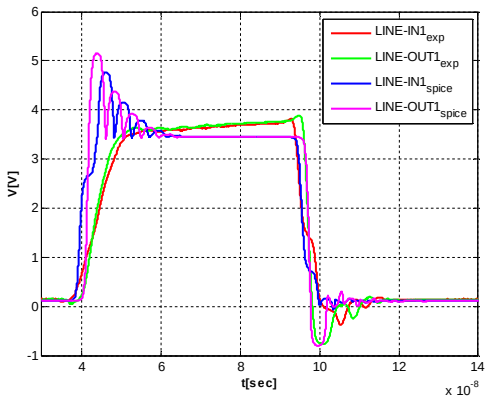

Figure 29. Experimental vs. simulation results.

	Experiment	Simulation
Rise time IN [ns]	10.519	4.60762n
Rise time OUT [ns]	7.6334	1.07788n
Fall time IN [ns]	5.3432	4.62725n
Fall time OUT [ns]	1.6752	1.14955n
Max level IN [V]	3.8104	4.77171
Max level OUT [V]	3.8905	5.16138
Min level IN [V]	-379.51m	-70.39873m
Min level OUT [V]	-771.06m	-802.05363m

Fast TTL family

For the Fast TTL family, the manufacturer indicates the following electrical and switching characteristics:

	Min	Typ	Max
VCC [V]	4.5	5	5.25
VOH [V]	2.5	3.4	
VOL [V]		0.3	0.5
Rise time [ns]	2.4	3.7	5
Fall time [ns]	1.5	3.2	4.3

In the case of this family, a 510Ω load resistor was connected at the output of the gate. Without this resistor, the GATE_OUT signal was not in the range indicated by the manufacturer.

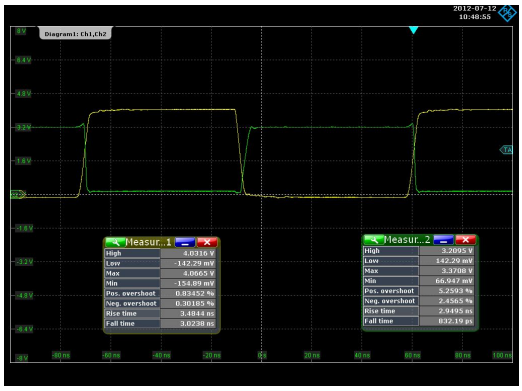

Figure 30. Experimental results.

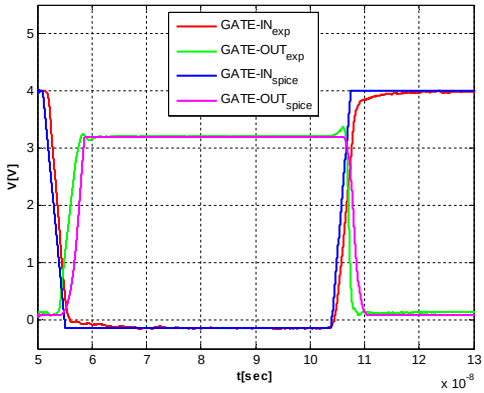

Figure 31. Experimental vs. simulation results.

	Experiment	Simulation
VOH [V]	3.2095	3.1897
VOL [V]	142.29m	88.65437m
Rise time [ns]	2.9495	2.52334n
Fall time [ns]	0.83219	2.23626n

One can observe that the rising and falling times are close to the range found in the datasheet, but the values measured are different than the ones from the simulation. The voltage levels are in the range in both cases.

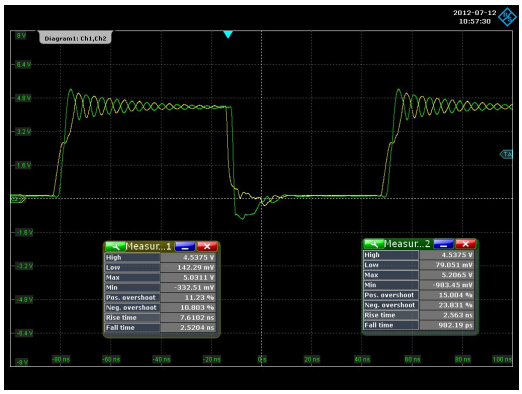

Figure 32. Experimental results obtained for board 1.

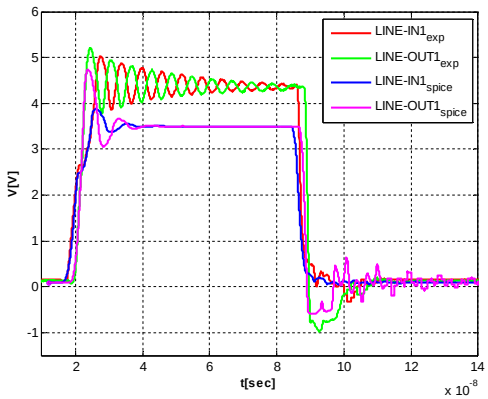

Figure 33. Experimental vs. simulation results.

The results of the experiments show that without impedance matching, the signals are distorted due to ringing. This effect did not appear in the simulation case.

	Experiment	Simulation
Rise time IN [ns]	7.6102	6.07906
Rise time OUT [ns]	2.563	2.29672
Fall time IN [ns]	2.5204	2.81401
Fall time OUT [ns]	0.98219	1.47375
Max level IN [V]	5.0311	3.87797
Max level OUT [V]	5.2065	4.72597
Min level IN [V]	-332.51m	44.54076m
Min level OUT [V]	-983.45m	-595.25645m

The measurements were redone for the case when a 1kΩ impedance matching resistor was used at the end of the t-line. The signal quality is significantly improved, as it can be observed in the following figures. In PSpice the results are the same with or without the 1kΩ resistor.

Figure 34. Experimental results obtained for board 1.

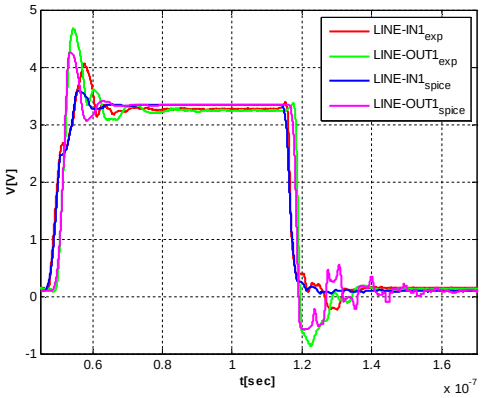

Figure 35. Experimental vs. simulation results.

	Experiment	Simulation
Rise time IN [ns]	5.8627	6.13225
Rise time OUT [ns]	2.2116	2.35480
Fall time IN [ns]	1.9791	2.73426
Fall time OUT [ns]	0.99477	1.51612
Max level IN [V]	3.2727	3.58809
Max level OUT [V]	3.336	4.26317
Min level IN [V]	-231.23m	50.90990m
Min level OUT [V]	-872.78m	-579.25457m

V. CONCLUSIONS

As the integration density of digital circuits and clock speed increases, more effective SI tools are needed. A good SI tool needs electrical models that describe the behavior of the integrated circuit.

Signal integrity is one of the most important factors to be considered when designing PCBs. SI problems are extremely difficult to diagnose and solve after the system is built or prototyped. Without pre-layout SI guidelines, prototypes may never leave the bench; without post-layout SI verifications, products may fail in the field [6].

The analysis presented in this paper underlines the importance of the electrical models used by the simulators. As it could have been observed, for almost all IC families that were analyzed, the PSpice implementation did not match with the characteristics of the real gate operation. Even in the case when the output of the gate was connected to a load, not to a t-line, differences appeared either at the steady-state voltage levels, either at the transition times, or both. Also, as most signal integrity tools based on SPICE types of circuit simulators, PSpice seems to treat power and ground as ideal supplies. The SPICE type simulators are mainly for linear and nonlinear lumped circuits, but the electromagnetic wave propagation and interactions are more complex, so they generally fail to accurately simulate voltage fluctuations on power and ground planes, and also fail to accurately simulate noise in signal lines caused by the interaction between the power and the signal distribution systems [5]. Also, the structure of the physical layout is not an input data for PSpice, as a good SI tool would require. For high accuracy modeling, full-wave electromagnetic field solvers, such as the 3D finite difference time-domain (FDTD) method or finite element method (FEM), should be applied. But 3D electromagnetic field solvers need very large computer resources (long computation time and huge computer memory space), so they are not suitable for prompt modeling in practical design and analysis [6].

Another aspect that must be kept in mind is that many SI problems are directly related to dV/dt or dI/dt, faster rise time significantly worsens some of the noise phenomena such as ringing, crosstalk, and power/ground switching noise [6]. In this analysis, the rise and fall times were in the nano-second range, but today it is not a surprise to see signals with even faster switching characteristics - rise and fall times are on the order of hundreds of picoseconds.

Despite all these drawbacks, the results obtained by simulation are in good agreement with the measured waveforms and indicate that PSpice could be used for a first SI analysis of circuits with reduced complexity. But to obtain reasonable results, the IC modeling should be checked to match the real case switching characteristics.

VI. ACKNOWLEDGMENT

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