

ELIN PROGRAMMABLE GAIN AMPLIFIERS

Mihaela CIRLUGEA , Lorant SZOLGA

Technical University of Cluj-Napoca, Bases of Electronics Department

Gh.Baritiiu Str. 26-28, 0264-401227, Mihaela.Cirlugea@bel.utcluj.ro , Lorant.Szolga@bel.utcluj.ro

Abstract: This paper presents the ELIN (externally linear internally nonlinear) method for designing a PGA (programmable gain amplifier) using MOS multiplying and weighting cells. This procedure is useful, for instance, in case of VLSI support vector machine classifiers that require many circuits for performing calculations, with high density but need good performances. This method is useful for SVM architectures because it requires simple nonlinear cells for an extended operation range. The procedure is good for weighting from 2^0 to 2^{-6} .

Keywords: current-mode, ELIN circuits, log-domain, PGA (Programmable Gain Amplifier), modular analog VLSI design, LIN-ELIN transformations.

I. INTRODUCTION

Analog VLSI design is focused on creating circuits with high complexity and high frequency in Low Voltage/Low Power parameters. Therefore, for occupying less area and having less parasitic effects, the function implementation has to be as efficient as possible. An elegant alternative offer current-mode Externally Linear Internally Nonlinear (ELIN) structures which have their starting point in the translinear cell, having a pretty wide dynamic range and operating in low voltage and high frequency conditions [1][3][6]. Usually, the VLSI design uses linearization of the basic blocks for obtaining a full linear circuit that adds limitations to the signals when working in the linear region. All this leads to small signals, reduced linearity, compensated nonlinearity, adding of supplementary components to the area and increasing the risk of parasitic effects [4].

The ELIN (Externally Linear Internally Nonlinear) contain, as their name says, internal nonlinear blocks which allow operating in large signal domains, are simple and don't need linearization procedures. When connecting these blocks, they behave in an extended dynamic range and without frequency loss. The design is pretty simple, allows a good linear bandwidth and a great parameter surveillance [6][2][4]. Some research was made and mixed techniques were used for the block linearization in electrical schemes by the instrumentality of the translinear principle applied in ELIN structures [5][7]. The results are very good, by keeping all the features of low voltage, high frequencies, implementation efficiency, high frequency and small parasitic effects, all these while maintaining a low circuit complexity.

This paper presents a design and linearization process for the circuit components, based on ELIN structures. The PGA (Programmable Gain Amplifier) cells contain each pairs of the reversible \mathbf{F} and \mathbf{F}^{-1} functions.

II. A GENERAL MODEL FOR F AND F-1 BLOCKS

Developing a circuit model with inner nonlinear blocks allows a better modularity for the scheme design and understanding, while making easier the replacement of circuit design structures. Considering two variables y_1 and y_2 that develop a linear relation *Lin*:

$$y_2 = \text{Lin}(y_1) \quad (1)$$

For our purpose, we consider y_i , $i = 1, 2$ in (1) being electric signals in a nonlinear continuous subjection, depending on some other variables x_i . Mathematically, one can write this relationship as $F(x_1)$ and $F(x_2)$ respectively. One can define the invertible nonlinear continuous function $\mathbf{F}: \mathbf{R} \rightarrow \mathbf{R}$ and its inverse $\mathbf{F}^{-1}: \mathbf{R} \rightarrow \mathbf{R}$, $\mathbf{F}^{-1}(y_i)$ so that we have:

$$\begin{cases} y = F(x) \\ x = F^{-1}(y) \end{cases} \quad (2)$$

In the proposed structure, we consider k a constant and a multiplication operator \otimes . If we write the function F as in (3 b), being linear, it can be considered as a gain or offset.

$$\begin{cases} F(kx) = F(k) \otimes F(x) & (a) \\ F(kF^{-1}(x)) = F(k) \otimes x & (b) \end{cases} \quad (3)$$

Again, from the mathematical point of view, we can clarify this relation exemplifying in (4) over functions like square root or power of 2 that respect (3):

$$(k\sqrt{x})^2 = k^2x \quad (4)$$

The presented functions are, as we said, invertible and not distributive in respect to multiplication. For our demonstration we need these functions to be applied on electrical signals like currents and voltages, so we can illustrate this F - F^{-1} method on our circuit. To keep the proper mathematical relationship we need variables x and y to be normalized signal values, so that x will correspond to normalized currents and y to normalized voltages, which will respect (2):

$$\begin{cases} y = \frac{i}{I} = F\left(\frac{v}{V}\right) & (a) \\ x = \frac{v}{V} = F^{-1}\left(\frac{i}{I}\right) & (b) \end{cases} \quad (5)$$

The variables i and v , denoted with lowercase letters, correspond to input/output single signals or signal differentials, while the reference terms are written in capital letters. As general block modules we can depict them, schematically as in Figure 1, where the model presented is for the current-mode situation, while we work in the translinear method using currents, not voltages.

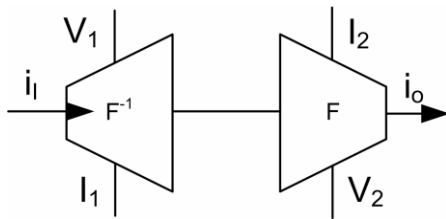


Figure 1. General F and F^{-1} modules, in current-mode

$$i_o = I_2 F\left(\frac{v}{V_2}\right) = I_2 F\left(\frac{1}{V_2} V_1 \cdot F^{-1}\left(\frac{i_i}{I_1}\right)\right) \quad (6)$$

Considering $V_1=V_2=V$, which has an electrical fundament in that the voltage references have to be equal for us to obtain a linear current input-output characteristic, from the expression (6) above, we obtain

$$i_o = \frac{I_2}{I_1} i_i \quad (7)$$

equation which will also lead to the use of the current-mode multiplier that will be presented in the following paragraphs. We must note that $F(kx)$ and $nF(x)$ are two different things! The amplifiers we want to obtain must keep their linear characteristics also for large signals not only in the small signal area. If the functions F - F^{-1} respect condition (3 a), the in-out characteristics will be linear, always for large signals.

III. ELIN IMPLEMENTATION OF PGA CIRCUITS

For implementing a circuit using the method presented above, one has to connect the two basic blocks in Figure 1, the first at the input, and the second at the output of the cir-

cuit. The calculus will be done without modifying the circuit's internal structure and its nonlinear characteristic. The space of F - F^{-1} can perform various operations such as square root, logarithmic, exponential and others, depending on the problem one has to solve.

If one works with the pair of mathematical functions such as logarithmic-exponent to implement the F - F^{-1} pair, the general block for in-out functions would be as presented in Figure 2:

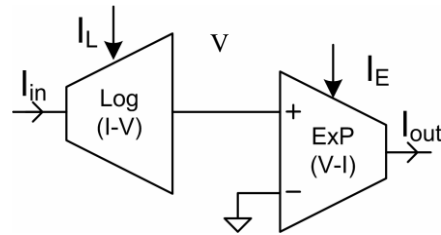


Figure 2. Log-domain variable gain amplifier

The log-domain variable gain amplifier, displayed in Figure 2, can be used for implementing our programmable gain amplifier. Analyzing the second figure, one can notice that the first block converts the current to voltage, to make the liaison to the circuit to be processed, while the second block, which will appear at the circuit's output, acts as a voltage-to-current converter. Thus, the two modules are complementary and can be used with the pair of functions F - F^{-1} Logarithmic (Log) – Exponential (Exp). To be noticed the bias currents, I_L respectively I_E , thus, the gain of the amplifier can be, of course, expressed as

$$A_I = \frac{I_E}{I_L} \quad (8)$$

This method was tested in [4]. The gain was tuned by modifying the bias current of the Logarithmic and Exponential cell using a current division network (CDN). The output current of the network was controlled by an 8 bit digital word, making capable of a gain between $1/2^4$ and 2^4 . The final PGA structure using log-domain cells is depicted in Figure 3.

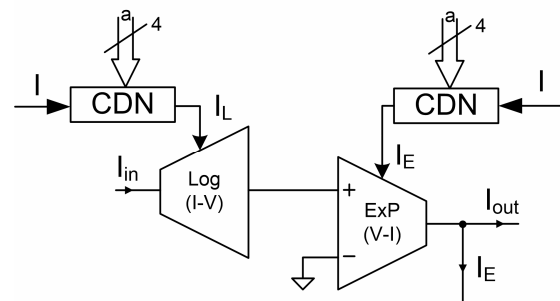


Figure 3. a) PGA internal structure b) PGA symbol

The PGA was capable of a gain tuning between -24dB and 27dB without major deviation from the desired gain as Figure 4 shows.

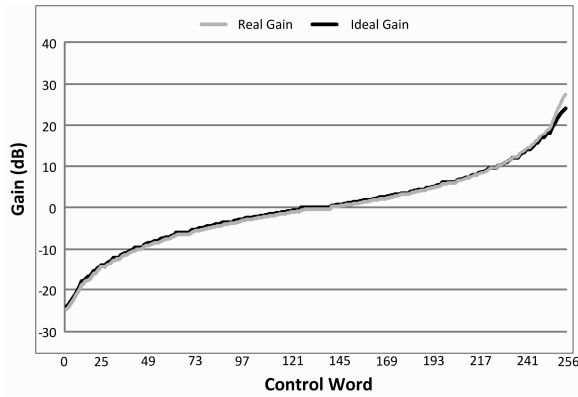


Figure 4. Measured gain vs. expected gain for the log-domain PGA

Another approach for implementing programmable gain amplifiers is to use the root - square root mathematical function pair. In Figure 5 is presented a translinear MOS amplifier for illustrating this method [8].

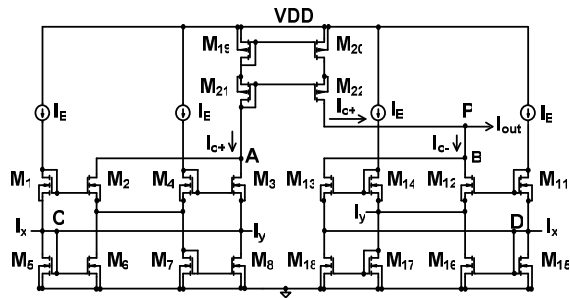


Figure 5. Four quadrants MOS multiplying circuit

The circuit implements relation (7), actualised with the following variables:

$$i_o = \frac{I_x i_y}{2I_B} \quad (10)$$

Applying the translinear principles over loops $M_1M_2M_3M_4$ and $M_{11}M_{12}M_{13}M_{14}$ and using the current relations of the current mirrors over the nodes A,B,C and D, system (11) results:

$$\begin{cases} \sqrt{I_1} + \sqrt{I_4} = \sqrt{I_2} + \sqrt{I_3} \\ \sqrt{I_{11}} + \sqrt{I_{14}} = \sqrt{I_{12}} + \sqrt{I_{13}} \\ I_o^+ = I_3 + I_2 \\ I_o^- = I_{13} + I_{12} \\ I_y + I_x = I_2 - I_3 \\ I_y - I_x = I_{12} - I_{13} \end{cases} \quad (11)$$

After solving the system, one obtains (12):

$$\begin{cases} I_o^+ = 2I_B + \frac{(I_x + I_y)^2}{8I_B} \\ I_o^- = 2I_B + \frac{(I_x - I_y)^2}{8I_B} \end{cases} \quad (12)$$

where applying Kirchoff's law and equation in circuit node P, we obtain the relation that defines the output current

$$\begin{cases} I_{out} = I_o^+ - I_o^- = \frac{I_x I_y}{2I_B} \\ (I_x + I_y), (I_x - I_y) \in (-4I_B, 4I_B) \end{cases} \quad (13)$$

Equation (10) needs condition (14) to be fulfilled

$$I_x \pm i_y \in (-4I_B, 4I_B) \quad (14)$$

For $I_B = 20\mu A$ we obtained the following set of functioning domains:

Table 1.

I_x values	Domain for I_y
$-40 \mu A$	$-40 \mu A$ to $40 \mu A$
$-20 \mu A$	$-60 \mu A$ to $60 \mu A$
$20 \mu A$	$-60 \mu A$ to $60 \mu A$
$40 \mu A$	$-40 \mu A$ to $40 \mu A$

Figure 6 shows the output current for the input setups presented in Table 1.

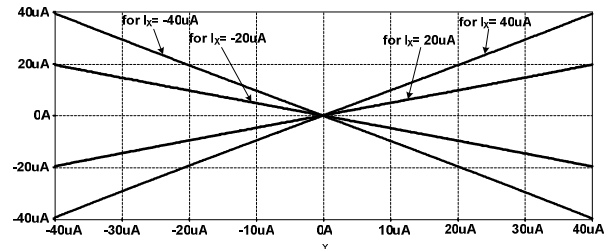


Figure 6. Simulation results for circuit in Figure 5, DC analysis

The simulations results prove the good functionality of the circuit. Considering:

$$i_y = i_{in} \text{ and } I_x / 2I_B = w \quad (15)$$

where w is a weighting factor, results that :

$$i_{out} = w * i_{in} \quad (16)$$

and the gain is :

$$G = \left| \frac{i_{out}}{i_{in}} \right| = |w| \text{ or } G_{dB} = 20 \lg |w| \quad (17)$$

Based on (14) and (15) and considering the current I_x much smaller than the input current, we obtain $|I_x| \cong 4I_B$ and thus:

$$G_{dB \max} \cong 20 \lg \left(\frac{4I_B}{2I_B} \right) = 20 \lg 2 = 12 \text{ dB} \quad (18)$$

If we want to obtain a weighting with the powers of 2 with

$$w = \left\{ 1/2^0, 1/2^1, \dots, 1/2^{10} \right\} \quad (19)$$

according to (17) we obtain

$$G_{dB \min} = 20 \lg (1/2^{10}) = -120 \text{ dB} \quad (20)$$

IV. EXPERIMENTAL RESULTS

The circuit was tested for $I_B = 10 \mu\text{A}$, $i_y = [-20 \mu\text{A}, 20 \mu\text{A}]$ and values of I_x that assure the w weighting in powers of 2 from relation (19). This can be accomplished by the same CDN used for the log-domain PGA.

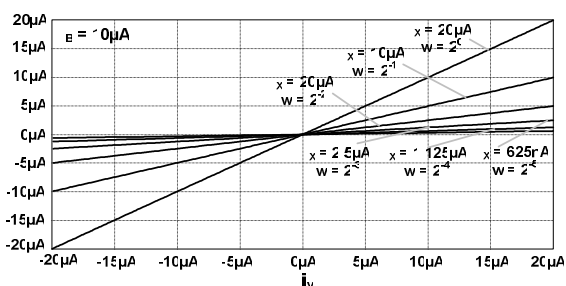


Figure 7. DC analysis results for circuit in Figure 5 to prove the weighting characteristic of it

After simulating the circuits for all the values mentioned above, it showed that it has a good accuracy for weights between 2^0 to 2^5 , while for weights in the range of 2^6 to 2^{10} the output current is linear but the offset introduced by the circuit makes it not to respect the weighting purpose, for an input current between $-1 \mu\text{A}$ and $1 \mu\text{A}$, case where the gain G_{\min} becomes -60 dB .

The relative error between the ideal current and the simulated one, calculated with (21) is between 0.27% and 1.62% , thus we can say that we have a good precision.

$$\text{Err}_{\text{-rel}} = \left| \frac{I_{\text{out_ideal}} - I_{\text{simulated}}}{I_{\text{out_ideal}}} \right| * 100 [\%] \quad (21)$$

If we increase the biasing current $I_B = 20 \mu\text{A}$ we can also in-

crease I_x and i_y so that for an i_y between $-40 \mu\text{A}$ and $40 \mu\text{A}$, we can have for $I_x = \{40, 20, 10, 5, 2.5, 1.25, 0.625\} \mu\text{A}$, meaning that we can increase w up to 2^6 with $G_{\min} = -72 \text{ dB}$.

V. CONCLUSIONS

In this paper we presented a novel approach for implementing low-power VLSI programmable gain amplifiers. The circuit was obtained using ELIN structures, more exactly a MOS multiplying circuit. The operation of the circuit is based on the root – square root mathematical function pair. The gain tuning was possible by changing the DC bias currents through a CDN. The CDN was designed to tune the gain in powers of 2, from 2^0 to 2^{10} . To validate the analytical presentation, the proposed programmable gain amplifier and the current division network were implemented using a generic BiCMOS $0.18 \mu\text{m}$ process. The simulation results show that for a gain between 2^0 and 2^6 the obtained results are according to the desired response. For this interval the deviation from the ideal response of the circuit is less than 2% which makes the circuit suitable for applications like SVM classifiers.

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