SECOND ORDER POLYNOMIAL FUNCTION IMPLEMENTATION USING ELIN ANALOG BUILDING BLOCKS

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Abstract: This paper presents an ELIN implementation of a second order polynomial function. The basic building blocks of the proposed circuit consist of a multiplier, an adder and two weighting cells. These blocks were implemented using current-mode log-domain cells. The circuit was implemented using bipolar transistors and the design was validated by PSPICE simulations.

Keywords: *current-mode, ELIN, arithmetic circuits.*

I. INTRODUCTION

Analogic signal processing represents an important area of analysis and design of the integrated circuits, used in domains like communication systems, medical equipment's, hearing devices and disc units. This is, because the features of these circuits, low power and high speed, allow the processing of analog signals. The importance of analog circuits consists in their advantageous use in amplitude modulation, waveform generation, frequency translations, oscillators with variable frequency, adaptive filters, neural networks, automatic gain control, etc. The generally improving of the efficiency of such circuits is necessary in the design of analog and mixed signals, or in generating arithmetical operations for signals. All these need low current and voltage operations so that the necessary power consumption has to be reduced as well. [1]

In [2] the authors propose a multiplying/dividing circuit working in current mode. This circuit can be used for a type2 fuzzy controller, namely for implementing the reductor stage transforming the type2 fuzzy set into a type1 fuzzy set. This circuit needs six stages of multiplication/division. The circuit proposed in this paper is obtained by interconnecting a geometric mean circuit with one of square operation and division. Because the two operations are complementary, the two circuits can be obtained having as starting point the same basic circuit while interchanging the inputs and outputs. The main block, containing cascaded current mirror blocks, has been built with MOS transistors that work in saturation and in the linear region. For this implementation, a 0.35µm technology CMOS has been used.

In [3] the authors present the scheme of a multiplying/division circuit in current mode, using two current follower transconductor amplifiers (CFTA). The CFTA device is a combination between a current follower and a transconductor amplifier, which have a transfer gain that can be controlled by the external biasing currents. The proposed circuit can perform the multiplication and division procedure in a four-quadrant circuit, by selecting the current signals applied on the two CFTA blocks. The main scheme is based on a current follower, a biasing circuit and a transconductor amplifier with multiple outputs. For the implementation, a bipolar transistor technology was used. This circuit can be used for peak detectors, modulators, phase detectors and frequency synthesizer and, more recently, in artificial neuronal networks and fuzzy controllers.

In [4] a voltage mode multiplier/divider is presented, realized with logarithmic and antilog amplifiers. The main block of such a voltage mode multiplier/divider is composed by two logarithmic amplifiers, an exponential amplifier and a summing/differential one. The exponential amplifier can produce the inverse function of a logarithmic amplifier; therefore, these two circuits are habitually used together for analogic calculus. For a better practical implementation, the authors propose the multiplier/divider circuit being implemented with compensating logarithmic and exponential amplifiers for avoiding issues that may appear like oscillation, temperature variations, base-emitter junction voltage variations and accepting of the bipolar input currents and voltages.

In [5], the authors present in a quadrature current mode circuit, a multiplier/divider log-antilog based on a differential difference current conveyor (DDCC) and four diodes. The log-antilog multipliers use the exponential properties of the biasing p-n junctions, having a diode or a bipolar transistor for assuring the necessary log-antilog function. The DDCC proposed has great advantages over CCII and the differential difference amplifier (DDA), namely a higher input impedance and an easier way of performing the arithmetical operations. The main block DDCC has been realized using MOS transistors, working in the linear and saturation region.

This paper is organized into four sections. Section II shows the proposed circuit, section III presents the log-domain basic building blocks and the log-domain implementation of the basic cells. In section IV the simulation results are presented followed by the conclusions.

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II. PROPOSED CIRCUIT

The schematic block of the proposed circuit is presented in Figure 1. It is designed to implement a second order polynomial function like the one described in (1).

$$ax^2 + bx + c \tag{1}$$

The circuit consists of a multiplier cell, two weighting cells and an adder. These circuits are current-mode circuits, where inputs and output are all electric currents. The multiplying cell and one of the weighting cells implements the first term of the function (ax2), the other weighting cell implements the second term (bx). The adder circuit has three inputs and realize the addition of the first two mentioned terms and generates the third term (c).

III. LOG-DOMAIN CIRCUITS

A. Basic log-domain building blocks

The basic building blocks (logarithmical cell and two exponential cells) used for our application are based on voltage controlled current mirrors [6][7]. The logarithmic cell and its symbol is presented in Figure 2; Figure 3 shows the exponential current sink cell and its symbol while Figure 4 shows the exponential current source cell and its symbol. The expression of the output voltage for the logarithmic cell is described in (2) and the output current for the two exponential cells is presented in (3)

$$V_{out} = 2V_T \ln\left(\frac{I_L + i_{in}}{I_L}\right) \tag{2}$$

$$I_{out} = I_E \exp\left(\frac{V_{in+} - V_{in-}}{2V_T}\right) \tag{3}$$

where VT is the thermal voltage, IL and IE are bias currents.

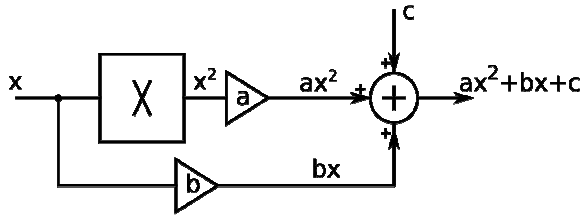

Figure 1. Block diagram of the proposed circuit

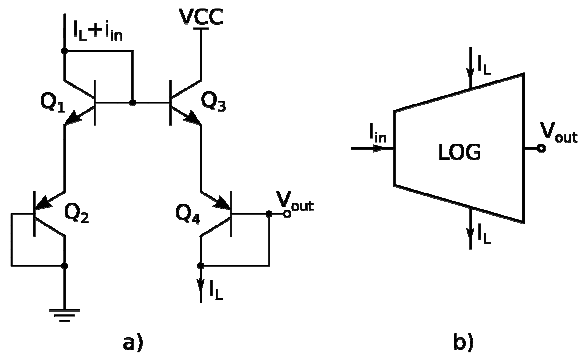

Figure 2. Logarithmic cell: a) electrical circuit, b) symbol

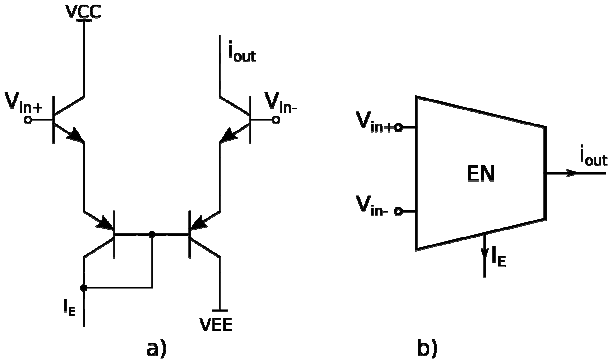

Figure 3. Exponential current sink cell: a) electrical circuit, b) symbol

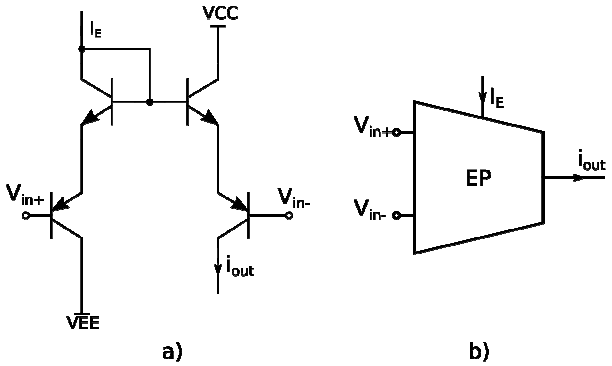

Figure 4. Exponential current source cell: a) electrical circuit, b) symbol

B. Log-domain weighting circuit

The log weighting circuit is the one in Figure 5. It contains a log cell and an exponential cell, cascaded. The output current is the one in (4).

$$I_{out} = I_{in}\frac{I_E}{I_L} + I_L + I_E \tag{4}$$

where I_L and I_E are the biasing currents for the LOG and EXP cells. Inspecting this equation, one can see that the weighting coefficient can be modified by the ratio of the two bias currents. Also, at output, in addition to the weighted input signal, also the bias currents appear. These can be eliminated with current mirrors, so that the output current becomes relation (5).

$$I_{out} = I_{in}\frac{I_E}{I_L} \tag{5}$$

C. Log-domain three input summing-weighting circuit

The adding-weighting circuit with 3 inputs in log-domain is presented in Figure 6. It contains 3 weighting circuits parallel connected. The output current is (6):

$$I_{out} = \sum_{i=1}^{3} i_{ini}\frac{I_{Ei}}{I_{Li}} + \sum_{i=1}^{3} I_{Li} - \sum_{i=1}^{3} I_{Ei} \tag{6}$$

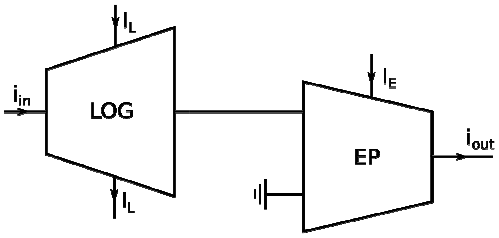

Figure 5. Log-domain weighting circuit

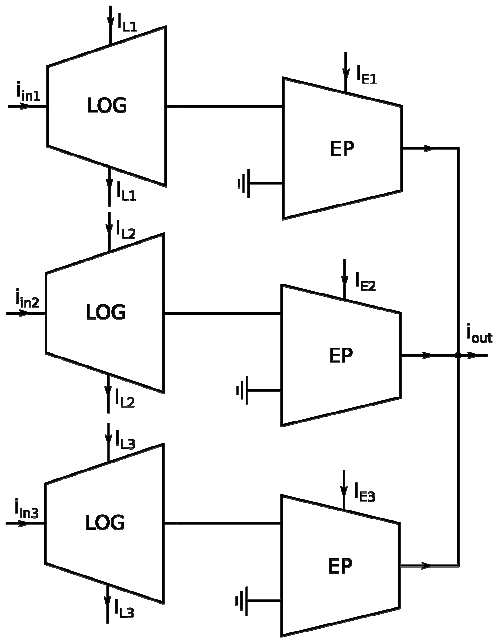

Figure 6 Log-domain 3-input adding-weighting circuit

where I_{L1}, I_{L2}, I_{L3}, I_{E1}, I_{E2}, I_{E3} are the biasing currents for the cells LOG and EP. If we choose them equal, the output current becomes (7):

$$I_{out} = i_{in1} + i_{in2} + i_{in3} \tag{7}$$

D. Log-domain multiplying circuit

The log-domain multiplying circuit is identical to the weighting cell in Figure 5, but, to the EP-cell bias-current a second current is added. The circuit is shown in Figure 7, having the output current expressed as (8):

$$I_{out} = \frac{i_{in1} \cdot i_{in2}}{I_L} + \frac{i_{in1} \cdot I_E}{I_L} + I_E + i_{in2} \tag{8}$$

where IL and IE are dc bias currents.

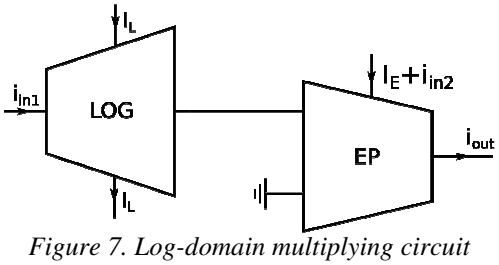

Figure 7. Log-domain multiplying circuit

If we consider the dc bias currents of the logarithmic and exponential cells equal, the output current can be rewritten as follows:

$$I_{out} = \frac{i_{in1} \cdot i_{in2}}{I_L} + i_{in1} + I_E + i_{in2} \tag{9}$$

From (9) one can see that at the output, besides the product of the input currents iin1 and iin2 there are also the dc bias current of the exponential cell and the two input currents. These terms can be removed using current mirrors.

IV. EXPERIMENTAL RESULTS

For testing the functioning of the circuit in Figure 1, the circuits in Figures 5, 6 and 7 have been implemented in a bipolar transistor technology.

First the weighting circuit in Figure 5 was tested, with a sinus input signal having an amplitude of 1uA and frequency of 10kHz. The bias current I_L was chosen 10uA and the current I_E of 20uA, resulting a weighting coefficient of 2. The input and output signals are presented in Figure 8. The dc output component is 19uA. This can be cancelled using a current mirror that extracts at the output the bias current of the EP-cell. The amplitude of the output signal is 1.85uA. The deviation from the wanted current 2uA is of 7.5% and is caused by parameters β and VAF of the bipolar transistors.

The summing circuit in Figure 6 has also been tested. At its input, 3 identic sinusoidal signals were applied, having the amplitude of 1uA and frequency of 10kHz. The bias currents of the LOG and EP cells were chosen to be equal, and having the value of 10uA. The signals obtained are presented in Figure 9. The dc component is 28.1uA and can be canceled with current mirrors that subtract the bias currents of the EP-cells. The output signal amplitude is 2.8uA. The deviation from 3uA is produced by the parameters β and V_{AF} of the bipolar transistors that were used for building the EP and log cells.

For testing the multiplying circuit in Figure 7, at the two inputs signals were applied, having an amplitude of 1uA and a frequency of 1kHz respective 100kHz. The biasing currents in dc were chosen to be 10uA. The input and output signals are those in Figure 10. One can notice that the value of the dc output current was not completely canceled, being equal to -1uA.

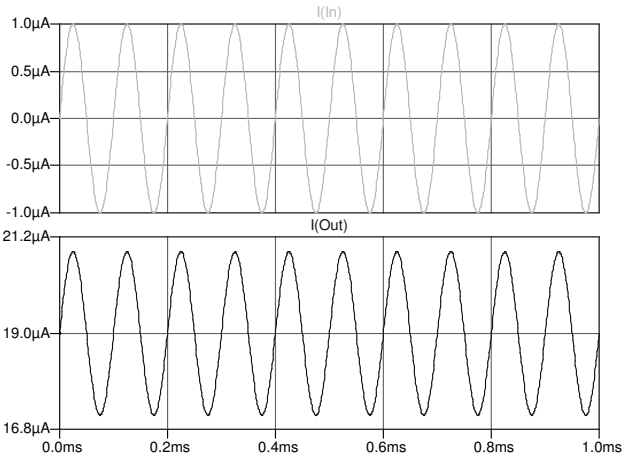

Figure 8. Simulation results for the weighting circuit

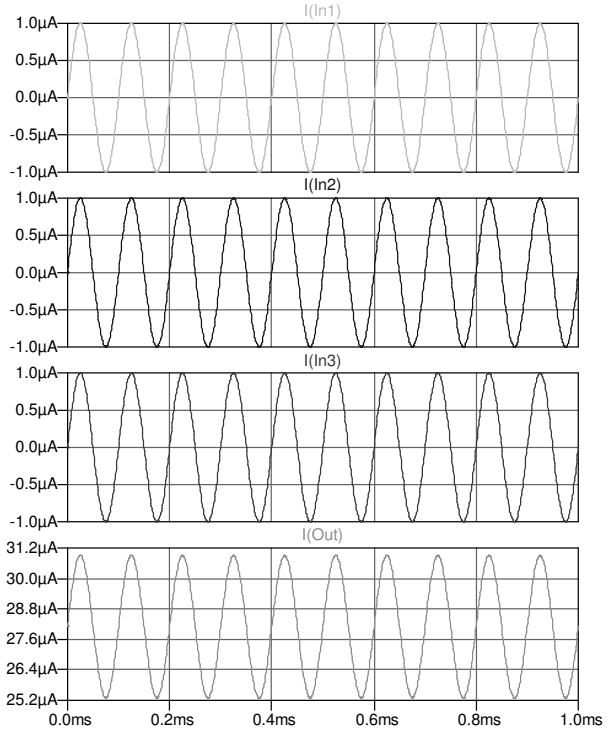

Figure 9. Simulation results for the adder circuit

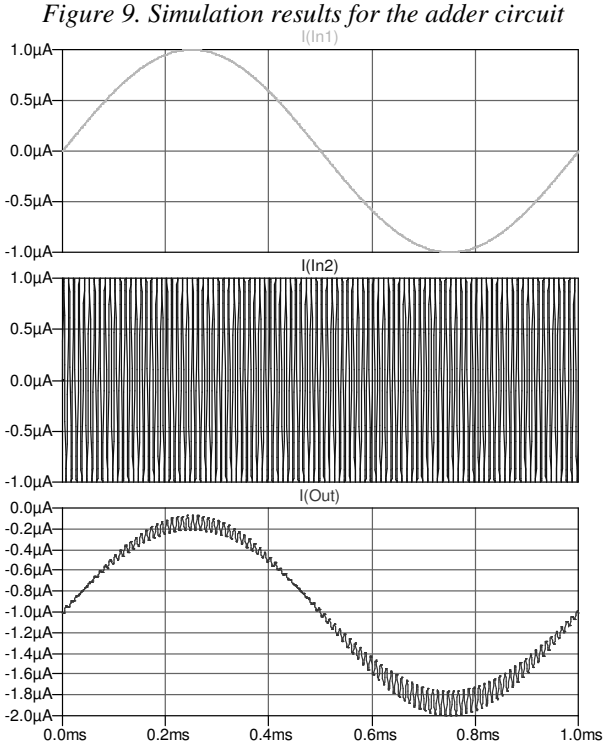

Figure 10. Simulation results for the multiplying circuit

Finally, the circuit was tested that implements the second order polynome in Figure 1. The coefficients a, b and c were set all to 2. The PSpice simulation result is shown in Figure 11 where on Ox axis we have the variable x. Both wanted and obtained signals are represented. One can notice that the obtained signal has the variation we wanted, but has also an offset of -700nA.

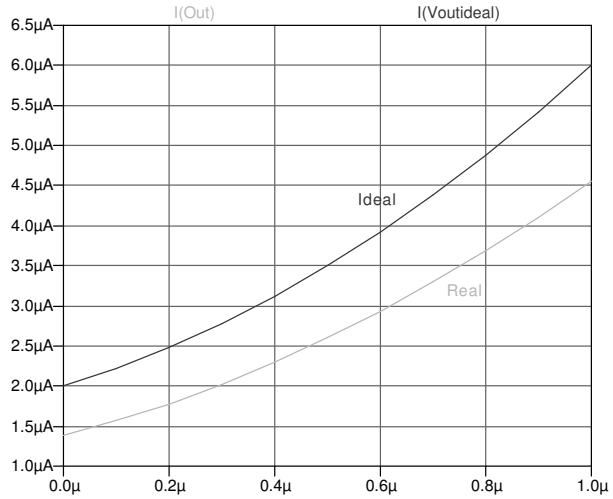

Figure 11. Simulation results for the proposed circuit

V. CONCLUSIONS

In this paper, a current-mode circuit is presented, that implements a second order polynome. The circuit was build using ELIN circuits in the logarithmic domain. The implementation was done by using a multiplying circuit, two weighting circuits and one adding-weighting circuits.

The major advantage of these circuits, in comparison to the others in literature, is their internal structure which is simpler.

For testing the functionality of the circuits, a bipolar transistor level was used, analysis being performed in PSpice. The obtained results confirm the correct functioning of the component circuit blocks but also of the final resulting circuit, though one can observe the influence of the bipolar transistor parameters β and the Early Voltage V_{AF} over the output currents.

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