

## BIBLIOGRAFIE

- [1] Al-Twaijry, H., Flynn, M., "Optimum Placement and Routing of Multiplier Partial Product Trees", Technical Report No. CSL-TR-96-706, Departments of Electrical Engineering and Computer Science, Stanford University, Stanford, 1996.
- [2] Alexander, M. J., Robins, G., "An Architecture-Independent Unified Approach to FPGA Routing", Technical Report No. CS-93-51, Department of Computer Science, University of Virginia, Charlottesville, 1993.
- [3] Alexander, M. J., Robins, G., "New Graph Arborescence and Steiner Constructions for High-Performance FPGA Routing", Technical Report No. CS-94-12, Department of Computer Science, University of Virginia, Charlottesville, 1994.
- [4] Alexander, M. J., Robins, G., "New Performance-Driven FPGA Routing Algorithms", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 12, December 1996, pp. 1505-1517.
- [5] Alpert, C. J., Hu, T. C., Huang, J. H., Kahng, A. B., Karger, D., "Prim-Dijkstra Tradeoffs for Improved Performance-Driven Routing Tree Design", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 7, July 1995, pp. 890-896.
- [6] Altera Corp., *The Maximalist Handbook*, 1990.
- [7] Atmel Corp., *Configurable Logic. PLD, FPGA, Gate Array Data Book*, San Jose, 1995.
- [8] Baruch, Z., "Datapath Allocation", *ACAM Scientific Journal*, Vol. 4, No. 2, 1995, pp. 67-75.
- [9] Baruch, Z., "Metode de descriere a sistemelor numerice". Referat de doctorat, Catedra de Calculatoare, Universitatea Tehnică din Cluj-Napoca, 1995.
- [10] Baruch, Z., "Scheduling Algorithms for High-Level Synthesis", *ACAM Scientific Journal*, Vol. 5, No. 1-2, 1996, pp. 48-57.
- [11] Baruch, Z., "Sistem CAD pentru sinteza sistemelor numerice". Referat de doctorat, Catedra de Calculatoare, Universitatea Tehnică din Cluj-Napoca, 1996.
- [12] Baruch, Z., "Translatarea limbajelor de descriere a unităților hardware". Referat de doctorat, Catedra de Calculatoare, Universitatea Tehnică din Cluj-Napoca, 1996.
- [13] Baruch, Z., Creș, O., Pusztai, K., "CAD System for the Atmel FPGA Circuits". Third International Conference on Technical Informatics CONTI98, Timișoara, 1998, In *Transactions on Automatic Control and Computer Science*, Vol. 43 (57), No. 4, pp. 228-237.
- [14] Baruch, Z., Creș, O., Pusztai, K., "Partitioning for FPGA Circuits". In *Proceedings of MicroCAD '97 International Computer Science Meeting*, Miskolc, Hungary, 1997, Section D, pp. 113-116.
- [15] Baruch, Z., Creș, O., Pusztai, K., "Routing for FPGA Circuits". In *Proceedings of A&Q '98 International Conference on Automation and Quality Control*, Cluj-Napoca, 1998, pp. Q214-Q219.
- [16] Baruch, Z., Creș, O., Pusztai, K., "Technology Mapping for the Atmel FPGA Circuits". Third International Conference on Technical Informatics CONTI98,

- Timișoara, 1998, In *Transactions on Automatic Control and Computer Science*, Vol. 43 (57), No. 4, pp. 218-227.
- [17] Baruch, Z., Pusztai, K., "AHPL Compiler". In *Proceedings of MicroCAD '93 International Computer Science Meeting*, Miskolc, Hungary, 1993, Section E, pp. 121-129.
- [18] Beetem, J., "Simultaneous Placement and Routing of the LABYRINTH Reconfigurable Logic Array", *The International Workshop of Field-Programmable Logic and Applications*, Oxford, U.K., 1991, pp. 232-243.
- [19] Boese, K. D., Kahng, A. B., McCoy, B. A., Robins, G., "Fidelity and Near-Optimality of Elmore-Based Routing Constructions", Technical Report No. CS-93-14, Department of Computer Science, University of California at Los Angeles, Los Angeles, 1993.
- [20] Boese, K. D., Kahng, A. B., McCoy, B. A., Robins, G., "Near-Optimal Critical Sink Routing Tree Constructions", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 12, December 1995, pp. 1417-1436.
- [21] Boese, K. D., Kahng, A. B., Robins, G., "High-Performance Routing Trees with Identified Critical Sinks", Technical Report No. CS-92-37, Department of Computer Science, University of California at Los Angeles, Los Angeles, 1992.
- [22] Borah, M., Owens, R. M., Irwin, M. J., "An Edge-Based Heuristic for Steiner Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 12, December 1994, pp. 1563-1568.
- [23] Brasen, D., Saucier, G., "FPGA Partitioning for critical paths". In *The European Design and Test Conference*, IEEE, 1994, pp. 99-103.
- [24] Braun, D., Burns, J. L., Romeo, F., Sangiovanni-Vincentelli, A., Mayaram, K., "Techniques for Multilayer Channel Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 7, No. 6, June 1988, pp. 698-712.
- [25] Brayton, R. K., Rudell, R., Sangiovanni-Vincentelli, A., Wang, A. R., "MIS: A Multiple-Level Logic Optimization System", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-6, No. 6, November 1987, pp. 1062-1081.
- [26] Brown, S., "FPGA Architectural Research: A Survey", *IEEE Design & Test of Computers*, Winter 1996, pp. 9-15.
- [27] Brown, S., *Routing Algorithms and Architectures for Field-Programmable Gate Arrays*, PhD Thesis, Department of Electrical and Computer Engineering, University of Toronto, Canada, 1992.
- [28] Brown, S., Khellah, M., Lemieux, G., "Segmented Routing for Speed-Performance and Routability in Field-Programmable Gate Arrays", Technical Report, Department of Electrical and Computer Engineering, University of Toronto, Canada, 1994.
- [29] Brown, S., Khellah, M., Vranesic, Z., "Minimizing FPGA Interconnect Delays", *IEEE Design & Test of Computers*, Winter 1996, pp. 16-23.
- [30] Brown, S., Rose, J., "FPGA and CPLD Architectures: A Tutorial", *IEEE Design & Test of Computers*, Summer 1996, pp. 42-57.
- [31] Bui, T. N., Moon, B. R., "Genetic Algorithm and Graph Partitioning", *IEEE Transactions on Computers*, Vol. 45, No. 7, July 1996, pp. 841-855.
- [32] Bui, T. N., Moon, B. R., "A Genetic Algorithm for a Special Class of the Quadratic Assignment Problem", *The Quadratic Assignment and Related Problems*, DIMACS Series in Discrete Mathematics and Theoretical Computer Science, Vol. 16, 1994, pp. 99-116.

- 
- [33] Bui, T. N., Peck, A., "Partitioning Planar Graphs", *SIAM Journal of Computing*, Vol. 21, No. 2, April 1992, pp. 203-215.
- [34] Cai, H., Otten, R. J. H. M., "Conflict-Free Channel Definition in Building-Block Layout". *IEEE Transactions on Computer-Aided Design*, Vol. CAD-8, No. 9, September 1989, pp. 838-847.
- [35] Cai, Y., Wong, D. F., "Channel/Switchbox Definition for VLSI Building-Block Layout". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 12, December 1991, pp. 1485-1493.
- [36] Cai, Y., Wong, D. F., "On Minimizing the Number of L-Shaped Channels in Building-Block Layout". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 12, No. 6, June 1993, pp. 757-769.
- [37] Casotto, A., Romeo, F., Sangiovanni-Vincentelli, A., "A Parallel Simulated Annealing Algorithm for the Placement of Macro-Cells", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-6, No. 8, August 1987, pp. 838-847.
- [38] Chakravarty, S., "A Characterization of Binary Decision Diagrams", *IEEE Transactions on Computers*, Vol. 42, No. 2, February 1993, pp. 129-137.
- [39] Chan, P. K., Schlag, M. D. F., Zien, J. Y., "Spectral K-Way Ratio Cut Partitioning and Clustering", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 9, September 1994, pp. 1088-1096.
- [40] Chan, P. K., Schlag, M. D. F., Zien, J. Y., "Spectral-Based Multiway FPGA Partitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 5, May 1996, pp. 554-560.
- [41] Chandrasekharam, R., Subhranian, S., Chaudhury, S., "Genetic Algorithm for Node Partitioning Problem and Applications in VLSI Design", *IEE Proceedings-E*, Vol. 140, No. 5, September 1993, pp. 255-260.
- [42] Chang, S. C., Marek-Sadowska, M., "Technology Mapping and Circuit Depth Optimization for Field-Programmable Gate Arrays", Technical Report, Department of Electrical and Computer Engineering, University of California, Santa Barbara, 1993.
- [43] Chang, S. C., Marek-Sadowska, M., "Technology Mapping via Transformations on Function Graphs", Technical Report, Department of Electrical and Computer Engineering, University of California, Santa Barbara, 1992.
- [44] Chang, Y. W., Wong, D. F., Wong, C. K., "Universal Switch Modules for FPGA Design", Technical Report No. TR-95-27, Department of Computer Sciences, University of Texas at Austin, Austin, 1995.
- [45] Chao, T. H., Hsu, Y. C., "Rectilinear Steiner Tree Construction By Local and Global Refinement", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 3, March 1994, pp. 303-309.
- [46] Chattopadhyay, S., Roy, S., Chaudhury, P. P., "KGPMAP: Library-Based Technology-Mapping Technique for Antifuse Based FPGAs", *IEE Proc.-Comput. Digit. Tech.*, Vol. 141, No. 6, November 1994, 361-368.
- [47] Chaudry, K., Robinson, P., "Channel Routing by Sorting", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 6, June 1991.
- [48] Chen, C. D., Lee, Y. S., Wu, A. C. H., Lin, Y. L., "TRACER-fpga: A Router for RAM-Based FPGA's", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 3, March 1995, pp. 371-374.
- [49] Chen, Y. P., *Algorithms for VLSI Partitioning and Routing*, PhD Thesis, University of Texas at Austin, Austin, 1996.

- 
- [50] Cheng, C. K., Wei, Y. C., "An Improved Two-Way Partitioning Algorithm with Stable Performance", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 12, December 1991, pp. 1502-1511.
- [51] Cheng, D. I., Chang, S. C., Marek-Sadowska, M., "Partitioning Combinational Circuits in Graph and Logic Domains", Technical Report, Department of Electrical and Computer Engineering, University of California, Santa Barbara, 1993.
- [52] Chiang, C., Sarrafzadeh, M., Wong, C. K., "An Optimal Algorithm for Rectilinear Steiner Trees for Channels with Obstacles", *International Journal of Circuit Theory and Applications*, Vol. 19, 1991, pp. 551-563.
- [53] Chiang, C., Sarrafzadeh, M., Wong, C. K., "Global Routing Based on Steiner Min-Max Trees", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 12, December 1990, pp. 1318-1325.
- [54] Chiang, C., Wong, C. K., Sarrafzadeh, M., "A Weighted Steiner Tree-Based Global Router with Simultaneous Length and Density Minimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 12, December 1994, pp. 1461-1469.
- [55] Cho, T. W., Pyo, S. S., Heath, R., "PARALLEX: A Parallel Approach to Switchbox Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 6, June 1994, pp. 684-693.
- [56] Chung, K., Rose, J., "TEMPT: Technology Mapping for the Exploration of FPGA Architectures with Hard-Wired Connections", Technical Report No. TR-92-09, Department of Electrical Engineering, University of Toronto, Canada, 1992.
- [57] Cohoon, J. P., Paris, W. D., "Genetic Placement", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-6, No. 11, November 1987, pp. 956-964.
- [58] Cohoon, J. P., Hegde, S. U., Martin, W. N., Richards, D. S., "Distributed Genetic Algorithms for the Floorplan Design Problem", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 4, April 1991, pp. 483-492.
- [59] Cong, J., Hwang, Y. Y., "Structural Gate Decomposition for Depth-Optimal Technology Mapping in LUT-Based FPGA Design", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 726-729.
- [60] Cong, J., Kahng, A. B., Robins, G., Sarrafzadeh, M., Wong, C. K., "Provably Good Performance-Driven Global Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 6, June 1992, pp. 739-752.
- [61] Cong, J., Wong, D. F., Liu, C. L., "A New Approach to Three- or Four-Layer Channel Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 7, No. 10, October 1988, pp. 1094-1104.
- [62] Cormen, T. H., Leiserson, C., Rivest, R., *Introduction to Algorithms*, The MIT Press/McGraw-Hill Book Company, 1991.
- [63] Coudert, O., "On Solving Covering Problems", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 197-202.
- [64] Data I/O Corp., *EasyABEL Design Software*, San Jose, 1992.
- [65] Dewey, A., "VHDL and Next-Generation Design Automation", *IEEE Design & Test of Computers*, June 1992, pp. 6-7.
- [66] Dewey, A., De Geus, A. J., "VHDL: Toward a Unified View of Design", *IEEE Design & Test of Computers*, June 1992, pp. 8-17.
- [67] Doll, K., Johannes, F. M., Antreich, K. J., "Iterative Placement Improvement by Network Flow Methods", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 10, October 1994, pp. 1189-1195.

- 
- [68] Dunlop, A. E., Kernighan, B. W., "A Procedure for Placement of Standard-Cell VLSI Circuits", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-4, No. 1, January 1985, pp. 92-98.
- [69] Dutt, S., Deng, W., "A Probability-Based Approach to VLSI Circuit Partitioning", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 100-105.
- [70] Dutt, S., Deng, W., "A Probability-Based Approach to VLSI Circuit Partitioning", Technical Report, Department of Electrical Engineering, University of Minnesota, Minneapolis, 1996.
- [71] Ebeling, C., McMurchie, L., Hauck, S. A., Burns, S., "Placement and Routing Tools for the Triptych FPGA", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 3, No. 4, December 1995, pp. 473-482.
- [72] Eberle, H., Gehring, S., Ludwig, S., Wirth, N., "Tools for Digital Circuit Design Using FPGAs". Technical Report No. 215, Institute for Computer Systems, ETH Zürich, May 1994.
- [73] Esbensen, H., "A Genetic Algorithm for Macro Cell Placement", in *Proceedings of the European Design Automation Conference*, 1992, pp. 52-57.
- [74] Esbensen, H., Mazumder, P., "SAGA: A Unification of the Genetic Algorithm with Simulated Annealing and its Application to Macro-Cell Placement", in *Proceedings of the 7th IEEE International Conference on VLSI Design*, 1994, pp. 211-214.
- [75] Farrahi, A. H., Sarrafzadeh, M., "On the Lookup-Table Minimization Problem for FPGA Technology Mapping", Technical Report, Department of Electrical Engineering and Computer Science, Northwestern University, Evanston, 1993.
- [76] Fiduccia, C. M., Mattheyses, R. M., "A Linear Time Heuristic for Improving Network Partitions". In *19<sup>th</sup> Design Automation Conference*, 1982, pp. 175-181.
- [77] Francis, R. J., "Technology Mapping for Lookup-Table Based Field-Programmable Gate Arrays", PhD Thesis, Graduate Department of Electrical Engineering, University of Toronto, Toronto, Canada, 1993.
- [78] Frezza, S. T., Levitan, S. P., "SPAR: A Schematic Place and Route System", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 12, No. 7, July 1993, pp. 956-973.
- [79] Gajski, D. D., Dutt, N. D., Wu, C. H., Lin, Y. L., *Introduction to Chip and System Design*. Kluwer Academic Publishers, 1992.
- [80] Gajski, D. D., Vahid, F., Narayan, S., Gong, J., *Specification and Design of Embedded Systems*. P T R Prentice Hall, Englewood Cliffs, 1994.
- [81] Ganley, J. L., Cohoon, J. P., "Optimal Rectilinear Steiner Tree Routing in the Presence of Obstacles", Technical Report No. CS-94-03, Department of Computer Science, University of Virginia, Charlottesville, 1994.
- [82] Gao, T., *Performance-Driven Placement and Routing Algorithms*, PhD Thesis, University of Illinois at Urbana-Champaign, 1994.
- [83] Goldberg, D., *Genetic Algorithms in Search, Optimization, and Machine Learning*, Addison-Wesley, 1989.
- [84] Griffith, J., Robins, G., Salowe, J. S., Zhang, T., "Closing the Gap: Near-Optimal Steiner Trees in Polynomial Time", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 11, November 1994, pp. 1351-1365.
- [85] Hadley, S. W., Mark, B. L., "An Efficient Eigenvector Approach for Finding Netlist Partitions", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 7, July 1992, pp. 885-892.

- 
- [86] Hagen, L., Kahng, A. B., "New Spectral Methods for Ratio Cut Partitioning and Clustering", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 9, September 1992, pp. 1074-1085.
- [87] Hall, K. M., "An r-dimensional Quadratic Placement Algorithm", *Management Science*, Vol. 17, 1970, pp. 219-229.
- [88] Hamada, T., Cheng, C. K., Chau, P. M., "An Efficient Multilevel Placement Technique Using Hierarchical Partitioning", *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, Vol. 39, No. 6, June 1992, pp. 432-439.
- [89] Hasan, Z., Harrison, D., Ciesielski, M., "A Fast Partitioning Method for PLA-Based FPGAs", *IEEE Design & Test of Computers*, Vol. 9, December 1992, pp. 34-39.
- [90] Hauck, S., Borriello, G., "Logic Partitioning Orderings for Multi-FPGA Systems". In *International Symposium on Field-Programmable Gate Arrays*, ACM, 1995, pp. 32-38.
- [91] Ho, J. M., Vijayan, G., Wong, C. K., "New Algorithms for the Rectilinear Steiner Tree Problem", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 2, February 1990, pp. 185-193.
- [92] Ho, T., Iyengar, S. S., Zheng, S., "A General Greedy Channel Routing Algorithm", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 2, February 1991, pp. 204-211.
- [93] Hodes, T. D., McCoy, B. A., Robins, G., "Dynamically-Wiresized Elmore-Based Routing Constructions", Technical Report No. CS-93-69, Department of Computer Science, University of Virginia, Charlottesville, 1993.
- [94] Huang, D. J. H., Kahng, A. B., "When Clusters Meet Partitions: New Density-Based Methods for Circuit Decomposition". In *The European Design and Test Conference*, IEEE, 1995, pp. 60-64.
- [95] Hwang, L. J., Gamal, A., "Min-Cut Replication in Partitioned Networks", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 1, January 1995, pp. 96-106.
- [96] Hwang, T. T., Owens, R. M., Irwin, M. J., Wang, K. H., "Logic Synthesis for Field-Programmable Gate Arrays", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 10, October 1994, pp. 1280-1287.
- [97] Ihler, E., Wagner, D., Wager, F., "Modeling Hypergraphs by Graphs with the Same Min-Cut Properties". In *Info. Proc. Lett.*, Vol. 45, 1993, pp. 171-175.
- [98] Johannes, F. M., "Partitioning of VLSI Circuits and Systems". In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 83-87.
- [99] Kahng, A. B., Robins, G., "A New Class of Iterative Steiner Tree Heuristics with Good Performance", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 7, July 1992, pp. 893-902.
- [100] Kahng, A. B., Robins, G., "On Performance Bounds for a Class of Rectilinear Steiner Tree Heuristics in Arbitrary Dimension", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 11, November 1992, pp. 1462-1465.
- [101] Kim, C., Shin, H., "A Performance-Driven Logic Emulation System: FPGA Network Design and Performance-Driven Partitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 5, May 1996, pp. 560-568.
- [102] Kirkpatrick, S., Gelatt, C. D., Vecchi, M. P., "Optimization by Simulated Annealing", *Science*, No. 220, May 1983, pp. 671-680.

- 
- [103] Koch, A., "Module Compaction in FPGA-Based Regular Datapaths", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 471-476.
- [104] Kravitz, S. A., Rutenbar, R. A., "Placement by Simulated Annealing on a Multi-processor", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-6, No. 4, July 1987, pp. 534-549.
- [105] Krishnamurthy, B., "An Improved Min-Cut Algorithm for Partitioning VLSI Networks", *IEEE Transactions on Computers*, Vol. 33, No. 5, May 1984, pp. 438-446.
- [106] Kuo, M. T., Liu, L. T., Cheng, C. K., "Network Partitioning into Tree Hierarchies", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 477-482.
- [107] Lam, J., Delosme, J. M., "Performance of a New Annealing Schedule". In *International Conference on Computer Aided Design*, IEEE/ACM, 1988, pp. 510-513.
- [108] Legl, C., Wurth, B., Eckl, K., "A Boolean Approach to Performance-Directed Technology Mapping for LUT-Based FPGA Designs", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 730-733.
- [109] Li, J., Lillis, J., Liu, L. T., Cheng, C. K., "New Spectral Linear Placement and Clustering Approach", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 88-93.
- [110] Li, W. N., "The Complexity of Segmented Channel Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 4, April 1995, pp. 518-523.
- [111] Liaw, H. T., Lin, C. S., "On the OBDD-Representation of General Boolean Functions", *IEEE Transactions on Computers*, Vol. 41, No. 6, June 1992, pp. 661-664.
- [112] Lillis, J., Cheng, C. K., Lin, T. T. Y., Ho, C. Y., "New Performance-Driven Routing Techniques with Explicit Area/Delay Tradeoff and Simultaneous Wire Sizing". In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 395-400.
- [113] Lin, R. B., Shragowitz, E., "Fuzzy Logic Approach to Placement Problem", In *Proceedings of the 29<sup>th</sup> Design Automation Conference*, ACM/IEEE, 1992, pp. 153-158.
- [114] Lin, S. C., Punch, W. F., Goodman, E. D., "A Hybrid Model Utilizing Genetic Algorithms and Hopfield Neural Networks for Function Optimization", GARAGE Technical Report No. 95-01-02, Michigan State University, 1995.
- [115] Lin, Y. L., Hsu, Y. C., Tsai, F. S., "SILK - A Simulated Evolution Router", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 8, No. 10, October 1989, pp. 1108-1114.
- [116] Liu, L. T., Kuo, M. T., Cheng, C. K., "Performance-Driven Partitioning Using a Replication Graph Approach". In *Design Automation Conference*, ACM/IEEE, 1995, pp. 206-210.
- [117] Liu, L. T., Kuo, M. T., Huang, S. C., Cheng, C. K., "A Gradient Method on the Initial Partition of Fiduccia-Mattheyses Algorithm". In *International Conference on Computer Aided Design*, IEEE/ACM, 1995, pp. 229-234.
- [118] Mailhot, F., De Micheli, G., "Algorithms for Technology Mapping Based on Binary Decision Diagrams and on Boolean Operations", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 12, No. 5, May 1993, pp. 599-620.
- [119] Mallela, S., Grover, L. K., "Clustering Based Simulated Annealing for Standard Cell Placement". In *Proceedings of the 25<sup>th</sup> Design Automation Conference*, ACM/IEEE, 1988, pp. 312-317.

- [120] McCoy, B. A., Robins, G., "Non-Tree Routing", Technical Report No. CS-93-16, Department of Computer Science, University of Virginia, Charlottesville, 1993.
- [121] Michel, P., Lauther, U., Duzy, P., *The Synthesis Approach to Digital System Design*. Kluwer Academic Publishers, 1992.
- [122] De Micheli, G., *Synthesis and Optimization of Digital Circuits*. McGraw-Hill, 1994.
- [123] Mindru, F., Baruch, Z., Mindru, A., "Global Router for an Array-Based Model of FPGAs", *Acta Electrotehnica Napocensis*, Mediamira Science Publisher, Vol. 17, No. 1, pp. 63-66.
- [124] Mohan, S., Mazumder, P., "Wolverines: Standard Cell Placement on a Network of Workstations", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 12, No. 9, September 1993, pp. 1312-1326.
- [125] Nag, S., Roy, K., "Iterative Wireability and Performance Improvement for FPGAs", in *Proceedings of the 30<sup>th</sup> ACM/IEEE Design Automation Conference*, 1993, pp. 321-325.
- [126] Narendra, K. S., Thathachar, M. A. L., *Learning Automata: An Introduction*. Englewoods Cliffs, Prentice Hall, 1989.
- [127] Nedevschi, S., Pusztai, K., Baruch, Z., Creș, O., "Introducerea tehnologiei FPGA în învățământul, cercetarea și industria românească". Raport de cercetare pentru Contractul Nr. 8003/98, Tema Nr. 54, Universitatea Tehnică din Cluj-Napoca, 1998.
- [128] Oh, J., Pyo, I., Pedram, M., "Constructing Lower and Upper Bounded Delay Routing Trees Using Linear Programming", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 401-404.
- [129] Oommen, B. J., St. Croix, E. V., "Graph Partitioning Using Learning Automata", *IEEE Transactions on Computers*, Vol. 45, No. 2, February 1996, pp. 195-208.
- [130] Oommen, B. J., Ma, D. C. Y., "Deterministic Learning Automata Solutions to the Equipartitioning Problem", *IEEE Transactions on Computers*, Vol. 37, No. 1, January 1988, pp. 2-13.
- [131] Pan, P., Liu, C. L., "Optimal Clock Period FPGA Technology Mapping for Sequential Circuits", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 720-725.
- [132] Patel, D., Schlag, M., Ercegovac, M., "An Environment for the Multi-level Specification, Analysis, and Synthesis of Hardware Algorithms". *Lecture Notes in Computer Science*, Vol. 201: Functional Programming Languages and Computer Architecture, 1985, pp. 238-255.
- [133] Pusztai, K., Baruch, Z., Creș, O., "Configurarea automată a circuitelor FPGA". Raport de cercetare pentru Contractul Nr. 5003/95, Tema Nr. 124, Universitatea Tehnică din Cluj-Napoca, 1996.
- [134] Pusztai, K., Baruch, Z., Balint, P., Harsanyi, A., "Interfață cu sisteme de proiectare a circuitelor". Raport de cercetare pentru Contractul Nr. 4003/94, Tema Nr. B29, Universitatea Tehnică din Cluj-Napoca, 1995.
- [135] Pusztai, K., Baruch, Z., Creș, O., "Sistem CAD pentru proiectarea cu circuite FPGA". Raport de cercetare pentru Contractul Nr. 7003/97, Tema Nr. 32, Universitatea Tehnică din Cluj-Napoca, 1997.
- [136] Rajaraman, R., Wong, D. F., "Optimum Clustering for Delay Minimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 12, december 1995, pp. 1490-1495.



- 
- [137] Ramkumar, B., Banerjee, P., "ProperCAD: A Portable Object-Oriented Parallel Environment for VLSI CAD", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 7, July 1994, pp. 829-838.
- [138] Riess, B. M., Giselbrecht, H. A., Wurth, B., "A New k-way Partitioning Approach for Multiple Types of FPGAs". In *Asia and South Pacific Design Automation Conference*, IFIP/ACM/IEEE, 1995, pp. 313-318.
- [139] Riess, B. M., Doll, K., Johannes, F. M., "Partitioning Very Large Circuits Using Analytical Placement Techniques". In *Design Automation Conference*, ACM/IEEE, 1994, pp. 646-651.
- [140] Rose, J., "Parallel Global Routing for Standard Cells", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 10, October 1990, pp. 1085-1095.
- [141] Rose, J., Snelgrove, W., Vranesic, Z., "Parallel Standard Cell Placement Algorithms with Quality Equivalent to Simulated Annealing", *IEEE Transactions on Computer-Aided Design*, Vol. CAD-7, No. 3, March 1988, pp. 387-396.
- [142] Roussel-Ragot, P., Dreyfus, G., "A Problem Independent Parallel Implementation of Simulated Annealing: Models and Experiments", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 8, August 1990, pp. 827-835.
- [143] Rubin, S. M., *Computer Aids for VLSI Design*, Addison-Wesley Publishing Company, 1987.
- [144] Rudell, R., "Tutorial: Design of a Logic Synthesis System", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 191-196.
- [145] Saab, Y., Rao, V., "Combinatorial Optimization by Stochastic Evolution", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 4, April 1991, pp. 525-535.
- [146] Sait, S. M., Youssef, H., *VLSI Physical Design Automation*, McGraw-Hill Book Company, 1995.
- [147] Sanghavi, J., Ranjan, R. K., Brayton, R. K., Sangiovanni-Vincentelli, A., "High Performance BDD Package by Exploiting Memory Hierarchy", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 635-640.
- [148] Sarrafzadeh, M., Wong, C. K., "Hierarchical Steiner Tree Construction in Uniform Orientations". *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 11, No. 9, September 1992, pp. 1095-1103.
- [149] Schnecke, V., Vornberger, O., "An Adaptive Parallel Genetic Algorithm for VLSI-Layout Optimization", *4<sup>th</sup> International Conference on Parallel Problem Solving from Nature (PPSN IV)*, Berlin, Germany, Sept. 1996.
- [150] Schnecke, V., Vornberger, O., "Genetic Design of VLSI-Layouts", in *Proceedings of 1<sup>st</sup> IEE/IEEE International Conference on GAs in Engineering Systems: Innovations and Applications*, GALESIA '95, Sheffield, U.K., Sept. 1995, pp. 430-435.
- [151] Sechen, C., Sangiovanni-Vincentelli, A., "TimberWolf3.2: A New Standard Cell Placement and Global Routing Package", In *Proceedings of the 23<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1986, pp. 432-439.
- [152] Shahookar, K., Mazumder, P., "A Genetic Approach to Standard Cell Placement Using Metagenetic Parameter Optimization", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 9, No. 5, May 1990, pp. 500-511.
- [153] Shahookar, K., Mazumder, P., "VLSI Cell Placement Techniques", *ACM Computer Surveys*, Vol. 23, No. 2, June 1991, pp. 143-220.

- [154] Shih, P., Chang, K., Feng, W., "Neural Computation Network for Global Routing". *Computer Aided Design*, Vol. 23, No. 8, October 1991, pp. 539-547.
- [155] Shih, S., Kuh, E. S., "Circuit Partitioning Under Capacity and I/O Constraints". In *Custom Integrated Circuits Conference*, IEEE, 1994, pp. 659-662.
- [156] Shin, H., Kim, C., "A Simple Yet Effective Technique for Partitioning", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 1, No. 3, September 1993, pp. 380-386.
- [157] Skahill, K., *VHDL for Programmable Logic*, Addison-Wesley Publishing Company, 1996.
- [158] Stornetta, T., Brewer, F., "Implementation of an Efficient Parallel BDD Package", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 641-644.
- [159] Sun, Y., Wang, T. C., Wong, C. K., Liu, C. L., "Routing for Symmetric FPGA's and FPIC's", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 1, January 1997, pp. 20-31.
- [160] Texas Instruments Inc., *Field Programmable Gate Array Data Manual*. Dallas, 1993.
- [161] Thakur, S., Chang, Y. W., Wong, D. F., Muthukrishnan, S., "Algorithms for an FPGA Module Routing Problem with Application to Global Routing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 1, January 1997, pp. 32-46.
- [162] Thakur, S., Wong, D. F., "On Designing ULM-Based FPGA Logic Modules", Technical Report No. TR-94-13, Department of Computer Sciences, University of Texas at Austin, Austin, 1994.
- [163] Thakur, S., Wong, D. F., "Series-Parallel Functions and FPGA Logic Module Design", Technical Report No. TR-95-31, Department of Computer Sciences, University of Texas at Austin, Austin, 1995.
- [164] Thakur, S., Wong, D. F., "Simultaneous Area and Delay Minimum K-LUT Mapping for K-Exact Networks", Technical Report No. TR-95-12, Department of Computer Sciences, University of Texas at Austin, Austin, 1995.
- [165] Thakur, S., Wong, D. F., Krishnamoorthy, S., "Delay Minimal Decomposition of Multiplexers in Technology Mapping", In *Proceedings of the 33<sup>rd</sup> Design Automation Conference*, ACM/IEEE, 1996, pp. 254-257.
- [166] Thakur, S., Wong, D. F., Muthukrishnan, S., "Algorithms for FPGA Switch Module Routability Analysis", Technical Report No. TR-94-14, Department of Computer Sciences, University of Texas at Austin, Austin, 1994.
- [167] Togawa, N., Sato, M., Ohtsuki, T., "A Simultaneous Placement and Global Routing Algorithm for Symmetric FPGAs", *The 2nd International ACM/SIGDA Workshop on Field-Programmable Gate Arrays*, Berkeley, CA, 1994.
- [168] Tragoudas, S., "Min-Cut Partitioning on Underlying Tree and Graph Structures", *IEEE Transactions on Computers*, Vol. 45, No. 4, April 1996, pp. 470-474.
- [169] Trimmerger, S., "Field-Programmable Gate Arrays", *IEEE Design & Test of Computers*, September 1992, pp. 3-5.
- [170] Tsay, R. S., Kuh, E. S., Hsu, C. P., "PROUD: A Sea-of-Gates Placement Algorithm". *IEEE Design & Test of Computers*, December 1988, pp. 318-323.
- [171] Ullman, J. D., *Computational Aspects of VLSI*, Computer Science Press, 1984.
- [172] Vannelli, A., "An Adaptation of the Interior Point Method for Solving the Global Routing Problem", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 2, February 1991, pp. 193-203.

- 
- [173] Wegener, I., Comments on "A Characterization of Binary Decision Diagrams", *IEEE Transactions on Computers*, Vol. 43, No. 4, April 1994, pp. 383-384.
- [174] Wegener, I., "The Size of Reduced OBDD's and Optimal Read-Once Branching Programs for Almost All Boolean Functions", *IEEE Transactions on Computers*, Vol. 43, No. 11, November 1994, pp. 1262-1269.
- [175] Wei, Y. C., Cheng, C. K., "Ratio Cut Partitioning for Hierarchical Designs", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 10, No. 7, July 1991, pp. 911-921.
- [176] Woo, N. S., Kim, J., "An Efficient Method of Partitioning Circuits for Multiple-FPGA Implementation". In *Proceedings of the 30<sup>th</sup> Design Automation Conference*, ACM/IEEE, 1993, pp. 202-207.
- [177] Xilinx Inc., *The Programmable Gate Array Data Book*, San Jose, 1991.
- [178] Xilinx Inc., *XACT Development System Reference Guide*, San Jose, 1993.
- [179] Yang, H. H., Wong, D. F., "Circuit Clustering for Delay Minimization under Area and Pin Constraints", Technical Report No. TR-94-03, Department of Computer Sciences, University of Texas at Austin, Austin, 1994.
- [180] Yang, H. H., Wong, D. F., "Efficient Network Flow Based Min-Cut Balanced Partitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 12, December 1996, pp. 1533-1540.
- [181] Yang, H. H., Wong, D. F., "New Algorithms for Min-Cut Replication in Partitioned Circuits". In *International Conference on Computer Aided Design*, IEEE/ACM, 1995, pp. 216-222.
- [182] Yang, J. C. Y., De Micheli, G., "Spectral Techniques for Technology Mapping", Technical Report No. CSL-TR-91-498, Department of Electrical Engineering and Computer Science, Stanford University, Stanford, 1991.
- [183] Yeh, C. W., Cheng, C. K., Lin, T. T. Y., "A General Purpose, Multiple-Way Partitioning Algorithm", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 12, December 1994, pp. 1480-1488.
- [184] Yeh, C. W., Cheng, C. K., Lin, T. T. Y., "Circuit Clustering Using a Stochastic Flow Injection Method", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 2, February 1995, pp. 154-162.
- [185] Yeh, C. W., "On the Acceleration of Flow-Oriented Circuit Clustering", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 11, November 1995, pp. 1305-1308.
- [186] Yeh, C. W., Cheng, C. K., Lin, T. T. Y., "Optimization by Iterative Improvement: An Experimental Evaluation on Two-Way Partitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 2, February 1995, pp. 145-153.
- [187] Yu, M. L., "A Study of the Applicability of Hopfield Decision Neural Nets to VLSI CAD", In *Proceedings of the 26<sup>th</sup> Design Automation Conference*, ACM/IEEE, 1989, pp. 412-417.
- [188] Zhu, K., Wong, D. F., "A Timing-Driven Global Router for Symmetrical Array Based FPGAs", Technical Report No. TR-94-22, Department of Computer Sciences, University of Texas at Austin, Austin, 1994.
- [189] Zobrist, G. W. (Editor), *Routing, Placement, and Partitioning*, Ablex Publishing Corporation, Norwood, New Jersey, 1994.
- [190] Zurada, J. M., *Introduction to Artificial Neural Systems*, West Publishing Company, 1992.