

---

## INDEX

### 3

3DNow! multimedia extension, 164

### A

Access methods, memory, 109

Access time, 107, 108, 109, 111, 121, 122, 141, 180

Acer Laboratories, 145

Adder

BCD (binary coded decimal), 60–61, 103

carry lookahead, 55–58, 68

carry save, 58–60, 67, 69, 278

carry select, 58

decimal, 60

floating-point, 96, 271

floating-point, pipelined, 270, 273

full, 52

half, 53

multioperand, 59

parallel, 54

ripple carry, 54

serial, 60, 103

Adder-subtractor, 101, 102

Addition

BCD (binary coded decimal), 60–61

carry save, 58, 278

floating-point, 94–97

floating-point, pipelined, 270

integer, 52–61

paper and pencil, 54

ripple carry, 54

sign-magnitude, 101

Additive latency, 154

Address cache memory, 202

Address mapping. *See* Address translation

Address translation

in cache memory, 184–92

in virtual memory, 199–202

ADT (Advanced DRAM Technology) alliance, 155

Advanced DRAM Technology (ADT) alliance, 155

Algorithmic level. *See* Processor level

Algorithmic-level synthesis. *See* High-level synthesis

Alpha processors. *See* Compaq Computer products

AltiVec technology, 376

ALU (arithmetic-logic unit), 52

AMD (Advanced Micro Devices)

products

29000 family processors, 300

AMD 760 chipset, 152

Athlon Thunderbird processor, 152

- Athlon XP processor, 152  
 Amdahl, Gene M., 27  
 Amdahl's law, 27  
 ANDES (architecture with nonsequential dynamic execution scheduling), 312  
 ANN. *See* Artificial neural network  
 Apple Computer, 359  
 Application-specific integrated circuit (ASIC), 36  
 Approximate reasoning, 12  
 Arithmetic mean (of execution times), 21  
 Arithmetic pipeline, 230, 270–82  
   with feedback, 274–77  
 Arithmetic-logic unit. *See* ALU  
 ARM (advanced RISC machine), 301  
 Array divider, 82–83  
 Array multiplier, 71, 73  
 Array multiplier, pipelined, 278  
 Array processor, 7  
 Artificial neural network (ANN), 10  
   hardware implementation of, 12  
   learning methods, 11  
   learning rule, 11  
   models, 11  
 ASIC (application-specific integrated circuit), 36  
 Associative mapping, in cache memory, 184–85  
 Associative memory, 109, 174–78  
   cell, 176  
 Associative processing, 178  
 Associative processor, 178  
 Asynchronous exception, 365  
 AT&T, 301, 302  
 AT&T products  
   92010 processor, 301  
   DSP32C DSP processor, 301  
 ATM (asynchronous transfer mode), 300, 379  
 Auto precharge, memory, 131  
 Auto refresh, memory, 132  
 Average latency, pipeline, 285  
 Axon, 10
- B**
- Bandwidth, of memory, 112, 135, 153, 164, 165  
   peak, 124, 148, 158, 162, 163  
   sustained, 124, 162  
 Bandwidth, of pipeline, 230  
 Base address, 200  
 Baugh, C. R., 73  
 Baugh-Wooley multiplication algorithm, 73  
 BCD adder, 60–61, 103  
 BEDO DRAM (burst extended data out DRAM), 127–28  
 Behavioral representation, 34  
 Benchmark programs, 20–26  
   evolution of, 23  
   kernel benchmarks, 23  
   synthetic benchmarks, 23  
 Berkeley IRAM project, 167  
 Berkeley ISTORE project, 167  
 Best fit memory allocation, 209  
 BHT. *See* Branch history table  
 Bias (for floating-point numbers), 85  
 Biased representation, 86  
 BiCMOS (bipolar-CMOS) technology, 306  
 BIOS (basic input-output system), 140  
 Bipolar transistor, 113  
 BIPS (billions of instructions per second), 18  
 Block address translation (BAT) array, 363, 366, 367, 369  
 Block, cache, 179  
 Booth multiplication algorithm, 66–67  
   modified, 103  
 Booth, Andrew D., 66  
 Bottleneck  
   of pipeline, 228, 235  
   von Neumann, 178  
 Bottleneck problem, 235  
 Branch following, 327  
 Branch history table (BHT), 248, 259, 368  
   of PowerPC 750 processor, 371

Branch instruction, 244  
Branch penalty, 245  
Branch prediction, 246–50, 262  
  1-bit, 247  
  2-bit, 248  
  counter-based, 247  
  dynamic, 247, 249  
  effect on performance, 249  
  in Alpha 21064A processor, 341  
  in Alpha 21264 processor, 352–53  
  in MIPS R10000 processor, 314  
  in PowerPC 750 processor, 370  
  in the Intel Architecture, 251  
  in UltraSPARC architecture, 327  
  static, 246, 249  
Branch target buffer (BTB), 248, 251, 254, 264  
Branch target cache, 258  
BTB. *See* Branch target buffer  
Burst mode transfer, 127, 128, 131, 132, 133, 134, 137, 139, 149, 150  
Bus  
  transaction-oriented, 255  
Bypassing, 239

## C

Cache data memory, 179, 186, 191  
Cache hit, 180  
Cache memory, 107, 179–98  
  address, 202  
  address mapping, 184–92  
  associative mapping, 184–85  
  block, 179  
  data (D-cache), 109, 193  
  direct mapping, 185–89  
  direct-mapped, 137, 142, 155  
  fully associative, 142  
  instruction (I-cache), 109, 193, 257  
  L1 (level 1), 164, 187, 193, 255  
  L2 (level 2), 193, 255  
  line, 179  
  look-aside, 180  
  look-through, 180  
  of Alpha 21064A processor, 341

  of Alpha 21164 processor, 349  
  of Alpha 21264 processor, 357  
  of MIPS R10000 processor, 315  
  of MIPS R5000 processor, 317  
  of MIPS R8000 processor, 314  
  of MIPS-III architecture, 310  
  of PowerPC 601 processor, 363  
  of PowerPC 750 processor, 375  
  of UltraSPARC architecture, 330  
  operation of, 181–84  
  organization of, 179–81  
  performance of, 193–95  
  replacement policy, 192–93  
  set-associative, 142  
  set-associative mapping, 189–92  
  snooping, 196  
  split, 109, 193  
  tag, 179  
  types of, 193  
  unified, 109, 193  
  write-back, 183  
  write-through, 184, 195  
Cache memory coherence problem, 183, 195–98  
Cache memory consistence problem.  
  *See* Cache memory coherence  
  problem  
Cache miss, 180  
Cache tag memory, 180, 186, 188, 191  
CAD (computer-aided design), 39, 43  
CAD editor, 39  
CAD tools, 39  
CAM (content addressable memory),  
  174  
  comparison, 174  
  exact match, 174  
Carry generate function, 56  
Carry lookahead adder (CLA), 55–58,  
  68  
Carry propagate function, 56  
Carry save adder (CSA), 58–60, 67, 69  
Carry select adder, 58  
CAS (column address strobe), 119

- CAS latency, 122, 124, 128, 131, 133, 135, 136, 137, 140, 141, 146, 149, 150, 155, 162
- CDB (common data bus), 239
- CDRAM (cached DRAM), 142
- Central processing unit. *See* CPU
- CFP2000, 26
- CFP95, 24
- Characteristic (for floating-point numbers), 85
- CINT2000, 26
- CINT95, 24
- Circuit level, 35
- CISC (complex instruction set computer) architecture, 293
- CLA (carry lookahead adder), 55–58, 68
- Clock access time, 134, 136
- Clock cycle time, 133
- CMOS technology, 269
- Collision matrix, pipeline, 287
- Collision vector, pipeline, 284, 286
- Collision, in pipeline, 231, 282
- Column access, 140
- Column access time, 122, 134, 137, 141
- Common data bus (CDB), 239
- Compaction, memory, 206, 210
- Compaq Computer Corporation, 337
- Compaq Computer products
- Alpha 21064 processor, 247, 338
  - Alpha 21064A processor, 338–43
  - Alpha 21066 processor, 343
  - Alpha 21066A processor, 344
  - Alpha 21068 processor, 344
  - Alpha 21164 processor, 344–49
  - Alpha 21264 processor, 166, 349–59
  - Alpha 21364 processor, 165
- Comparison CAM, 174
- Complex instruction set computer (CISC) architecture, 293
- Computer-aided design. *See* CAD
- Content addressable memory (CAM), 174
- Control Data computers
- CDC 6600, 241
  - Control Data Corp., 241
  - Control hazard, 236, 244–51
  - Control memory, 232
  - Control parallelism, 10
  - Control speculation, 267
  - Controller synthesis, 40
  - Convolution, 292
  - Copy-back policy. *See* Write-back policy
  - CPI (cycles per instruction), 15, 16
  - CPU (central processing unit), 52
    - microprogrammed, 232
    - organization, 256
    - performance, 14, 15
  - CPU time, 13, 14, 15
  - CPU2000, 25
  - CPU95, 24
  - CRIMM (continuity RIMM), 157, 172
  - CSA (carry save adder), 58–60
  - Current window pointer (CWP), 296
  - CWP (current window pointer), 320
  - Cycle time, 111, 121
  - Cypress Semiconductor, 321
- D**
- Data cache (D-cache), 109, 193
- Data dependency. *See* Data hazard
- Data flow architecture, 6
  - dynamic, 7
  - static, 7
- Data hazard, 236–44
  - RAW (read after write), 238
  - WAR (write after read), 238
  - WAW (write after write), 238
- Data parallelism, 10
- Data path synthesis, 40
- Data stream, 1
- Data translation buffer (DTB)
  - of Alpha 21064A processor, 340, 341
  - of Alpha 21164 processor, 345, 348
  - of Alpha 21264 processor, 358

- DDR II SDRAM (double data rate II SDRAM), 153–56
  - DDR IIa SDRAM (double data rate IIa SDRAM) SDRAM, 155
  - DDR III SDRAM (double data rate III SDRAM), 153
  - DDR SDRAM (double data rate SDRAM), 148–52
  - DDR-200 SDRAM (PC1600), 151
  - DDR-266 SDRAM (PC2100), 151
  - DDR-266A SDRAM (PC2100A), 152
  - DDR-300 SDRAM (PC2400), 151
  - DDR-333 SDRAM (PC2700), 151
  - DDR-400 SDRAM (PC3200), 153
  - DDR-533 SDRAM (PC4300), 153
  - DDR-800 SDRAM (PC6400), 153
  - Decimal adder, 60
  - Delayed branch, 250, 258
  - Delayed load, 258
  - Delta delay, 46
  - Demand-paged virtual memory, 216, 220
  - Denormal numbers, 91
  - Design problem, 38
  - Design process, 38–41
  - Design tasks, 38
    - abstraction, 38
    - analysis, 38
    - extraction, 38
    - generation, 38
    - optimization, 38
    - refinement, 38
    - synthesis, 38
  - Destructive readout (DRO), 110, 113
  - Deterministic networks, 11
  - Dhrystone, 23
  - Digital Equipment Corporation (DEC), 337
  - DIMM (dual in-line memory module), 140, 145, 149, 153, 171
  - DIP (dual in-line package), 171
  - Direct mapping, in cache memory, 185–89
  - Direct-access memory, 109
  - Direct-mapped cache memory, 137, 142, 155
  - Dirty bit, in cache memory, 183
  - Dirty bit, in paging, 205
  - Dividend, 73
  - Divider circuit
    - array, 82–83
    - combinational, 82
    - restoring, 74, 77
  - Division
    - floating-point, 97
    - higher-radix, 82
    - integer, 73–84
    - nonrestoring, 78–79, 80, 81
    - restoring, 74–78, 82
    - signed, 84
    - SRT (Sweeney, Robertson, Tocher), 79–81
  - Divisor, 73
  - Doubled bank organization, 162
  - DRAM (dynamic random-access memory), 113
    - asynchronous, 124
    - categories of, 124
    - protocol based, 125
    - synchronous, 125
    - technologies, 124–70
  - DRDRAM (direct Rambus DRAM).  
*See* Rambus DRAM
  - DSP (digital signal processing), 301
  - DTB. *See* Data translation buffer
  - Dual-bank memory, 127
  - Dynamic address translation, 200
  - Dynamic data flow architecture, 7
  - Dynamic dependency checking, 239
  - Dynamic memory, 111
  - Dynamic pipeline, 231, 282
  - Dynamic pipeline scheduling, 286
- E**
- Early auto-precharge, 141
  - ECC (error correction code), 112, 164, 169, 171, 311, 325, 349

- ECL (emitter coupled logic)
    - technology, 306
  - EDC (error detection code), 112
  - EDO DRAM (extended data out DRAM), 126–27
  - EEPROM (electrically erasable programmable read-only memory), 110
  - Effective address, 200, 217
  - Efficiency, of pipeline, 230
  - EIA (Electronic Industries Association), 128
  - Elapsed time, 13
  - Electrically erasable programmable read-only memory. *See* EEPROM
  - Embedded processor, 300
  - Enhanced DDR II SDRAM, 155
  - Enhanced Memory Systems, 137, 140, 155
  - Enhanced Memory Systems products
    - SM2604 ESDRAM, 141
    - SM3603, SM3604 HSDRAM, 136
  - EPIC (explicitly parallel instruction computing), 263–69
  - EPROM (erasable programmable read-only memory), 110
  - Erasable programmable read-only memory. *See* EPROM
  - Error correction code (ECC), 112, 164, 169, 171, 311, 325, 349
  - Error detection code (EDC), 112
  - ESDRAM (enhanced SDRAM), 137–42
  - ESDRAM-lite, 140, 155
  - Exact match CAM, 174
  - Exception
    - asynchronous, 365
    - imprecise, 365
    - in Alpha 21264 processor, 355
    - in MIPS architecture, 311
    - in PowerPC architecture, 364
    - precise, 303, 312, 365
    - synchronous, 365
  - Exceptions, 92
    - divide-by-zero, 93
    - inexact, 93
    - invalid, 93
    - overflow, 93
    - underflow, 93
  - Execution time, 13
  - Explicitly parallel instruction computing (EPIC), 263–69
  - Exponent, 85
- F**
- FCRAM (fast cycle RAM), 145–48
  - Feed-forwarding. *See* Forwarding
  - Fetching problem, 235
  - FIFO (first-in, first-out) replacement policy, 212
  - First fit memory allocation, 208
  - Fixed-point number representation, 84
  - Flash memory, 110, 148
  - Flat memory model, in the Intel Architecture, 219
  - Floating-point adder, 96, 271
  - Floating-point adder, pipelined, 270, 273
  - Floating-point number representation, 84–93
    - IBM System/360 format, 271
    - IEEE 754 floating-point standard, 88
  - Floating-point operations, 93–99
    - addition, 94–97
    - division, 97
    - multiplication, 97–99
    - precision, 100
    - rounding, 92, 100, 101
    - subtraction, 94–97
  - Floating-point unit
    - of Alpha 21264 processor, 356
    - of MIPS R10000 processor, 314
    - of MIPS R4400 processor, 310
    - of MIPS R8010 coprocessor, 314
    - of PowerPC 601 processor, 361
    - of PowerPC 750 processor, 373
    - of UltraSPARC architecture, 328
  - Flynn's taxonomy, 1, 2

Forbidden latency, pipeline, 284  
 Forbidden list, pipeline, 284, 286  
 Forwarding, 239, 263, 322  
 FPM DRAM (fast page mode DRAM), 125–26  
 Fragmentation, memory, 209  
   external, 206  
   internal, 206  
 Front side bus (FSB), 135, 152, 153  
 FRP (fully resolved predicate), 268  
 FSB (front side bus), 135, 152, 153  
 Fujitsu, 147, 148, 300, 321  
 Fujitsu Microelectronics, 145  
 Fujitsu products  
   MB81E161622 FCRAM, 147  
   MB82D01160 Mobile FCRAM, 148  
   MB82D01171A Mobile FCRAM, 148  
   SPARClite embedded processor, 300, 321, 323  
 Full adder, 52  
 Full subtracter, 53  
 Fully resolved predicate (FRP), 268  
 Fully-associative cache memory, 142  
 Fuzzy logic, 12  
   accelerators, 13  
   applications, 12  
   controller, 12  
   processors, 12

## G

GaAs (gallium arsenate) technology, 269  
 Gate level. *See* Logic level  
 GDT (global descriptor table), 217  
 Geometric mean (of execution times), 22  
 Global descriptor table (GDT), 217  
 Gradual underflow, 91, 92  
 Graphics Performance Characterization Group (GPCG), 24  
 Graphics unit  
   of UltraSPARC architecture, 331  
 Guard digit, 100

## H

Half adder, 45, 53  
 Half subtracter, 53  
 Hardware description language (HDL), 36, 41  
 Harvard Mark I computer, 295  
 Harvard-based architecture, 295  
 Hazard, pipeline  
   control, 236  
   data, 236  
   structural, 236  
 HDL (hardware description language), 36, 41  
 HDTV (high-definition television), 301  
 Hennessy, John, 300  
 Heterogeneous multiprocessor, 4  
 Heuristic, 39  
 Hewlett-Packard Laboratories, 263  
 Hidden auto-precharge, 137, 140  
 Hidden bit, 86  
 Hidden RAS-to-CAS delay, 137, 141  
 Hierarchy of memories, 105–9  
 High Performance Group (HPG), 24  
 Higher-radix division, 82  
 Higher-radix multiplication, 81  
 High-level synthesis, 40  
 Hill, Mark D., 194  
 Hit ratio, 106, 193  
 Hit time, 107  
 Homogeneous multiprocessor, 4  
 Horizontal microinstruction, 261  
 HSDRAM (high speed SDRAM), 136  
 Hybrid architecture, 9  
 HyperPage Mode memory. *See* EDO DRAM  
 Hyundai Microelectronics, 145, 155

## I

IBM (International Business Machine), 299, 300, 359  
 IBM products  
   801 minicomputer, 299  
   AS/400 computers, 360

- PC/RT computer, 299
- RIOS processor, 360
- RS/6000 computers, 360
- System/360 computer, 239, 271
- System/370 computer, 232
- IEEE (Institute of Electrical and Electronics Engineers) Computer Society, 88
- IEEE 754 floating-point standard, 88–93
- IEEE standard 1076-1987, 42
- IEEE standard 1076-1993, 42
- If-conversion, 267
- ILP (instruction-level parallelism), 256, 263, 270
- Imprecise exception, 365
- Impure zero, 86
- Independent bank organization, 162
- Inertial delay, 46
- Inexact exception, 93
- Infineon Technologies AG, 152, 155
- Inmos transputer, 300
- Instruction
  - issue, 256
  - prefetch, 235, 266
  - prefetch, multiple, 251
  - stall, 237, 252, 265
- Instruction buffer, 257
- Instruction cache (I-cache), 109, 193, 257
- Instruction frequency, 16
- Instruction mix, 16
- Instruction pipeline, 230, 232–70
  - throughput improvement of, 256–70
- Instruction queue. *Sæ* Instruction buffer
- Instruction stream, 1
- Instruction translation buffer (ITB)
  - of Alpha 21064A processor, 341
  - of Alpha 21164 processor, 345, 347
  - of Alpha 21264 processor, 354
- Instruction-level parallelism (ILP), 256, 263, 270
- Integer operations
  - addition, 52–61
  - division, 73–84
  - multiplication, 61–73
  - subtraction, 53, 54, 55
- Integrated Device Technology (IDT), 300
- Integrated Device Technology products
  - 71256 SRAM, 188
- Intel, 128, 129, 133, 152, 155, 156, 162, 163
- Intel Architecture
  - branch prediction, 251
  - memory management, 216–22
  - microarchitecture, 258
  - pipeline, 251–55
- Intel Architecture processors. *Sæ* Intel products
- Intel products
  - 80x86 processors, 206
  - Foster processor, 152
  - i430TX chipset, 129
  - i430VX chipset, 129
  - i440BX chipset, 133
  - i820 (Camino) chipset, 162
  - i840 chipset, 163
  - i850 chipset, 163
  - i860 chipset, 163
  - i860 RISC processor, 300
  - i960 RISC processor, 300
  - Intel Architecture processors, 216, 260, 300
  - Itanium processor, 152, 164
  - iWarp processor, 300
  - McKinley procesor, 152
  - Pentium 4 processor, 152, 254
  - Pentium III Coppermine processor, 152
  - Pentium III processor, 254
  - Pentium processor with MMX extensions, 260
  - Pentium processors, 206, 260
- Interleaved memory, 173–74
- Interlock, pipeline, 237
- Invalid exception, 93



IRAM (intelligent RAM), 165–70  
ITB. *See* Instruction translation buffer

## J

JEDEC (Joint Electron Device Engineering Council), 128, 140, 142, 149, 153, 155

## L

L1 (level 1) cache memory, 164, 187, 193, 255  
L2 (level 2) cache memory, 128, 193, 255  
Latency  
  additive, 154  
  of memory, 135, 164, 165  
  of pipeline, 229, 283  
  write, 154  
LDT (local descriptor table), 217  
Learning rule, for an ANN, 11  
Least frequently used replacement policy, 192  
Lee, J. K., 246  
Library mapping. *See* Technology mapping  
Line, cache, 106, 179  
Linear address, 216, 218  
Linpack, 23  
Livermore Loops, 23  
Load/store architecture, 16, 298, 299, 306  
Local descriptor table (LDT), 217  
Locality of reference, 29, 105, 179, 187, 202  
Logic level, 36  
Logical address, 199, 217  
Logic-level synthesis, 41  
Loosely coupled multiprocessor, 4  
LRU (least recently used) replacement policy, 192, 213  
LSI Logic, 300, 321

## M

Macro-cell, 36  
Main memory, 107  
MAJC (microprocessor architecture for Java computing), 262, 333  
MAL (minimum average latency), pipeline, 285  
Mantissa, 85  
Matrix multiplication, 280  
MCM (multi-chip module), 37  
MDRAM (multi-bank DRAM, MoSys DRAM), 148  
Mean time between failures (MTBF). *See* MTBF  
Memory  
  access methods of, 109  
  allocation, 207–11  
  associative, 109, 174–78  
  cache, 107, 179–98  
  cell, 112–14  
  contention, 4, 174  
  design of, 118–19  
  direct access, 109  
  dynamic, 111  
  electrically erasable programmable read only, 110  
  erasable programmable read only, 110  
  hierarchy, 105–9  
  interleaved, 173–74  
  module, 171–73  
  organization of, 115–18  
  performance of, 111–12, 121–24, 133–34  
  programmable read only, 110  
  random access, 109, 110, 112, 113  
  read only, 110  
  replacement policy, 107, 192–93, 207, 211–16  
  sequential access, 109  
  static, 111  
  technologies, 124–70  
  types of, 109–11  
  unit, 114

- virtual, 198–222
- volatile, 113
- Memory address table, 200, 206
- Memory allocation
  - best fit, 209
  - first fit, 208
  - non-preemptive, 208
  - preemptive, 210
  - worst fit, 210
- Memory compaction, 206, 210
- Memory fragmentation, 209
  - external, 206
  - internal, 206
- Memory management
  - in PowerPC 601 processor, 363
  - in the Intel Architecture, 216–22
  - in the MIPS architecture, 311
- Memory management unit (MMU), 200
  - of MIPS R4400 processor, 304
  - of PowerPC 750 processor, 374
  - of PowerPC 860 processor, 380
  - of UltraSPARC-IIi processor, 329
- MERSI cache-coherence protocol, 377
- MESI (modified, exclusive, shared, invalid) cache-coherence protocol, 196–98, 255
- Message-passing mechanism, 5
- MFLOPS (millions of floating-point operations per second), 19
- Microarchitecture level. *See* Register-transfer level (RTL)
- Microinstruction
  - horizontal, 261
- Micron Technology, 152, 155
- Micron Technology products
  - MT4LC8M8E1 64-Mbit DRAM, 119
- Microoperation, 251
- Microprogram counter, 232
- Microprogrammed CPU, 232
- MIMD (multiple instruction, multiple data) computer, 2
- Minimum average latency (MAL), pipeline, 285
- Minimum latency, pipeline, 286
- Minuend, 53, 54, 55
- MIPS (microprocessor without interlocking pipe stages), 300, 302
- MIPS (millions of instructions per second), 17
- MIPS Computer Systems, 302
- MIPS Computer Systems products
  - R10000 processor, 258, 312
  - R2000 processor, 302
  - R3000 processor, 303
  - R3001 controller, 303
  - R3500 processor, 303
  - R4000 processor, 260, 303
  - R4300i processor, 304
  - R4400 processor, 260, 304
  - R4600 processor, 305
  - R4650 processor, 305
  - R4700 processor, 306
  - R5000 processor, 315
  - R8000 processor, 312–15
- MIPS Technology, 302, 312
- MISD (multiple instruction, single data) computer, 1
- Miss penalty, 107
- Miss ratio, 107, 194
- MMU (memory management unit), 200
- MMX (multimedia extensions), 253, 254
- Modified Booth multiplication algorithm, 103
- MOS (metal-oxide semiconductor) transistor, 113
- Motion video instructions (MVI) extension, 345, 350
- Motorola, 301, 359, 360
- Motorola products
  - 5600x DSP processor, 301
  - 88000 series processors, 300
  - 9600x DSP processor, 301
  - MC98601 processor, 360
  - MPC7400 processor, 376–78
  - MPC850 processor, 379–82
  - MPC860 processor, 379–82

- MTBF (mean time between failures), 112
- Multi-bank memory, 128, 156
- Multi-chip module (MCM), 37
- Multicomputer, 4
- Multifunction pipeline, 274
- Multi-multiprocessor, 5
- MultiOp instruction, 264
- Multiple prefetching, 251
- Multiplicand, 61
- Multiplication
- Booth, 66–67
  - floating-point, 97–99
  - higher-radix, 81
  - integer, 61–73
  - matrix, 280
  - on groups of bits, 81
  - paper and pencil, 62
  - shift-and-add, 62–65
  - shifting over ones, 71
  - shifting over zeros, 70
- Multiplier, 61
- Multiplier circuit
- array, 71, 73
  - array, pipelined, 278
  - Booth, 66
  - Booth and Wallace tree, 69
  - Booth and Wallace tree, two-pass, 70
  - combinational, 68, 69, 71, 73
  - for matrix multiplication, 280
  - pipelined, 277–79
  - pipelined, Wallace tree, 279
  - shift-and-add, 62, 64
  - Wallace tree, 68
  - with systolic array, 280
- Multiprocessor, 3
- heterogeneous, 4
  - homogeneous, 4
  - loosely coupled, 4
  - tightly coupled, 4
- Multiprocessor parallelism, 256
- Multiprogramming, 198
- Multi-segment memory model, in the Intel Architecture, 219
- N**
- NaN (not a number), 92
- Native MFLOPS rating, 19
- NEC Corporation, 142, 145, 300, 302, 312
- NEC Hitachi Memory, 145, 155
- NEC products
- V-800 processor, 301
  - VR10000 processor, 312
- Negative overflow, 87
- Negative underflow, 87
- Nintendo video game, 170
- Non-destructive readout (NDRO), 110, 113
- Non-preemptive memory allocation, 208
- Nonrestoring division, 78–79, 80, 81
- Non-uniform memory access (NUMA) architecture, 333
- Non-unit assumed latency (NUAL) operation, 265
- Nonvolatile memory, 111
- Normalized floating-point number, 86
- Normalized MFLOPS rating, 19
- Not a Number (NaN), 92
- NUAL (non-unit assumed latency) operation, 265
- NUMA (non-uniform memory access) architecture, 333
- O**
- Open Systems Group (OSG), 24
- OPT (optimal) replacement policy, 211
- Out-of-order execution, 166, 253, 312
- Overflow, 88, 93
- Overlapping register windows, 296
- P**
- Page, 202, 205, 220
- Page directory, 218, 220
- Page fault, 203, 204
- Page fault frequency, 204, 212

- Page frame, 202
- Page hit, 123
- Page hit latency, 124
- Page miss, 123
- Page miss latency, 124, 137
- Page mode access, 122, 125
- Page mode cycle time, 123
- Page table, 202, 205, 218, 220
- Page-fault exception, 220
- Paging, 202–5
  - in the Intel Architecture, 220
- Paging and segmentation, 206–7
- PALcode (privileged architecture library), of Alpha processors, 341
- Palmtop computer, 301
- Paper and pencil multiplication, 62
- Parallel adder, 54
- Parallelism, 262
  - instruction-level, 256, 263, 270
  - multiprocessor, 256
  - spatial, 256
- Patterson, David A., 167, 296, 300
- PC100 SDRAM, 130, 133, 136
- PC133 SDRAM, 130, 133, 136, 147
- PC150 SDRAM, 133
- PC1600 SDRAM (DDR-200), 151
- PC2100 SDRAM (DDR-266), 151
- PC2100A SDRAM (DDR-266A), 152
- PC2400 SDRAM (DDR-300), 151
- PC2700 SDRAM (DDR-333), 151
- PC3200 SDRAM (DDR-400), 153
- PC4300 SDRAM (DDR-533), 153
- PC600 Rambus DRAM, 173
- PC6400 SDRAM (DDR-800), 153
- PC66 SDRAM, 130
- PC700 Rambus DRAM, 173
- PC800 Rambus DRAM, 173
- PDA (personal digital assistant), 170, 301, 365
- Peak bandwidth, 124, 148, 158, 162, 163
- Pentium processors. *See* Intel products
- Percentage of vectorization, 32
- Performance, 13
  - cache memory, 193–95
  - CPU, 13–26
    - memory, 111–12, 121–24, 133–34
    - pipeline, 229–30, 245, 246
    - processor, 165
- Philips, 300
- Physical address, 199, 217, 218
- Physical representation, 35
- Pipeline
  - arithmetic, 230, 270–82
  - average latency, 285
  - bandwidth, 230
  - bottleneck, 228
  - collision matrix, 287
  - collision vector, 284, 286
  - control, 282–88
  - control hazard in, 244–51
  - data hazard in, 236–44
  - dynamic, 231, 282
  - efficiency, 230
  - forbidden latency, 284
  - forbidden list, 284, 286
  - instruction, 230, 232–70
  - latency, 229, 283
  - minimum average latency (MAL), 285
  - minimum latency, 286
  - multifunction, 274
  - of Intel Architecture, 251–55
  - of MIPS processors, 306
  - of UltraSPARC architecture, 327
  - performance, 229–30, 245, 246
  - reservation table, 283
  - scheduling, 282
  - stage, 228
  - state diagram, 284, 287
  - static, 230, 282
  - structural hazard in, 228–29
  - structure, 228
  - throughput, 285
  - types, 230
  - utilization of, 235
- Pipeline interlock, 237
- Pipelined
  - ALU, of MIPS R5000 processor, 317

- array multiplier, 278
  - floating-point adder, 270, 273
  - microprogram control unit, 232
  - multiplier, 277–79
  - multiplier, Wallace tree, 279
  - multiplier, with carry save adders, 279
  - vector processor, 8
  - write operations, in the MIPS R5000 processor, 318
  - Pipelining, 127, 139, 145, 228
  - Positive overflow, 87
  - Positive underflow, 87
  - Posted-CAS enhancement, 154, 155
  - POWER (performance optimized with enhanced RISC) architecture, 360
  - PowerPC processors
    - 601, 360–65
    - 602, 365–66
    - 603 and 603e, 366–67
    - 604 and 604e, 367–68
    - 740 and 750, 368–76
    - 7400, 376–78
    - 850 and 860, 379–82
  - Precharge, memory, 128, 132, 137, 144, 146, 147, 149, 150, 155, 160, 162
  - Precise exception, 303, 365
  - Predicated execution, 266
  - Preemptive memory allocation, 210
  - Prefetch
    - instruction, 235, 266
    - instruction, multiple, 251
    - memory, 144, 164
  - Principle of locality, 211
  - Processing elements (PEs), 7, 9, 10
  - Processing nodes (PNs), 4, 7
  - Processor level, 36
  - Processor throughput, 20
  - Processor utilization, 20
  - Programmable read-only memory. *See* PROM
  - PROM (programmable read-only memory), 110
  - Protected flat memory model, in the Intel Architecture, 219
  - Pure zero, 86
- Q**
- QRSL (quad Rambus signaling level), 158
  - Quad Serializer / Deserializer (SerDes) signaling, 158
  - Quality factors, 26
  - Quantum, in multiprogramming, 198
- R**
- RAID (redundant array of inexpensive disks), 300
  - RAM (random-access memory), 109, 110, 112
    - access circuitry, 117
    - dynamic (DRAM), 113
    - static (SRAM), 113
  - Rambus channel, 156, 163, 172
  - Rambus device, 162, 163
  - Rambus DRAM, 156–65
  - Rambus Inc., 152, 156, 162, 163
  - Rambus packet, 160
  - Rambus transaction, 161
  - Ramtron International Corp., 137
  - Random access time, 122, 136, 147, 171, 173
  - Random cycle time, 134, 136, 147
  - Random replacement policy, 192, 225
  - Random-access memory. *See* RAM. *See* RAM
  - RAS (Row Address Strobe), 119
  - RAS precharge time, 122, 124, 137, 141
  - RAS-to-CAS delay, 122, 124, 131, 133, 135, 136, 137, 140, 141
  - RAW (read after write) hazard, 238
  - RDRAM (Rambus DRAM). *See* Rambus DRAM
  - Read-only memory. *See* ROM
  - Read-write memory, 110
  - Real address, 199

- Reduced instruction set computer (RISC) architecture, 293
  - Redundant quotient representation, 81
  - Refreshing, memory, 111, 113, 144, 155
  - Register, 107
  - Register file, 107, 236
  - Register renaming, 259, 354
  - Register-transfer level (RTL), 36
  - Register-transfer level synthesis, 40
  - Reinforcement learning, 11
  - Relative address, 200
  - Reliability, of memory, 112
  - Replacement policy, 107
    - FIFO (first-in, first-out), 212
    - in cache memory, 192–93
    - in virtual memory, 207, 211–16
    - least frequently used, 192
    - LRU (least recently used), 192, 213
    - OPT (optimal), 211
    - random, 192, 225
    - SLRU (simplified least recently used), 226
    - stack, 213–16
  - Replicating, execution unit, 236
  - Reservation station, 239
  - Reservation table, pipeline, 283
  - Resource allocation, 40
  - Resource assignment, 40
  - Response time, 13
  - Restoring division, 74, 82
  - RIMM (Rambus in-line memory module), 157, 172
  - Ripple borrow subtracter, 102
  - Ripple carry adder, 54
  - Ripple carry addition, 54
  - Ripple carry subtracter, 54
  - RISC (reduced instruction set computer) architecture, 293
    - advantages of, 294–96
    - applications of, 299–301
    - characteristics of, 298–99
    - VLSI implementation, 295
    - vs. CISC architecture, 299
  - RISC processors, 302–83
  - RLDRAM (Reduced Latency DRAM), 152
  - Robertson multiplication algorithm, 73
  - Robertson, James E., 79
  - ROM (read-only memory), 110
  - Ross Technology, 321, 322
  - Ross Technology products
    - HyperSPARC processor, 322
  - Round digit, 100
  - Rounding, 92, 100, 101
  - Row access time, 140. *See* Random access time
  - RSL (Rambus signaling level), 158
  - RTL (register-transfer level), 36
  - RTOS (real-time operating system), 309
- S**
- Samsung Electronics, 155
  - Scalable shared memory (SSM) architecture, 333
  - Scheduling, 40
    - dynamic pipeline, 286–88
    - static pipeline, 283–86
  - Scheduling, pipeline, 282
  - Scientific notation, 85
  - Scoreboard method, 241–44, 258
  - SDRAM (synchronous DRAM), 128–36
  - Secondary memory, 107
  - Segment, 205, 218
  - Segment descriptor, 217
  - Segment descriptor table, 217
  - Segment selector, 217
  - Segmentation, 205–6
    - in the Intel Architecture, 219–20
  - Semiconductor memory, 112–73
  - Sense amplifier, 112, 137, 138, 141, 142, 156, 160, 162
  - Sequential locality, 106
  - Sequential-access memory, 109
  - Sequin, C., 296
  - Serial adder, 60, 103
  - Serial subtracter, 103

- Set-associative cache memory, 142
- Set-associative mapping, in cache memory, 189–92
- Shift-and-add multiplication, 62–65
- Shifting-over-ones multiplication, 71
- Shifting-over-zeros multiplication, 70
- Siemens, 300
- Signed division, 84
- Significand, 89
- Silicon compiler., 39
- Silicon Graphics, Inc. (SGI), 302
- Silicon Integrated Systems, 145
- Silicon Integrated Systems products
  - SiS5571 chipset, 129
- SIMD (single instruction, multiple data) computer, 2
- SIMD (single instruction, multiple data) extensions, 254
- SIMM (single in-line memory module), 171
- Simulator, 39
- SISD (single instruction, single data) computer, 1
- SLDRAM (SyncLink DRAM), 148
- SLRU (simplified LRU) replacement policy, 226
- Smith, A. J., 246
- Snoop read hit, 196
- Snoop write hit, 196
- Snooping, in cache memory, 196
- SODIMM (small outline dual in-line memory module), 172
- Sony, 300, 302
- SPARC (scalable processor architecture), 300, 320
- SPARC Compliance Definition (SCD), 321
- SPARC International, 321
- SPARC processors
  - HyperSPARC, 322
  - MicroSPARC, 323
  - MicroSPARC-II, 323
  - SPARClite, 323
  - SuperSPARC, 322
  - UltraSPARC-I, 324
  - UltraSPARC-II, 324
  - UltraSPARC-IIi, 325–32
  - UltraSPARC-III, 333
- Spatial locality, 29, 105, 193
- Spatial parallelism, 256
- SPD (serial presence detect), 129, 172
- SPEC (Standard Performance Evaluation Corporation), 23
- SPEC rate, 25
- SPEC ratio, 24
- SPEC89, 23
- SPEC92, 23
- Speculative execution, 164, 166, 253, 258
- Speedup
  - of computer, 27
  - of pipeline, 230
- SRAM (static random-access memory), 113
- SRT (Sweeney, Robertson, Tocher) division, 79–81
- SSM (scalable shared memory) architecture, 333
- STTL\_2 (stub-series terminated logic), 149
- Stack processing, 213
- Stack replacement policy, 213–16
- Stage, of pipeline, 228
- Stall, instruction, 237, 252, 265
- Standard cells, 36
- State diagram, pipeline, 284, 287
- Static address translation, 199
- Static data flow architecture, 7
- Static dependency checking, 238
- Static memory, 111
- Static pipeline, 230, 282
- Static pipeline scheduling, 283–86
- Sticky bit, 101
- Stochastic networks, 11
- Structural hazard, 236
- Structural representation, 34
- Subnormal numbers. *See* Denormal numbers
- Subsystem level. *See* Processor level
- Subtractor

- full, 53
  - half, 53
  - ripple borrow, 102
  - serial, 103
  - Subtraction, 54, 55
    - floating-point, 94–97
    - integer, 53
    - sign-magnitude, 101
  - Subtrahend, 53, 54, 55
  - Sun Microsystems, 321, 333
  - Sun Microsystems products
    - Advanced PCI Bridge (APB) chip, 325
    - JavaStation network computer, 321
    - MAJC processor, 165
    - MAJC-5200 processor, 262, 334–36
    - Sun workstation, 300, 321
    - UltraSPARC-I processor, 324
    - UltraSPARC-II processor, 324
    - UltraSPARC-IIi processor, 325–32
    - UltraSPARC-III processor, 333
    - WorkShop optimizing compilers, 328
  - Superpipeline
    - of MIPS R4000 and R4400 processors, 307
  - Superpipeline processing, 260–61
  - Superscalar architecture, 166
  - Superscalar processing, 256–59
  - Supervised learning, 11
  - Sustained bandwidth, 124, 162
  - Sweeney, Dura W., 79
  - Synapse, 10
  - Synchronous exception, 365
  - Synthesis, 38
    - algorithmic, 40
    - controller, 40
    - data path, 40
    - high-level, 40
    - logic-level, 41
    - register-transfer level, 40
    - system-level, 39, 40
    - technology mapping, 41
  - Synthesizer, 39
  - System CPU time, 13
  - System level, 36
  - System representation, 34
  - System-level synthesis, 39, 40
  - Systolic array, 2, 9, 280–82
  - Systolic matrix multiplier, 280
- ## T
- Tag
    - address, in cache memory, 179, 180, 186, 190
    - memory, cache, 180, 186, 188, 191
  - Technology mapping, 41
  - Temporal locality, 29, 105, 193
  - Texas Instruments, 300, 301, 320, 321
  - Texas Instruments products
    - MicroSPARC processor, 323
    - MicroSPARC-II processor, 323
    - SuperSPARC processor, 322
    - TMS 320C0x0 family of DSP processors, 301
  - Throughput
    - of pipeline, 230, 246, 285
    - of processor, 20
  - Throughput improvement, instruction pipeline, 256–70
  - Tightly coupled multiprocessor, 4
  - TLB. *See* Translation look-aside buffer
  - Tocher, Keith D., 79
  - Tomasulo, R. M., 239
  - Tomasulo's method, 239–41, 258
  - Toshiba, 148, 300, 312
  - Transfer rate. *See* Bandwidth, of memory
  - Transistor level. *See* Circuit level
  - Translation look-aside buffer (TLB), 179, 201, 203, 220, 260
    - of MIPS R2000 processor, 302
    - of MIPS R5000 processor, 317
    - of MIPS R8000 processor, 313
    - of PowerPC 601 processor, 363
    - of PowerPC 750 processor, 375
    - of UltraSPARC architecture, 329
  - Transport delay, 46
  - Turnaround time, 13



TV set-top box, 301

## U

UAL (unit assumed latency) operation, 265

Ultra port architecture (UPA) bus, 329

Underflow, 88, 93

Unit assumed latency (UAL) operation, 265

Unsupervised learning, 11

UPA (ultra port architecture) bus, 325

User CPU time, 13

## V

VCM (virtual channel memory), 142–45, 156

Vector architecture, 167

Vector arithmetic-logic unit, of PowerPC 7400 processor, 378

Vector instruction, 276

Vector IRAM (V-IRAM), 168

Vector processor, 2, 8

Vertical micro-threading, 334

Very long instruction word (VLIW), 261–63, 334

VHDL (VHSIC hardware description language), 42–51

architecture, 44

behavioral description, 43, 45

block statement, 46

characteristics of, 43

component instantiation statement, 47

data flow description, 43, 46

delta delay, 46

entity, 44

inertial delay, 46, 49

model simulation, 50

resolution function, 49

signal assignment, 46

structural description, 43, 47

time model, 48

transport delay, 46, 50

variable assignment, 46

VHSIC (very high speed integrated circuit) project, 42

Via Technologies, 145, 152

Via Technologies products

Apollo Pro 133A chipset, 145

Apollo Pro 266 chipset, 152

KT 133A chipset, 145

KX 133 chipset, 145

V-IRAM (vector IRAM), 168

Virtual address, 199, 206, 216, 217

Virtual Channel Memory (VCM), 142–45, 156

Virtual memory, 198–222

address translation, 199–202

demand-paged, 216, 220

paging, 202–5

paging and segmentation, 206–7

replacement policy, 211–16

segmentation, 205–6

Visual instruction set (VIS), 332

VLIW (very long instruction word), 166, 261–63, 334

Volatile memory, 111, 113

von Neumann architecture, 1, 232

von Neumann bottleneck, 178

VRML (virtual reality modeling language) extensions, 315

## W

Wallace tree multiplier, 67–70

Wallace, C. S., 67

Wallace-tree multiplier, pipelined, 279

WAR (write after read) hazard, 238

WAW (write after write) hazard, 238

Weighted arithmetic mean (of execution times), 21

Weitek, 300

Whetstone, 23

Wooley, B. A., 73

Worst fit memory allocation, 210

Write latency, 154

Write-back algorithm, 142

Write-back policy, 183

Write-through policy, 184, 195

**Y**

Y-chart, 35, 38

**Z**

Zadeh, Lofti, 12



