

# CONTENTS

1. INTRODUCTION.....	1
1.1 I/O SYSTEMS .....	1
1.2 I/O SYSTEM STRUCTURE .....	2
1.3 I/O MODULES.....	3
1.3.1 I/O Module Function .....	3
1.3.2 I/O Module Structure .....	4
1.4 CHAPTER SUMMARY.....	5
1.5 CONCEPTS AND KNOWLEDGE.....	5
REFERENCES.....	6
EXERCISES .....	6
2. METHODS FOR I/O OPERATIONS .....	7
2.1 PROGRAMMED I/O .....	7
2.1.1 Principle of Programmed I/O.....	7
2.1.2 Device Addressing.....	7
2.1.3 I/O Instructions.....	9
2.1.4 Example: Programming Interface for a Keyboard .....	10
2.1.5 Disadvantage of Programmed I/O .....	12
2.2 INTERRUPT-DRIVEN I/O .....	12
2.2.1 Principle of Interrupt-Driven I/O .....	12
2.2.2 Multiple Interrupt Systems.....	14
2.2.3 Priority Interrupt Systems.....	15
2.2.3.1 <i>Parallel Priority Interrupts</i> .....	15
2.2.3.2 <i>Daisy-Chain Priority Interrupts</i> .....	17
2.2.4 Interrupt Service Routines.....	19
2.3 DIRECT MEMORY ACCESS .....	20
2.3.1 Principle of I/O through Direct Memory Access .....	20
2.3.2 Execution of DMA Transfers .....	21
2.3.3 Configurations of Systems Using DMA Transfers .....	23
2.4 I/O PROCESSORS.....	24
2.4.1 Principle of I/O through I/O Processors.....	24
2.4.2 I/O Program Execution .....	25
2.4.3 Intel I/O Processors .....	26
2.5 CHAPTER SUMMARY.....	29
2.6 CONCEPTS AND KNOWLEDGE.....	29
REFERENCES.....	30
EXERCISES .....	31

3. COMPUTER BUSES .....	32
3.1 INTRODUCTION.....	32
3.2 ELECTRICAL CONSIDERATIONS.....	33
3.2.1 Transmission Lines.....	33
3.2.2 Signal Reflections.....	34
3.2.3 Bus Terminations .....	35
3.3 DATA TRANSFER SYNCHRONIZATION .....	37
3.3.1 Synchronous Buses .....	37
3.3.2 Asynchronous Buses.....	39
3.4 PARALLEL AND SERIAL BUSES .....	42
3.5 BUS ARBITRATION.....	43
3.5.1 Centralized Bus Arbitration .....	43
3.5.2 Decentralized Bus Arbitration .....	46
3.6 LOCAL BUSES.....	47
3.7 PCI BUS.....	48
3.7.1 PCI Bus Overview .....	48
3.7.2 PCI Bus Operation .....	51
3.7.2.1 PCI Bus Features.....	51
3.7.2.2 PCI Bus Arbitration.....	52
3.7.2.3 PCI Bus Transactions.....	52
3.7.2.4 PCI Bus Interrupts .....	53
3.7.3 PCI-X Bus.....	54
3.8 PCI EXPRESS BUS.....	55
3.8.1 PCI Express Bus Overview .....	55
3.8.2 PCI Express Bus Architecture.....	57
3.8.2.1 PCI Express Bus Link .....	57
3.8.2.2 PCI Express Bus Topology.....	58
3.8.2.3 PCI Express Bus Architecture Layers.....	60
3.8.2.4 PCI Express Bus Transactions.....	62
3.8.2.5 PCI Express Bus Interrupts.....	62
3.8.3 Versions of the PCI Express Bus Standard .....	63
3.9 I <sup>2</sup> C BUS .....	64
3.9.1 I <sup>2</sup> C Bus Overview.....	64
3.9.2 Data Transfers.....	65
3.9.3 I <sup>2</sup> C Bus Arbitration .....	67
3.9.4 I <sup>2</sup> C Bus Versions .....	67
3.10 SPI BUS.....	68
3.10.1 SPI Bus Overview .....	68
3.10.2 SPI Bus Signals .....	69
3.10.3 Data Transfers.....	71
3.10.4 Clock Polarity and Phase.....	71
3.10.5 Comparison to I <sup>2</sup> C Bus .....	73
3.11 UNIVERSAL SERIAL BUS.....	73

3.11.1 Universal Serial Bus Overview .....	73
3.11.2 Universal Serial Bus Topology.....	74
3.11.3 Universal Serial Bus Versions.....	76
3.11.4 Cables and Connectors .....	78
3.11.5 Universal Serial Bus Transfer Types.....	83
3.12 VME BUS .....	83
3.12.1 VME Bus Overview.....	83
3.12.2 Parallel VME Bus Variants.....	86
3.12.2.1 <i>Original VME Bus</i> .....	86
3.12.2.2 <i>VME64 Bus</i> .....	87
3.12.2.3 <i>VME64x Bus</i> .....	87
3.12.2.4 <i>VME320 Bus</i> .....	87
3.12.3 VXS Bus .....	88
3.12.4 VPX Bus.....	89
3.13 CHAPTER SUMMARY.....	91
3.14 CONCEPTS AND KNOWLEDGE.....	93
REFERENCES.....	94
EXERCISES .....	96
<b>4. EXPANSION MODULES FOR EMBEDDED SYSTEMS .....</b>	<b>98</b>
4.1 REQUIREMENTS FOR EMBEDDED SYSTEMS .....	98
4.2 EXPANSION MODULES BASED ON THE VME BUS .....	99
4.2.1 VME Modules .....	99
4.2.2 VXS Modules.....	101
4.2.3 VPX Modules.....	104
4.2.4 OPENVPX.....	106
4.3 COMPACTPCI MODULES .....	109
4.3.1 CompactPCI Overview .....	109
4.3.2 CompactPCI Extensions .....	112
4.3.2.1 <i>Hot Swap</i> .....	112
4.3.2.2 <i>Computer Telephony</i> .....	113
4.3.2.3 <i>Ethernet Connectivity</i> .....	113
4.3.2.4 <i>PCI eExtensions for Instrumentation</i> .....	113
4.3.2.5 <i>CompactPCI Express</i> .....	115
4.3.2.6 <i>CompactPCI PlusIO</i> .....	117
4.3.2.7 <i>CompactPCI Serial</i> .....	119
4.4 MEZZANINE MODULES .....	122
4.4.1 Introduction.....	122
4.4.2 Previous Mezzanine Modules.....	123
4.4.3 Switched Mezzanine Card.....	125
4.4.4 FPGA Mezzanine Card.....	127
4.5 COM EXPRESS MODULES .....	132
4.5.1 COM Express Overview.....	132
4.5.2 Type 10 COM Express Modules .....	134

4.5.3 Type 6 COM Express Modules .....	136
4.5.4 Type 7 COM Express Modules .....	137
4.6 CHAPTER SUMMARY .....	139
4.7 CONCEPTS AND KNOWLEDGE .....	141
REFERENCES .....	142
EXERCISES .....	144
<b>5. COMPUTER DISPLAYS .....</b>	<b>146</b>
5.1 CATHODE RAY TUBE DISPLAYS .....	146
5.2 LIQUID CRYSTAL DISPLAYS .....	150
5.2.1 Liquid Crystals .....	150
5.2.2 Twisted Nematic Technology .....	153
5.2.2.1 Principle of Operation .....	153
5.2.2.2 Twisted Nematic Liquid Crystal Display Structure .....	157
5.2.2.3 Improved Twisted Nematic Technologies .....	158
5.2.3 Addressing Techniques .....	161
5.2.3.1 Direct and Multiplexed Addressing .....	161
5.2.3.2 Passive-Matrix Displays .....	162
5.2.3.3 Active-Matrix Displays .....	163
5.2.3.4 Defective Pixels .....	168
5.2.4 Backlighting Types .....	171
5.2.5 Liquid Crystal Display Parameters .....	174
5.2.5.1 Response Time .....	175
5.2.5.2 Contrast Ratio .....	179
5.2.5.3 Color Depth .....	182
5.2.5.4 Color Gamut .....	183
5.2.5.5 Viewing Angle .....	191
5.2.6 Vertical Alignment Technology .....	192
5.2.6.1 Principle of Vertical Alignment Technology .....	192
5.2.6.2 Multi-Domain Vertical Alignment Technology .....	193
5.2.6.3 Advanced Multi-Domain Vertical Alignment Technology .....	196
5.2.6.4 Patterned Vertical Alignment Technology .....	198
5.2.7 In-Plane Switching Technology .....	201
5.2.7.1 Principle of In-Plane Switching Technology .....	201
5.2.7.2 Super In-Plane Switching Technology .....	204
5.2.7.3 Horizontal In-Plane Switching Technology .....	206
5.2.7.4 Advanced High-Performance In-Plane Switching Technology .....	207
5.2.7.5 Plane to Line Switching Technology .....	208
5.3 PLASMA DISPLAY PANELS .....	209
5.4 FIELD EMISSION DISPLAYS .....	212
5.5 ORGANIC LIGHT EMITTING DIODE DISPLAYS .....	213
5.5.1 Organic Light Emitting Diodes .....	213
5.5.2 Organic Light Emitting Diode Types .....	214
5.5.2.1 Small-Molecule and Polymer Organic Light Emitting Diodes .....	214

5.5.2.2 <i>Fluorescent and Phosphorescent Organic Light Emitting Diodes</i> .....	216
5.5.3 Organic Light Emitting Diode Structure and Operation .....	221
5.5.4 Organic Light Emitting Diode Display Structure.....	223
5.5.5 Passive-Matrix Organic Light Emitting Diode Displays .....	225
5.5.6 Active-Matrix Organic Light Emitting Diode Displays .....	226
5.5.7 Color Generation Techniques .....	229
5.5.8 Manufacturing Technologies .....	232
5.5.8.1 <i>Vacuum Thermal Evaporation</i> .....	233
5.5.8.2 <i>Organic Vapor Phase Deposition</i> .....	234
5.5.8.3 <i>Color Patterning with Shadow Masks</i> .....	235
5.5.8.4 <i>Laser-Based Color Patterning</i> .....	236
5.5.8.5 <i>Spin Coating</i> .....	237
5.5.8.6 <i>Inkjet Printing</i> .....	238
5.5.8.7 <i>Organic Vapor Jet Printing</i> .....	240
5.5.9 Transparent Organic Light Emitting Diode Displays .....	241
5.5.10 Flexible Organic Light Emitting Diode Displays.....	244
5.5.11 Sub-Pixel Layouts for Organic Light Emitting Diode Displays .....	247
5.5.12 Advantages and Disadvantages of OLED Displays .....	250
5.6 ELECTRONIC PAPER DISPLAYS.....	253
5.6.1 Introduction.....	253
5.6.2 Electronic Paper Display Technologies .....	255
5.6.2.1 <i>Electrophoretic Technology</i> .....	255
5.6.2.2 <i>Electrowetting Technology</i> .....	260
5.6.2.3 <i>Interferometric Modulator Technology</i> .....	263
5.6.3 Color Technologies .....	268
5.6.3.1 <i>Color Electrophoretic Technologies</i> .....	268
5.6.3.2 <i>Color Electrowetting Technologies</i> .....	272
5.6.3.3 <i>Color Interferometric Modulator Technology</i> .....	273
5.6.4 Applications of Electronic Paper Displays.....	275
5.7 QUANTUM DOT DISPLAYS .....	283
5.7.1 Quantum Dots .....	283
5.7.2 Quantum Dot Technologies Used in LCD Panels .....	286
5.7.3 Quantum Dot on OLED Technology.....	289
5.7.4 Quantum Dot on MicroLED Technology .....	290
5.7.5 Quantum Dot Electro-Luminescent Technology.....	292
5.8 CHAPTER SUMMARY.....	293
5.9 CONCEPTS AND KNOWLEDGE.....	303
REFERENCES.....	305
EXERCISES .....	311
6. GRAPHICS ADAPTERS.....	315
6.1 STRUCTURE OF A GRAPHICS ADAPTER .....	315
6.2 GRAPHICS MEMORY .....	318
6.2.1 Types of Graphics Memories .....	318

6.2.2 Graphics Double Data Rate 6 Memory .....	319
6.2.3 High Bandwidth Memory.....	322
6.3 GRAPHICS PIPELINE.....	324
6.3.1 Application Stage .....	324
6.3.2 Geometry Processing Stage .....	326
6.3.2.1 Model Transform .....	326
6.3.2.2 View Transform.....	328
6.3.2.3 Lighting .....	328
6.3.2.4 Projection.....	330
6.3.2.5 Clipping .....	330
6.3.2.6 Screen Mapping .....	331
6.3.2.7 Optional Geometry Processing Stages .....	332
6.3.3 Rasterization Stage .....	333
6.3.3.1 Triangle Setup .....	333
6.3.3.2 Triangle Traversal .....	334
6.3.4 Pixel Processing Stage.....	335
6.3.4.1 Pixel Shading.....	335
6.3.4.2 Output Merging .....	339
6.4 GRAPHICS PROCESSING UNIT .....	341
6.4.1 Overview.....	341
6.4.2 Graphics Library Specifications .....	345
6.4.2.1 Microsoft DirectX.....	345
6.4.2.2 Open Graphics Library .....	348
6.4.2.3 Vulkan .....	350
6.4.3 The 2D Graphics Engine .....	353
6.4.4 The 3D Graphics Engine .....	354
6.4.4.1 Graphics Processing Unit Pipeline.....	354
6.4.4.2 Data-Parallel Architecture .....	358
6.4.4.3 Unified Shader Architecture.....	362
6.4.4.4 Memory Architecture.....	364
6.4.5 General-Purpose Computing on Graphics Processing Units.....	366
6.4.5.1 Overview .....	366
6.4.5.2 Compute Unified Device Architecture.....	371
6.4.5.3 Open Computing Language .....	375
6.4.6 NVIDIA Turing TU102 GPU .....	380
6.4.6.1 Overview .....	380
6.4.6.2 Streaming Multiprocessor.....	381
6.4.6.3 GPU Chip Organization .....	382
6.4.6.4 Tensor Cores .....	385
6.4.6.5 Ray Tracing Cores .....	388
6.4.7 Intel Gen11 Processor Graphics.....	393
6.4.7.1 Overview .....	393
6.4.7.2 Intel System-on-Chip Architecture .....	394

6.4.7.3 Intel Gen11 Processor Graphics Architecture.....	395
6.4.7.4 Subslice Architecture.....	397
6.5 DISPLAY INTERFACE .....	398
6.5.1 High-Definition Multimedia Interface.....	398
6.5.1.1 Overview .....	398
6.5.1.2 TMDS Link and Data Encoding.....	401
6.5.1.3 Display Data Channel.....	404
6.5.1.4 Consumer Electronics Control .....	405
6.5.1.5 HDMI Ethernet and Audio Return Channel .....	408
6.5.1.6 Video Formats.....	411
6.5.1.7 Audio Formats.....	413
6.5.1.8 HDMI Versions .....	414
6.5.1.9 Connectors and Cables.....	416
6.5.2 DisplayPort Interface .....	418
6.5.2.1 Overview .....	418
6.5.2.2 Main Link .....	421
6.5.2.3 Auxiliary Channel .....	424
6.5.2.4 DisplayPort Versions .....	426
6.5.2.5 Dual-Mode DisplayPort.....	427
6.5.2.6 Connectors and Cables.....	428
6.5.2.7 Embedded DisplayPort.....	430
6.6 CHAPTER SUMMARY.....	433
6.7 CONCEPTS AND KNOWLEDGE.....	438
REFERENCES.....	440
EXERCISES .....	445
7. OPTICAL DISCS .....	449
7.1 OPTICAL DISC CLASSIFICATION .....	449
7.2 COMPACT DISC .....	452
7.2.1 Short History of Compact Disc .....	452
7.2.2 Compact Disc Physical Medium .....	455
7.2.3 Compact Disc Data Organization and Encoding.....	456
7.2.3.1 Data Recording and Encoding.....	456
7.2.3.2 First Level of Error Correction .....	459
7.2.3.3 Sector Format .....	459
7.2.3.4 Second Level of Error Correction .....	461
7.2.3.5 Sub-Channels .....	462
7.2.3.6 Compact Disc Organization.....	462
7.2.4 Optical Read Assembly .....	463
7.2.5 Compact Disc Types .....	466
7.2.5.1 Compact Disc-Digital Audio .....	466
7.2.5.2 Compact Disc-Digital Audio Variants.....	466
7.2.5.3 Compact Disc Digital Video .....	468
7.2.5.4 Compact Disc Super Video .....	468

7.2.5.5 <i>Super Audio Compact Disc</i> .....	469
7.2.5.6 <i>Compact Disc-Recordable</i> .....	472
7.2.5.7 <i>Compact Disc-Read/Write</i> .....	475
7.3 DVD .....	477
7.3.1 Overview .....	477
7.3.2 DVD-Video .....	480
7.3.3 DVD-Read/Only Memory .....	482
7.3.4 DVD-Recordable .....	483
7.3.5 DVD+Recordable .....	485
7.3.6 DVD-Read/Write .....	488
7.3.7 DVD+ReWritable .....	489
7.4 BLU-RAY DISC .....	491
7.4.1 Overview .....	491
7.4.2 Blu-ray Disc Physical Format .....	495
7.4.2.1 <i>Optical Aberrations and Tolerances</i> .....	495
7.4.2.2 <i>Modulation and Error Correction</i> .....	496
7.4.2.3 <i>Groove System</i> .....	497
7.4.2.4 <i>Dual-Layer Discs</i> .....	500
7.4.3 Blu-ray Disc Recordable and Rewritable .....	500
7.4.3.1 <i>Single-Layer and Dual-Layer Physical Formats</i> .....	500
7.4.3.2 <i>Triple-Layer and Quadruple-Layer Physical Formats</i> .....	501
7.4.3.3 <i>Audio Visual Logical Formats</i> .....	504
7.4.4 Blu-ray Disc-Read/Only Memory .....	507
7.4.4.1 <i>Blu-ray Disc-Read/Only Memory Physical Format</i> .....	507
7.4.4.2 <i>Ultra HD Blu-ray Physical Format</i> .....	507
7.4.4.3 <i>Audio Visual Logical Format</i> .....	509
7.5 CHAPTER SUMMARY .....	517
7.6 CONCEPTS AND KNOWLEDGE .....	525
REFERENCES .....	526
EXERCISES .....	529
ABBREVIATIONS AND ACRONYMS .....	531
INDEX .....	543