

## 6.11.8. PowerPC 850 and 860

### 6.11.8.1. Overview

The PowerPC 850 (Motorola MPC850) is an integrated communications processor comprising a PowerPC core and several peripheral controllers. This processor can be used in a variety of applications, especially in communications and networking products. The MPC850, which includes support for *Universal Serial Bus* (USB), Ethernet and *Asynchronous Transfer Mode* (ATM), was specifically designed for low-cost remote access and telecommunication applications.

In addition to a high-performance embedded PowerPC core, the MPC850 processor integrates many system functions, including a versatile memory controller and a communications processor module (CPM) that uses a specialized, independent RISC processor for communications. This two-processor architecture is more efficient than traditional architectures because the CPM releases the PowerPC core from the task of peripheral control.

The MPC850 processor also contains a 16x16 multiply accumulate controller (MAC). It can execute one operation per clock cycle, operation which is concurrent with other instructions.

The CPM of the MPC850 processor supports up to seven serial channels: one or two serial communication controllers (SCCs), one USB channel, two serial management controllers (SMCs), one inter-integrated controller (I<sup>2</sup>C) port, and one serial peripheral interface (SPI). The SCCs are capable of supporting Ethernet, ATM, HDLC and a number of other protocols, along with a transparent mode of operation. In addition, up to 64 logical HDLC channels are supported on a single SCC.

The PowerPC 860 (Motorola MPC860) processor has similar functions with the MPC850 communications processor, but differs by the size of the cache memories, the size of the TLBs, and the type and number of peripheral controllers. The MPC860 is based on Motorola's MC68360 Quad Integrated Communications Controller (QUICC). The CPU on the MPC860 is a 32-bit PowerPC implementation that incorporates memory management units (MMUs) and instruction and data cache memories. The communications processor module (CPM) from the MC68360 controller has been enhanced by the addition of the I<sup>2</sup>C channel. Digital signal processing (DSP) functionality has been added to the CPM. The memory controller has been enhanced, enabling the MPC860 processor to support any type of memory, including high-performance memories and new types of DRAM memories. A PCMCIA controller supports up to two sockets. A real-time clock has also been integrated.

In the following we present the MPC860 processor in more details.

### 6.11.8.2. Block Diagram

The block diagram of the MPC860 processor is shown in Figure 6.18.

The MPC860 processor integrates a PowerPC core with high-performance, low-power peripherals. It is comprised of three modules that each use the 32-bit in-

ternal bus: the PowerPC core, the system interface unit (SIU), and the communications processor module (CPM).

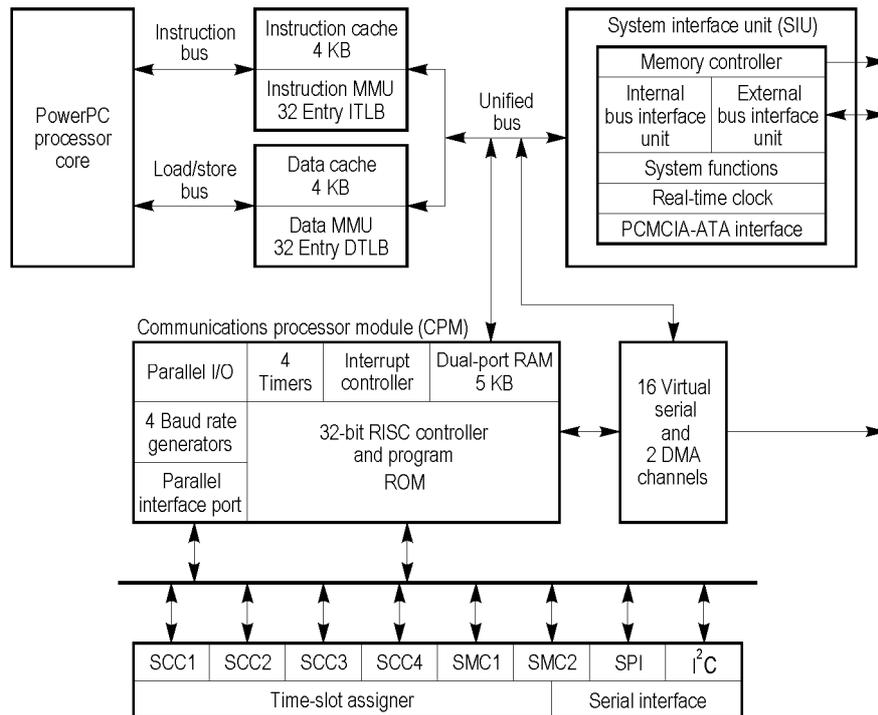


Figure 6.18. Block diagram of the MPC860 processor.

### 6.11.8.3. The PowerPC Core

The PowerPC core is fully static; it contains an integer unit (IU) and a load/store unit (LSU). The core supports integer operations on a 32-bit internal data path. The core interface to the internal and external buses is 32 bits.

The IU uses thirty-two, 32-bit general-purpose registers for source and destination operands. Typically, it can execute one integer instruction in each clock cycle. The clock signal is applied to the elements in the integer unit only when valid data is present in the data queue. This reduces the power consumption of the processor to the minimum required for operation. The core is integrated with MMUs as well as 4-KB instruction and data cache memories. Each MMU contains a 32-entry, fully associative instruction and data TLB, with page sizes of 4 KB, 16 KB, 256 KB, 512 KB, and 8 MB. It supports 16 virtual address spaces.

The instruction and data cache memories are 2-way set associative with physical addressing. They have four words per block, supporting a burst line fill using the LRU replacement algorithm. The cache memories can be locked on a block basis for

critical routines. The data cache memory can be programmed for the copy-back or write-through policy via the MMU.

#### **6.11.8.4. System Interface Unit**

The system interface unit (SIU) of the MPC860 processor integrates general-purpose features useful in almost any 32-bit processor system. Dynamic bus sizing is supported, which allows 8-bit, 16-bit, and 32-bit peripherals and memory to exist in the 32-bit system bus mode. The SIU also provides power management functions, reset control, periodic interrupt timer, time base and a real-time clock.

The memory controller supports up to eight memory banks with interfaces to DRAM, SRAM, EPROM, flash EPROM, SRDRAM, EDO and other memories, with two-clock access to external SRAM and burst-mode support. The controller provides variable block sizes from 32 KB to 256 MB, and 0–30 wait states for each bank of memory.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined with sizes of 256 KB, 512 KB, 1 MB, 2 MB, 4 MB, 8 MB, 16 MB, 32 MB, or 64 MB for all port sizes.

#### **6.11.8.5. PCMCIA Controller**

The PCMCIA interface is a master controller and is compliant with release 2.1 of the PCMCIA standard. The interface supports up to two independent PCMCIA sockets requiring only external transceivers and buffers. The interface provides 8 memory or I/O windows where each window can be allocated to a particular socket. If only one PCMCIA port is being used, the other PCMCIA port may be used as general-purpose input with interrupt capability.

#### **6.11.8.6. Communications Processor Module**

The communications processor module (CPM) allows the MPC860 processor to be used in communications and networking products. The main components of this module are the following:

- Communications processor (CP);
- Sixteen independent serial DMA (SDMA) controllers;
- Four general-purpose timers.

The CP contains a RISC processor, four serial communication controllers (SCC), four serial management controllers (SMC), one serial peripheral interface (SPI), one I<sup>2</sup>C interface, a dual-port RAM of 5 KB, an interrupt controller, a time-slot assigner (TSA), three parallel ports, a parallel interface port (PIP), four independent baud rate generators, and sixteen serial DMA channels.

The serial communication controllers support many protocols implemented in microcode, such as: Ethernet/IEEE 802.3 (up to 10 Mbps), HDLC/SDLC, HDLC bus (implements a HDLC-based local area network), asynchronous HDLC with point-to-point protocol (PPP), AppleTalk, universal asynchronous receiver transmitter (UART), synchronous UART, serial infrared (IrDA), binary synchronous communication (BISYNC), or a totally transparent mode with optional cyclic redundancy check (CRC).

The time-slot assigner allows SCCs and SMCs to operate in multiplexed and/or non-multiplexed mode. It can be internally connected to six serial channels (four SCCs and two SMCs).

The SDMA controllers provide two general-purpose DMA channels for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The four 16-bit general-purpose timers on the CPM allow the internal cascading of two timers to form a 32-bit timer.

#### **6.11.8.7. Differences between the MPC850 and MPC860 Processors**

The following list outline how the MPC860 processor differs from the MPC850 processor.

- Dual-port RAM is 5 KB in size (8 KB in the MPC850 processor);
- 4 KB of instruction and data cache memories (2-KB of instruction cache memory and 1-KB of data cache memory in the MPC850 processor);
- MMUs with 32-entry TLBs (8 entries in the MPC850 processor);
- 32 external address lines instead of 26 in the MPC850 processor;
- No USB port (one USB port in the MPC850 processor);
- PCMCIA interface with two sockets (only one socket in the MPC850 processor);
- Four SCCs instead of one or two in the MPC850 processor;
- 16 serial DMA channels instead of 14 in the MPC850 processor;
- Parallel interface port (Centronics port) added.

#### **6.11.9. Summary**

The main features of the PowerPC architecture are the following:

##### **RISC Features**

- Large register set;
- Load/store architecture;
- Hardwired instruction decoding;

- Single-cycle execution, or superscalar execution.

#### Non-RISC Features

- Multiple addressing modes.

## 6.12. Problems

- 6.12.1.** What are the main differences between RISC and CISC architectures? Considering cost and technology, which design is more advantageous? Justify your answer.
- 6.12.2.** Compare the Harvard architecture with a single-cache architecture. What are the advantages and disadvantages of having two separate cache memories (one for data and one for instructions) instead of having a single larger cache memory (for data and instructions)?
- 6.12.3.** What are the main advantages of an on-chip cache memory compared to an off-chip cache memory?
- 6.12.4.** Choose between the following two design strategies. The first is to have a large set of registers and a small cache memory on the processor's chip and the other to have a small set of registers and a large cache memory. Justify your answer.
- 6.12.5.** Considering cost and performance, what properties of RISC and CISC architectures should be adapted in a hybrid architecture that involves a combination of RISC and CISC?
- 6.12.6.** In a superscalar design, it is possible for instructions to complete execution out of program order. Describe some of the techniques that have been used by the processors to ensure in-order execution completion of instructions. The answer should be based on the processors that were presented in this chapter.
- 6.12.7.** In a superscalar design, one problem that should be addressed is represented by the data hazards. Describe techniques that have been employed in different architectures to avoid the data hazard problem.
- 6.12.8.** Describe the function and structure of the following units: (a) Superpipeline in the MIPS R4000 series; (b) Graphics unit in the UltraSPARC architecture; (c) Memory reference unit in the Alpha 21264 architecture; (d) Instruction unit in the PowerPC 750 processor; (e) Communications processor module in the PowerPC 850 processor.



## A

AltiVec technology, 382  
AMD products  
  29000 family processors, 301  
ANDES (architecture with  
  nonsequential dynamic execution  
  scheduling), 314  
Apple Computer, 364  
ARM (advanced RISC machine), 301  
Asynchronous exception, 370  
AT&T, 302, 303  
AT&T products  
  92010 processor, 301  
  DSP32C DSP processor, 302  
ATM (asynchronous transfer mode),  
  301, 385

## B

BiCMOS (Bipolar-CMOS) technology,  
  307  
Block address translation (BAT) array,  
  368, 371, 372, 374  
Branch following, 330  
Branch history table (BHT)  
  of PowerPC 750 processor, 377  
Branch prediction  
  in Alpha 21064A processor, 344  
  in Alpha 21264 processor, 356–57  
  in MIPS R10000 processor, 315  
  in PowerPC 750 processor, 376  
  in UltraSPARC architecture, 330

## C

Cache memory  
  of Alpha 21064A processor, 344  
  of Alpha 21164 processor, 352  
  of Alpha 21264 processor, 361  
  of MIPS R10000 processor, 316  
  of MIPS R5000 processor, 319  
  of MIPS R8000 processor, 316  
  of MIPS-III architecture, 312  
  of PowerPC 601 processor, 368  
  of PowerPC 750 processor, 381  
  of UltraSPARC architecture, 333

CISC (complex instruction set computer)  
  architecture, 293  
Compaq Computer Corporation, 340  
Compaq Computer products  
  Alpha 21064 processor, 341  
  Alpha 21064A processor, 341–46  
  Alpha 21066 processor, 347  
  Alpha 21066A processor, 347  
  Alpha 21068 processor, 347  
  Alpha 21164 processor, 348–53  
  Alpha 21264 processor, 353–63  
Complex instruction set computer  
  (CISC) architecture, 293  
Current window pointer (CWP), 297  
CWP (current window pointer), 322  
Cypress Semiconductor, 323

## D

Data translation buffer (DTB)  
  of 21064A processor, 345  
  of Alpha 21064A processor, 344  
  of Alpha 21164 processor, 348, 351  
  of Alpha 21264 processor, 362  
Digital Equipment Corporation  
  (DEC), 340  
DSP (digital signal processing), 302  
DTB. *See* Data translation buffer

## E

ECC (error correction code), 312, 327,  
  353  
ECL (emitter coupled logic)  
  technology, 307  
Embedded processor, 301  
Error correction code (ECC), 312, 327,  
  353  
Exception  
  asynchronous, 370  
  imprecise, 370  
  in Alpha 21264 processor, 359  
  in MIPS architecture, 313  
  in PowerPC architecture, 369  
  precise, 304, 313, 370  
  synchronous, 370

**F**

Floating-point unit  
 of Alpha 21264 processor, 360  
 of MIPS R10000 processor, 316  
 of MIPS R4400 processor, 311  
 of MIPS R8010 coprocessor, 316  
 of PowerPC 601 processor, 366  
 of PowerPC 750 processor, 379  
 of UltraSPARC architecture, 331

Forwarding, 324

Fujitsu, 300, 322, 323

Fujitsu products  
 SPARClike embedded processor, 301,  
 323, 325

**G**

Graphics unit  
 of UltraSPARC architecture, 334

**H**

Harvard Mark I computer, 296

Harvard-based architecture, 296

HDTV (high-definition television),  
 301

Hennessy, John, 300

**I**

IBM (International Business Machine),  
 300, 364

IBM products  
 801 minicomputer, 300  
 AS/400 computers, 364  
 PC/RT computer, 300  
 RIOS processor, 364  
 RS/6000 computers, 364

Imprecise exception, 370

Inmos transputer, 300

Instruction translation buffer (ITB)  
 of Alpha 21064A processor, 345  
 of Alpha 21164 processor, 348, 350  
 of Alpha 21264 processor, 358

Integrated Device Technology (IDT),  
 300

Intel products  
 i860 RISC processor, 301

i960 RISC processor, 301

Intel Architecture processors, 301

iWarp processor, 300

ITB. *See* Instruction translation buffer

**L**

Load/store architecture, 298, 299, 307

LSI Logic, 300, 323

**M**

MAJC (microprocessor architecture  
 for Java computing), 337

Memory management  
 in PowerPC 601 processor, 368  
 in the MIPS architecture, 312

Memory management unit (MMU)  
 of MIPS R4400 processor, 305  
 of PowerPC 750 processor, 380  
 of PowerPC 860 processor, 386  
 of UltraSPARC-III processor, 331

MERSI cache-coherence protocol, 383

MIPS (microprocessor without  
 interlocking pipe stages), 300, 302

MIPS Computer Systems, 302

MIPS Computer Systems products  
 R10000 processor, 313  
 R2000 processor, 303  
 R3000 processor, 303  
 R3001 controller, 304  
 R3500 processor, 304  
 R4000 processor, 304  
 R4300i processor, 304  
 R4400 processor, 305  
 R4600 processor, 306  
 R4650 processor, 306  
 R4700 processor, 307  
 R5000 processor, 317  
 R8000 processor, 313–17

MIPS Technology, 302, 313

Motion video instructions (MVI)  
 extension, 348, 354

Motorola, 302, 364

Motorola products  
 5600x DSP processor, 302  
 88000 series processors, 301  
 9600x DSP processor, 302

- MC98601 processor, 364
  - MPC7400 processor, 382–84
  - MPC850 processor, 385–88
  - MPC860 processor, 385–88
- N**
- NEC Corporation, 300, 303, 313
  - NEC products
    - V-800 processor, 301
    - VR10000 processor, 313
  - non-uniform memory access (NUMA) architecture, 336
  - NUMA (non-uniform memory access) architecture, 336
- O**
- Out-of-order execution, 313
  - Overlapping register windows, 297
- P**
- PALcode (privileged architecture library), of Alpha processors, 345
  - Palmtop computer, 301
  - Patterson, David A., 296, 300
  - PDA (personal digital assistant), 301, 370
  - Philips, 300
  - Pipeline
    - of MIPS processors, 307
    - of UltraSPARC architecture, 330
  - Pipelined
    - ALU, of MIPS R5000 processor, 318
    - write operations, in the MIPS R5000 processor, 320
  - POWER (performance optimized with enhanced RISC) architecture, 364
  - PowerPC processors
    - 601, 364–70
    - 602, 370–71
    - 603 and 603e, 371–72
    - 604 and 604e, 372–73
    - 740 and 750, 373–82
    - 7400, 382–84
    - 850 and 860, 385–88
  - Precise exception, 304, 370
- R**
- RAID (redundant array of inexpensive disks), 301
  - Reduced instruction set computer (RISC) architecture, 293
  - Register renaming, 358
  - RISC (reduced instruction set computer) architecture, 293
    - advantages of, 294–96
    - applications of, 300–302
    - characteristics of, 298–99
    - VLSI implementation, 295
    - vs. CISC architecture, 299
  - RISC processors, 302–89
  - Ross Technology, 323, 324
  - Ross Technology products
    - HyperSPARC processor, 324
  - RTOS (real-time operating system), 310
- S**
- Scalable shared memory (SSM) architecture, 336
  - Sequin, C., 296
  - Siemens, 300
  - Silicon Graphics, Inc. (SGI), 302
  - Sony, 300, 303
  - SPARC (scalable processor architecture), 300, 322
  - SPARC Compliance Definition (SCD), 323
  - SPARC International, 322
  - SPARC processors
    - HyperSPARC, 324
    - MicroSPARC, 325
    - MicroSPARC-II, 325
    - SPARClite, 325
    - SuperSPARC, 324
    - UltraSPARC-I, 326
    - UltraSPARC-II, 327
    - UltraSPARC-IIi, 327–36
    - UltraSPARC-III, 336
  - SSM (scalable shared memory) architecture, 336
  - Sun Microsystems, 323, 337
  - Sun Microsystems products

Advanced PCI Bridge (APB) chip, 328  
JavaStation network computer, 323  
MAJC-5200 processor, 337–39  
Sun workstation, 300, 323  
UltraSPARC-I processor, 326  
UltraSPARC-II processor, 327  
UltraSPARC-IIi processor, 327–36  
UltraSPARC-III processor, 336  
WorkShop optimizing compilers, 330  
Superpipeline  
  of MIPS R4000 and R4400 processors, 308  
Synchronous exception, 370

### T

Texas Instruments, 300, 302, 322, 323  
Texas Instruments products  
  MicroSPARC processor, 325  
  MicroSPARC-II processor, 325  
  SuperSPARC processor, 324  
  TMS 320C0x0 family of DSP processors, 302  
TLB. *See* Translation look-aside buffer  
Toshiba, 300, 313  
Translation look-aside buffer (TLB)  
  of MIPS R2000 processor, 303

  of MIPS R5000 processor, 319  
  of MIPS R8000 processor, 314  
  of PowerPC 601 processor, 368  
  of PowerPC 750 processor, 380  
  of UltraSPARC architecture, 332  
TV set-top box, 301

### U

Ultra port architecture (UPA) bus, 332  
UPA (ultra port architecture) bus, 327

### V

Vector arithmetic-logic unit, of  
  PowerPC 7400 processor, 384  
Vertical micro-threading, 337  
Very long instruction word (VLIW), 337  
Visual instruction set (VIS), 335  
VLIW (very long instruction word), 337  
VRML (virtual reality modeling language) extensions, 317

### W

Weitek, 300