Contents of the Lecture

1. Introduction
2. Methods for I/O Operations
3. Buses
4. Liquid Crystal Displays
5. Other Types of Displays
6. Graphics Adapters
7. Optical Discs
3. Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Bus Arbitration
- VME Bus
- Local Buses
- PCI Bus
- PCI Bus Variants
- Serial Buses
Buses: electrical pathways for transmission of signals between various modules of a computer system

Computer systems have several different buses:

- A system bus for connecting the CPU to the memory
- One or more I/O buses for connecting the peripheral devices to the CPU
Buses in a computer system
Dual-Bus Architectures DIB (*Dual Independent Bus*)

The system bus is replaced with two buses: 
- **FSB** (Front Side Bus): between the CPU and main memory 
- **BSB** (Back Side Bus): between the CPU and the level-2 (or level-3) cache memory
Certain devices connected to the bus are active and may initiate a transfer → master

Other devices are passive and wait for transfer requests → slave

Example: The CPU requests a disk controller to read or write a data block

The CPU is acting as a master

The controller is acting as a slave
3. Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Bus Arbitration
- VME Bus
- Local Buses
- PCI Bus
- PCI Bus Variants
- Serial Buses
Electrical Considerations (1)

Designing high-performance buses requires to minimize several undesirable electrical phenomena

- Cause the decrease of systems’ reliability
- The most important: *signal reflections*

Signal reflections are the result of impedance discontinuities: connectors, capacitive loads, device inputs, board layer changes
Signal reflections have the effect of voltage and current oscillations.

To eliminate signal reflections, bus termination must be used.

Termination:
- Passive (resistive)
- Active

Resistive terminators can be connected in series or in parallel.
Series termination

In the ideal case:

\[ R_s + Z_s = Z_0 \]

- \( Z_s \) – source impedance
- \( Z_0 \) – line impedance
Parallel termination

A resistor is placed at the receiving end $\rightarrow$ split resistor network

The equivalent resistance $R_e$ should equal the line impedance $Z_0$

May be used for bidirectional buses
3. Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Bus Arbitration
- VME Bus
- Local Buses
- PCI Bus
- PCI Bus Variants
- Serial Buses
Data Transfer Synchronization

- Synchronous Buses
- Asynchronous Buses
Data Transfer Synchronization

Depending on the synchronization of data transfers, buses can be divided into:

- Synchronous
- Asynchronous

Operations of **synchronous** buses are controlled by a clock signal → require an integral number of clock periods

**Asynchronous** buses do not use a clock signal → bus cycles can have any duration
Data Transfer Synchronization

- Synchronous Buses
- Asynchronous Buses
Synchronous Buses (1)

- Each word is transferred during an integral number of clock cycles.
- This duration is known to both the source and destination units → synchronization

**Synchronization:**
- Connecting both units to a *common clock signal* → short distances
- Using *separate clock signals* for each unit → synchronization signals must be transmitted periodically
Synchronous Buses (2)

Synchronous transfer – Read
Synchronous Buses (3)

Synchronous transfer – Write
The requirement that the *slave* unit responds in the next clock cycle can be eliminated.

An additional control signal *ACK* or *WAIT* is provided, controlled by the *slave* unit.

The signal is only asserted when the *slave* unit has completed its data transfer.

The *master* unit waits until it receives the *ACK* or *WAIT* signal → *wait states* are inserted.
Disadvantages of synchronous buses:

- If a transfer is completed before an integral number of cycles, the units have to wait until the end of the cycle.
- The speed has to be chosen according to the slowest device.
- After choosing a bus cycle, it is difficult to take advantage of future technological improvements.
Data Transfer Synchronization

- Synchronous Buses
- Asynchronous Buses
Asynchronous Buses (1)

An asynchronous bus eliminates the disadvantages of synchronous buses. Instead of the clock signal, additional control signals are used, and a logical protocol between the units (source, destination)

The protocol may be:
- **Unidirectional** – the synchronization signals are generated by one of the two units
- **Bidirectional** – both units generate synchronization signals
Asynchronous Buses (2)

Transfer through unidirectional protocol
(a) Source-initiated transfer
   DREADY (Data Ready)
(b) Destination-initiated transfer
   DREQ (Data Request)
Asynchronous Buses (3)

- The *DREADY* and *DREQ* signals can be used to:
  - Transfer the data from the source unit to the bus
  - Load the data from the bus by the destination unit

- **Strobe signals**

**Example:** The source unit generates a data word asynchronously and places it in a buffer register
The **DREQ** signal enables the clock input of the buffer.
The unidirectional protocol does not allow to verify that the transfer has been completed successfully.

**Example:** In a source-initiated transfer, the source does not have a confirmation of data reception by the destination.

**Solution:** introducing an **acknowledge** signal $ACK \rightarrow$ bidirectional protocol
(a) Source-initiated transfer through bidirectional protocol
(b) Destination-initiated transfer through bidirectional protocol
Asynchronous Buses (8)

Memory read operation using an asynchronous protocol
Asynchronous Buses (9)

**MSYN** *(Master Synchronization)*

**SSYN** *(Slave Synchronization)*

Fully interlocked protocol *(full handshake)*: each action is conditioned by a previous action
3. Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Bus Arbitration
- VME Bus
- Local Buses
- PCI Bus
- PCI Bus Variants
- Serial Buses
Bus Arbitration

- Centralized Arbitration
- Decentralized Arbitration
Bus Arbitration

Has the task to determine the module that will become *master* in case of simultaneous requests

Arbitration methods
- **Centralized**: bus allocation is performed by a bus arbiter
- **Decentralized (distributed)**: there is no bus arbiter
Bus Arbitration

- Centralized Arbitration
- Decentralized Arbitration
Centralized Arbitration (1)

Methods for centralized arbitration:

- Daisy chaining of devices
- Independent requesting
- Polling

Centralized arbitration in which daisy chaining of devices is used

- A single bus request line, $BUSREQ$ ($Bus Request$) $\rightarrow$ wired OR
- A bus grant line $BUSGNT$ ($Bus Grant$)
The device physically closest to the arbiter detects the signal on the *BUSGNT* line.
Centralized Arbitration (3)

- Only two control lines are required for bus arbitration.
- Device priority is fixed → given by the chaining order on the BUSGNT line.
- To modify the default priorities, buses may have multiple priority levels.
- For each priority level, there is a bus request line and a bus grant line.
Centralized Arbitration (4)

Each device attaches to one of the bus request lines, according to the device priority.
C
entralized Arbitration (5)

- Daisy chaining – Advantages:
  - Small number of control lines required
  - The possibility to connect, theoretically, an unlimited number of devices

- Daisy chaining – Disadvantages:
  - Fixed priorities of the devices
  - A high-priority device may lock out a low-priority device
  - Susceptibility to failures of the BUSGNT line
Centralized Arbitration (6)

Centralized arbitration by independent requesting

- There are separate $BUSREQ$ and $BUSGNT$ lines for every device
- The arbiter may immediately identify all devices requesting the bus and may determine their priority
- Priority of requests is programmable
- Disadvantage: to control $n$ devices, $2n$ $BUSREQ$ and $BUSGNT$ lines must be connected to the bus arbiter
Centralized arbitration by polling

- The *BUSGNT* line is replaced with a set of poll-count lines
- Devices request access to the bus via a common *BUSREQ* line
- The bus arbiter generates a sequence of addresses on the poll-count lines
- Each device compares these addresses to a unique address assigned to that device
- On a match, the device asserts the *BUSY* signal and connects to the bus
Centralized Arbitration (8)

Poll-count lines
Bus arbiter

BUSREQ
BUSY

D₁  D₂  ...  Dₙ
Centralized Arbitration (9)

The priority of a device is determined by the position of its address in the polling sequence.

Advantage: the sequence can be programmed if the poll-count lines are connected to a programmable register.

Another advantage: a failure in one device does not affect other devices.

These advantages are achieved at the cost of more control lines.
Bus Arbitration

- Centralized Arbitration
- Decentralized Arbitration
Decentralized Arbitration (1)

There is no bus arbiter

**Example** of decentralized arbitration

- $n$ prioritized bus request lines $\rightarrow n$ devices
- To use the bus, a device asserts its request line
- All devices monitor all the request lines

**Disadvantages**: more bus lines required; the number of devices is limited
Example of decentralized arbitration with only three lines

- **BUSREQ** → wired OR
- **BUSY** → asserted by the bus master
- Bus arbitration → daisy chained
- The method is similar to the daisy-chain arbitration, but without an arbiter

**Advantages**: lower cost; higher speed; not subject to arbiter failure
Decentralized Arbitration (3)
3. Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Bus Arbitration
- VME Bus
- Local Buses
- PCI Bus
- PCI Bus Variants
- Serial Buses
VME Bus

Overview
Parallel VME Bus Variants
Modules and Connectors
VXS Bus
Serial VME Bus
Overview (1)

- VME (Versa Module Eurocard)
- Originates from VERSAbus (Motorola)
- VERSAbus has been adapted for the double Eurocard form factor (6U, 267×160 mm)
  - VMEbus, rev. A
- The VME specifications have been updated (revisions B, C, C.1)
- IEC, IEEE, and ANSI/VITA standards
Asynchronous bus

- Allows various components to operate at a speed appropriate to the technology used

Used for industrial applications and embedded systems

There are no license fees

The reliability of the bus is ensured by:

- Mechanical design → connectors with metallic pins
- Logical protocol
Overview (3)

Applications:
- Industrial control
- Military: radars, communications, avionics
- Aerospace
- Railway transportation
- Telecommunications: cellular telephone base stations, telephone switches
- Medical: nuclear magnetic resonance imaging
- Various: high-energy physics, nuclear physics
Family of three buses

**VME: main bus**
- Bus for memory extension
- Allows to increase performance by reducing the overall traffic on the main VME bus

**VSB: secondary bus**

**VMS: serial bus**
- Used for communication and synchronization between multiple processors
(a) Minimal system; (b) Multiprocessor system
VME Bus

VME Bus

Overview

Parallel VME Bus Variants

Modules and Connectors

VXS Bus

Serial VME Bus
Parallel VME Bus Variants (1)

Original VME Bus

- Non-multiplexed data and address lines
- Data size: 8 .. 32 bits
- Address size: 16 .. 32 bits
- Multiprocessing capability: M/S architecture
- Centralized arbitration by daisy-chaining
- A number of 7 interrupt request lines
- Connectors with 96 pins (3 rows x 32)
- Up to 21 expansion boards in a backplane
Parallel VME Bus Variants (2)

VME64 Bus
- 64-bit data (double Eurocard)
- 64-bit addresses (double Eurocard)
- 32-bit or 40-bit addresses (single Eurocard)
- Lower-noise connectors
- “Plug and Play” features → ROM memory

VME64x Bus
- 3.3 V power supply pins
- 141 user-defined I/O pins
Parallel VME Bus Variants (3)

- New connectors with 160 pins (5 rows x 32)
  - Compatible with the 96-pin connectors
- Additional connector with 95 pins (5 x 19)
- Higher bandwidth (up to 160 MB/s)
- Modified protocol for data transfer cycles → 2eVME (*Double-edge* VME)
- The possibility for *insertion of modules during operation* (live-insertion)
- Front panels with guiding pins
Parallel VME Bus Variants (4)

VME320 Bus
- Bandwidths of over 320 MB/s (peak bandwidths of over 500 MB/s)
- Star-interconnection method
  - All of the interconnections are joined together at the middle slot of the backplane
- A new protocol → 2eSST (Double-edge Source Synchronous Transfer)
  - During the data phases, it is a source-synchronous protocol
VME Bus

- Overview
- Parallel VME Bus Variants
- Modules and Connectors
- VXS Bus
- Serial VME Bus
Modules and Connectors (1)

- **VME module sizes**
  - Single-height: 3U x 160 mm (U – unit of measure; 1U = 1.75 inches = 44.45 mm)
  - Double-height: 6U x 160 mm
  - Triple-height: 9U x 400 mm

- **Conduction cooled modules**
  - Used in military and aerospace applications
  - Heat is conducted through the printed circuit board or through a conduction plate
VME backplanes
- Length of 19 inches; 1 .. 21 connectors
- Standard: 3-row connectors
- VME64x: 5-row connectors
- VME320

VME connector types
- P (Plug): reside on the modules (boards)
- J (Jack): reside on the backplane
- P1/J1, P2/J2: 96 or 160 pins
P3/J3: P3 connectors may be included on 9U modules
P0/J0: 95 pins; may be used for high-speed signals
Custom connectors can be placed between the P1/J1 and P2/J2 connectors, e.g., for:
- Coaxial cables
- Fiber-optic cables
VME Bus

- Overview
- Parallel VME Bus Variants
- Modules and Connectors
- VXS Bus
- Serial VME Bus
VXS Bus (1)

**VXS – VMEbus Switched Serial**

ANSI/VITA standard to combine the parallel VME bus with high-speed switched serial interconnects

- ANSI/VITA 41.0: Base specification
- ANSI/VITA 41.1: InfiniBand connector
- ANSI/VITA 41.2: Serial RapidIO connector
- ANSI/VITA 41.3: Gigabit Ethernet connector
- ANSI/VITA 41.4: PCI Express connector (4x)
Switched serial interconnect

Point-to-point connections between modules

Switch boards (1-2): contain an active switch

Regular (payload) boards (up to 18): other boards that connect to the switch boards

Clock and data signals are combined into a single serial bitstream

Data rates of 3.125 or 6.25 Gbits/s

With 8b/10b encoding: 312.5 or 625 MB/s

With 64b/66b encoding: 378 or 756 MB/s
Switch boards

- 6U x 160 mm
- Replace the parallel P1 and P2 connectors with 5 serial connectors (P1 .. P5)
- MultiGig RT connectors
- A1 K1, A2 K2: alignment and keying connectors
- PWR1: power connector
- Can access VME resources via serial-to-VME bridges
Payload boards

- **P1, P2**: VME64x parallel connectors; 5 rows
- **P0**: high-speed serial connector; 7 rows
- **A0 K0**: alignment and keying connector

The **P0** connector provides eight full-duplex serial links (up to 2.5 GB/s or 5 GB/s in each direction)
VXS Backplanes

Maximum configuration: 18 payload boards; 2 switch boards; 1 VME64x board

Single star topology: each payload board connects to a single switch board

Dual star topology: each payload board connects to both switch boards (redundancy)

Mesh topology: each payload board is directly connected to every other board

Up to 3 boards connected without a switch
VXS Bus (6)

VXS topologies: dual star; single star; mesh
VME Bus

- Overview
- Parallel VME Bus Variants
- Modules and Connectors
- VXS Bus
- Serial VME Bus
Serial VME Bus (1)

- VPX
  - Replaces the parallel VME bus with switched serial interconnects
- ANSI/VITA standard 46
  - ANSI/VITA 46.0: Base specification
  - ANSI/VITA 46.1: VMEbus signal mapping
  - ANSI/VITA 46.3: Serial RapidIO connector
  - ANSI/VITA 46.4: PCI Express connector
  - ANSI/VITA 46.6: Gigabit Ethernet connector
Maintains the 3U and 6U Eurocard form factors of the VME specifications

6U hybrid backplanes can also be used to accommodate VME64, VXS, and VPX boards

MultiGig RT2 connectors are used

- Speeds up to 10.3 Gbits/s
- 3U boards: three connectors (P0 .. P2)
- 6U boards: seven connectors (P0 .. P6)
- Up to 160 differential I/O signals
Summary (1)

- **Bus terminators** must be used to eliminate or reduce signal reflections
  - May be connected in series or in parallel
- Although **synchronous buses** have drawbacks, most buses are synchronous
- For **asynchronous buses**, bidirectional protocols are more reliable
- **Bus arbitration methods** can be centralized or decentralized
  - **Centralized arbitration** methods: daisy-chaining, independent requesting, polling
Summary (2)

The **VME bus** is one of the most successful interconnect technologies

- Mechanical, electrical, and software compatibility is ensured with all existing VME boards

The **parallel VME bus** has been improved significantly, but it has reached its limits

The **VXS** bus ensures the transition to high-speed serial interconnects

The **VPX** bus uses only serial interconnects

- It will gradually replace the parallel VME bus
Concepts, Knowledge (1)

- Signal reflections
- Series and parallel termination
- Synchronous buses
- Synchronous transfers
- Disadvantages of synchronous buses
- Asynchronous buses
- Source-initiated transfer, unidirectional
- Destination-initiated transfer, unidirectional
- Source-initiated transfer, bidirectional
- Destination-initiated transfer, bidirectional
Centralized bus arbitration
Centralized arbitration by daisy-chaining
Centralized arbitration by independent requesting
Centralized arbitration by polling
Decentralized bus arbitration
Features of the VME64x bus
Features of the VME320 bus
Features of the VXS technology
Features of the VPX technology
Questions

1. What are the disadvantages of centralized arbitration by daisy-chaining?
2. How does the centralized arbitration by polling work?
3. What are the main features of the VME320 bus?
4. What are the main features of the VXS technology?