The justification process

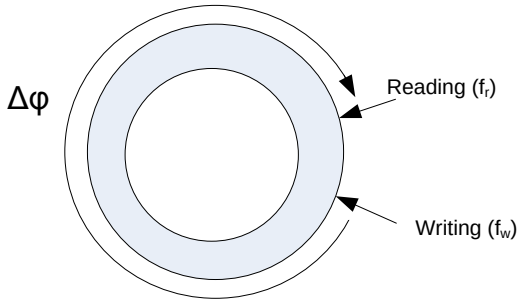

Figure 1 – The elastic memory/buffer

$\Delta\varphi_{\max} = k \cdot 2 \cdot \pi$, where *k* represents the number of memory locations.

We propose to find the justification moments in order to avoid the double readings due to the fact that the reading frequency is larger than the writing frequency, $f_r > f_w$. In order to simplify the analysis we consider the phase range of interest $[\ 2 \cdot \pi \cdot (k-1) \cdot t, 2 \cdot \pi \cdot k \cdot t\ ]$, and the analysis of the justification process could be performed in the range $[\ 0, 2 \cdot \pi\ ]$, and $\Delta\varphi_{\max} = 2 \cdot \pi$.

There are known the following parameters of the secondary PDH frame:

- The secondary PDH multiplex frame
  - 848 bits
    - 824 bits from tributaries
    - 24 control bits
      - 10 synchronization bits
      - 1 alarm bit
      - 1 service bit
      - 12 justification signaling bits (3 x 4 bits)
  - Bit rate = 8448 kbps
- Tributaries
  - Total no. of bits = 848/4=212 bits
  - No. of bits/tributary = 24/4 = 6 bits
  - No. of information bits/tributary = 212 – 6 = 206 bits
  - Bit rate = 8448kbps/4 = 2112kbps
  - Information bit rate = 2112kbps*206/212 = 2052.22641kbps
  - Input bit rate = 2048kbps
- The analysis of the justification process is performed in the following conditions:
  - f_w=2048 kHz
  - frame size: Nc = 206 bits (only information bits)
  - f_r=2052.22641 kHz
  - justification position = 155

In a first step has to be computed a threshold which if it is atained a justification decision is tacken. This is due to the fact that the justification can be done only in some imposed locations in the frame. This thershold has to be computed in such a

way to ensure that the phase diference between the writing and the reading clocks is smaller than the maximum allowed value in the justification moment, $\Delta\varphi_{\max} = 2 \cdot \pi$. The worst case scenario is represented by the situation when the justification decision is tacken right after a possible justification moment, meaning that we have to wait an entire frame perriod in order to realize the justification.

$thr \le 2 \cdot \pi - Nc \cdot \Delta\varphi_b$, where $\Delta\varphi_b$ represents the phase difference between the two clock signals during a bit period

$$\Delta\varphi_b = 2 \cdot \pi \cdot (f_r - f_w) \cdot T_b = \frac{2 \cdot \pi \cdot 4.22641}{2052.22641} = 2 \cdot \pi \cdot 0.002059426$$

$$thr \le 2 \cdot \pi \cdot (1 - 0.424241913) = 2 \cdot \pi \cdot 0.575758086$$

In the following we identify the justification moments (see Figure 2) :

- The first justification decision is tacken in the bit location:

$$n1 = \frac{thr}{\Delta\varphi_b} = \frac{2 \cdot \pi \cdot 0.575758086}{2 \cdot \pi \cdot 0.002059426} = 279.57 \Rightarrow n1 = 280$$

The next justification position is on the bit location 361, and the phase difference in that moment is: $361 \cdot \Delta\varphi_b = 2 \cdot \pi \cdot 0.743452786$, and after justification the phase difference becomes: $361 \cdot \Delta\varphi_b - 2 \cdot \pi = -2 \cdot \pi \cdot 0.256547214$.

- The second justification decision is tacken in bit position:

$$n2 = 361 + \frac{thr + 0.256547214}{\Delta\varphi_b} = 361 + \frac{2 \cdot \pi \cdot 0.8323053}{2 \cdot \pi \cdot 0.002059426} = 765.73 \Rightarrow n2 = 766$$

The next justification position is on the bit location 773. The phase difference in the justification moment is: $(773 - 361) \cdot \Delta\varphi_b - 2 \cdot \pi \cdot 0.256547214 = 2 \cdot \pi \cdot 0.591936298$, and after that becomes: $2 \cdot \pi \cdot 0.591936298 - 2 \cdot \pi = -2 \cdot \pi \cdot 0.408063702$.

- The third justification decision is tacken in bit position:

$$n3 = 773 + \frac{thr + 0.408063702}{\Delta\varphi_b} = 773 + \frac{2 \cdot \pi \cdot 0.983821788}{2 \cdot \pi \cdot 0.002059426} = 1250.71 \Rightarrow n3 = 1251$$

The next justification moment in on bit lacation 1391. The phase difference in the justification moment is: $(1391 - 773) \cdot \Delta\varphi_b - 2 \cdot \pi \cdot 0.408063702 = 2 \cdot \pi \cdot 0.864661566$, and after that becomes $2 \cdot \pi \cdot 0.864661566 - 2 \cdot \pi = -2 \cdot \pi \cdot 0.135338434$.

If we consider that the justification scheme presented in figure 2 is a repetitive one we can compute the average justification frequency as 3 justifications in 7 frames, meaning: $fj_{mean} = \frac{3}{7} \cdot f_{frame} = \frac{3}{7} \cdot \frac{f_r}{206} = \frac{3}{7} \cdot 9.962264126 = 4.269554kHz$

$$Fjitter_{justification} = fj_{mean} = 4.269554kHz$$

$$Fjitter_{waiting} = repetition\_frequency\_of\_the\_justification\_scheme =$$

$$= \frac{f_{frame}}{no.\_frames\_in\_the\_justification\_scheme} = \frac{9.96}{7} = 1.42kHz$$

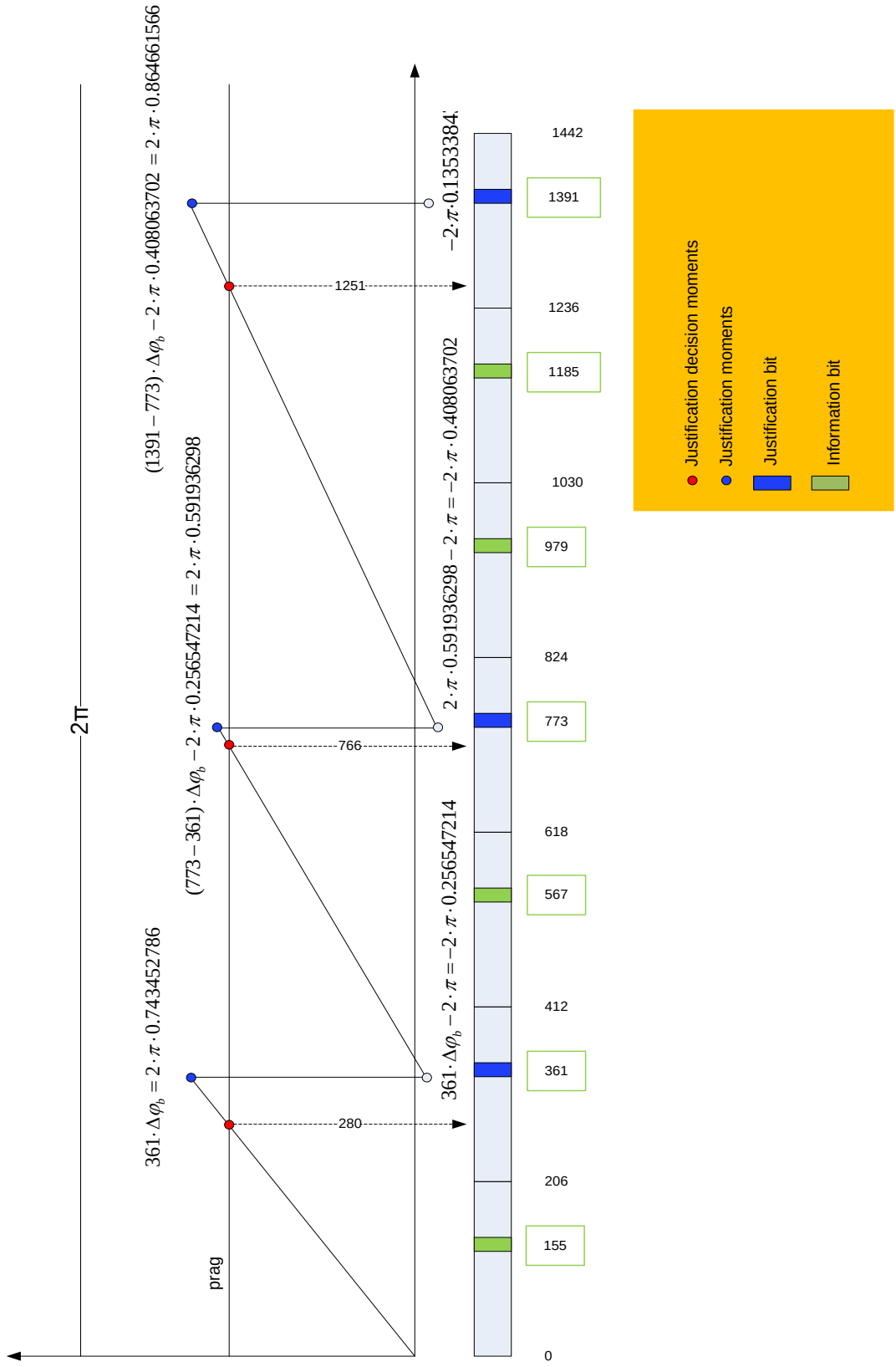

Figure 2 – The justification process

Homework:

- Problems: 30,31,32 / page 160
- Problem 50 / page 161
- Problems; 46,47 / page 161
- Problems: 51,52 / page 161