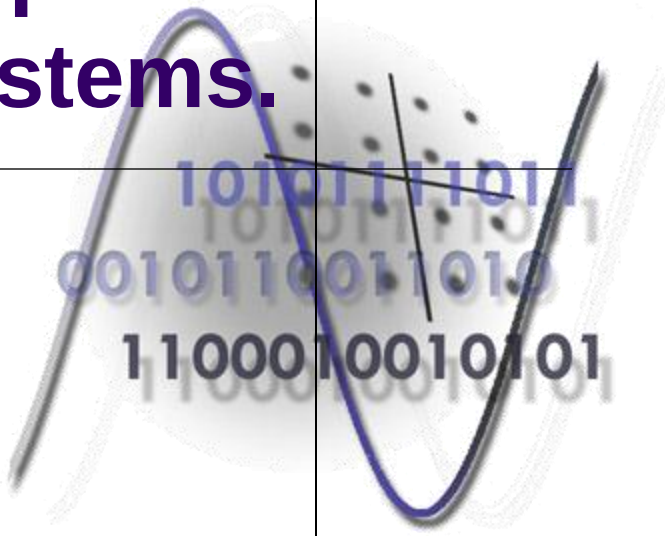
Course 10-11
The PDH multiplexing hierarchy. The digital regenerator. The jitter in digital telephone transmission systems.



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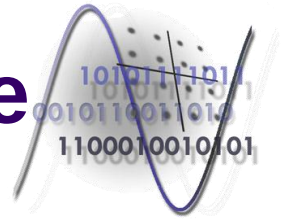
Content of the course

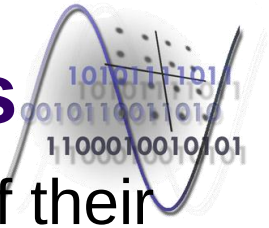


- Multiplexing of plesiochronous signals;
  - Digital signals classification;
  - Rate matching by justification;
  - The principle of positive justification;
  - Justification signaling insertion (multiplexing);
- The PDH multiplexing hierarchy;
  - PDH multiplexing systems;
  - PDH frame formats;
  - Disadvantages of the PDH system.
- The digital regenerator;
  - Characteristics / role;
  - Block schematic;
  - Bit clock recovery.

Content of the course

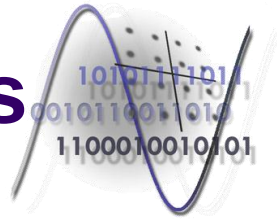
- The jitter in digital transmission systems;
  - Definition / characteristics;
  - The origin of the jitter;
  - Jitter accumulation / jitter compensation;
  - Jitter performances.

Multiplexing of digital signals



- Classification of digital signals from the point of view of their generation and the relation between their clock signals:
  - Isochronous signal:
    - the time interval between two significant moments is theoretically equal with a unitary time interval or with a multiple of this;
  - Anisochronous signals:
    - the time interval separating two significant moments it is not necessarily related to a unitary interval or to a multiple of this;
    - the symbols of a non-isochronous binary signal do not have the same duration.
  - Homochronous signals:
    - isochronous signals with the same rate and constant phase relation;
    - can be divided in:
      - Mesochronous signals – isochronous signals with the same rate and non-constant phase relation – constant average phase relation;
      - Synchronous signals – isochronous signals with the same rate and constant phase relation.

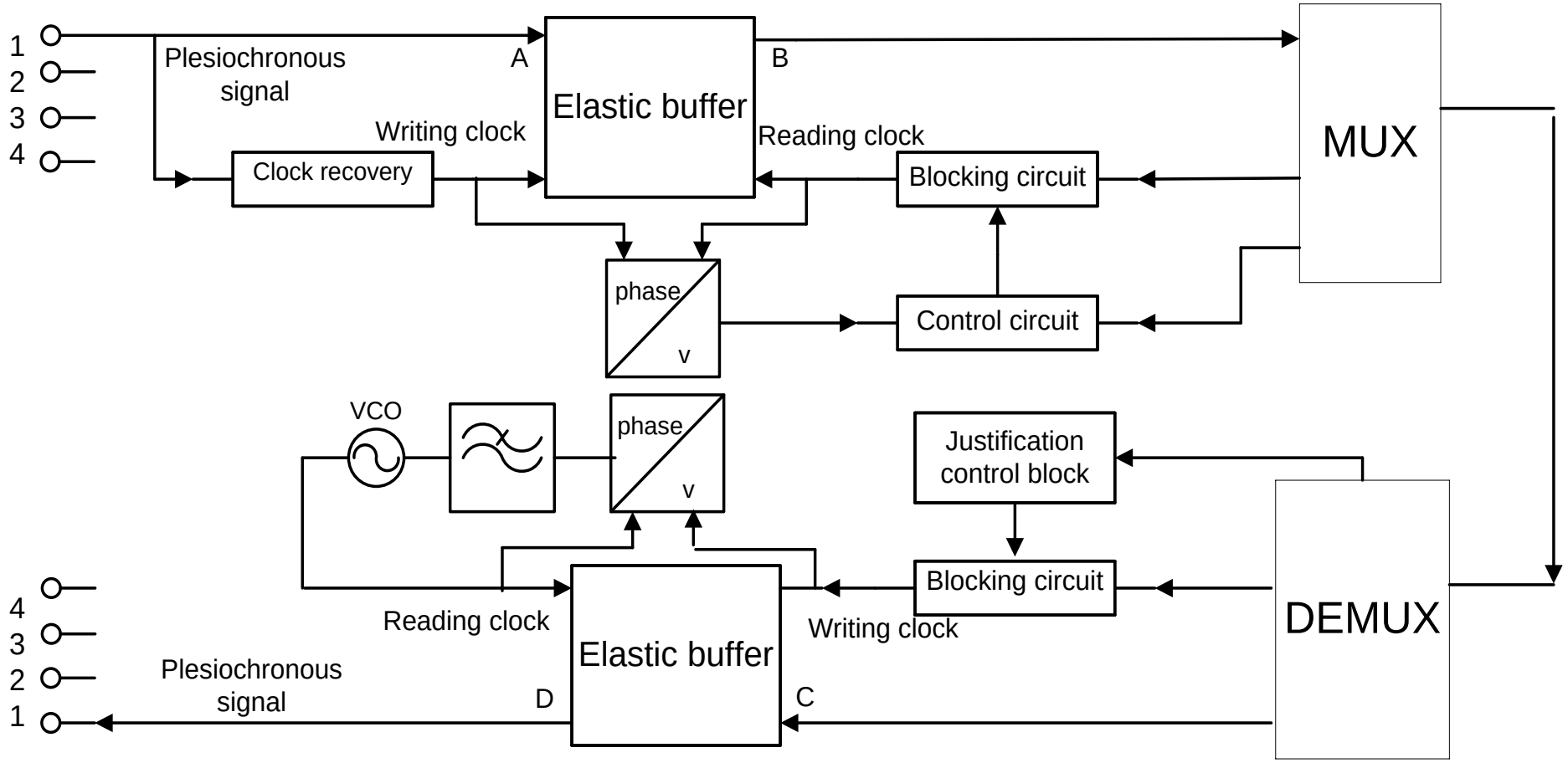
Multiplexing of digital signals



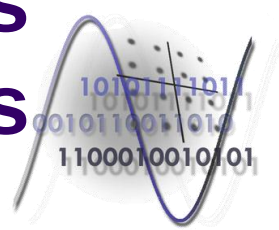
- Heterochronous signals:
  - isochronous signals with different rates and variable phase relation;
  - plesiochronous signals – signals with the same nominal rate, all the variations of this rate being maintained between specified limits;
    - for ex. signals with identical nominal rates from different sources.
- Multiplexing of plesiochronous digital signals
  - Can be realized in two possible ways:
    - generation of signals with high stability of the clock frequency and use of some buffers;
      - very high price and periodical loss of information;
    - use of the justification (stuffing) method;
      - without information loss;

Multiplexing of plesiochronous signals

- Block schematic of PDH multiplexing – demultiplexing equipments;



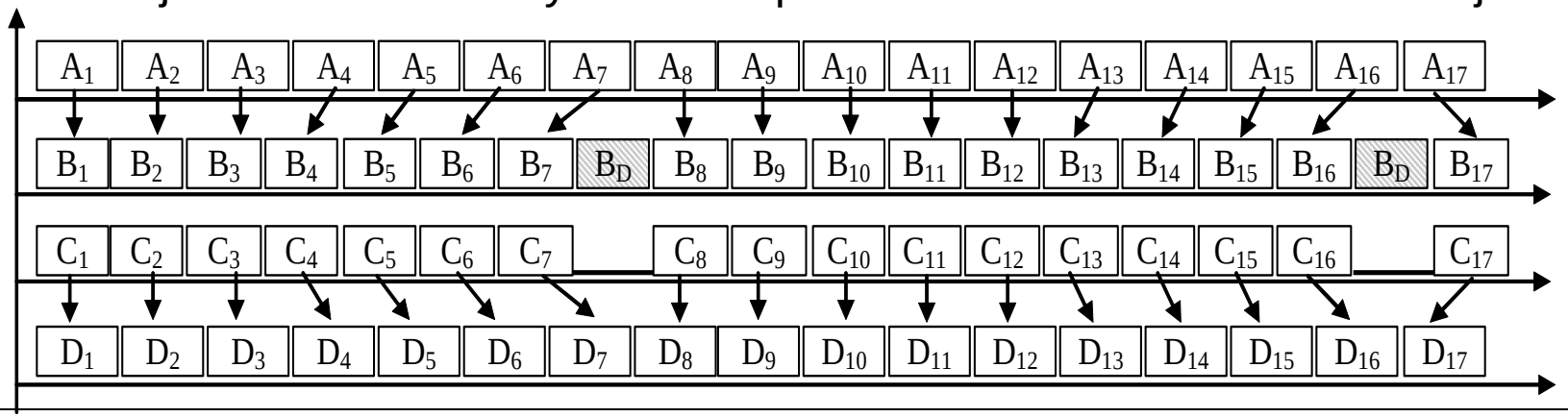
Multiplexing of plesiochronous signals



- Principle of the rate matching between the tributary and multiplexer based on positive justification;
  - The plesiochronous binary signal is written in the elastic memory with a specific clock frequency, f_i;
  - The reading of the memory and the transmission of the signal in the channel is realized with a higher clock frequency $f_o > f_i$;
    - appears a clean out tendency of the elastic memory content;
    - it is detected by using a phase comparator (compares f_o and f_i);
  - When a phase difference threshold value is exceeded (between signals f_o and f_i), the phase comparator generates a blocking commands of the reading impulse;
    - it is created a break in the line signal (one stuffing impulse is inserted) which decreases the phase difference between the clock signals;
      - the stuffing impulse has no information.

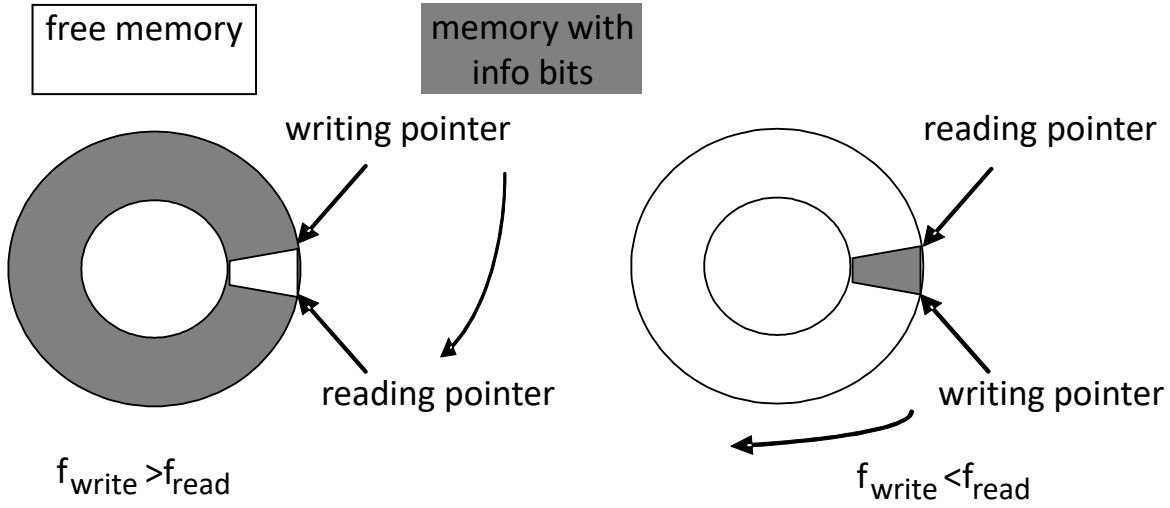
Multiplexing of plesiochronous signals

- The justification (stuffing) is signaled to the reception side on a link multiplexed with the data signal;
  - the signaling of the justification (stuffing) is necessary to inform the receiver about the exact moment and location of the justification (stuffing);
    - this information is necessary for suppression of the justification bits in the receiver;
- Only the information bits are written in the memory at the reception side with a frequency f_o, the memory being read with a frequency f_i;
- The extraction of the justification (stuffing) impulses generates a jitter in the output signal;
  - this jitter is controlled by a PLL loop which reduces the effects of the jitter.



Multiplexing of plesiochronous signals

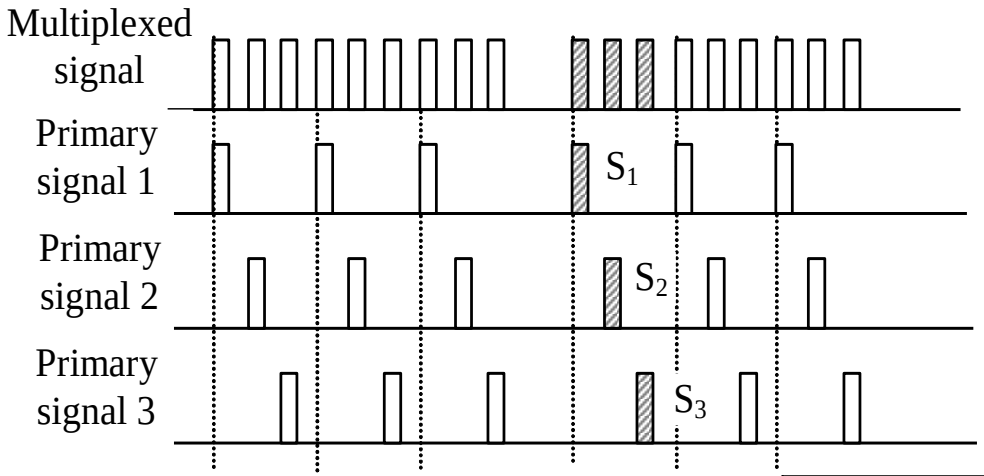
- Use of the elastic buffer for rate adaptation:

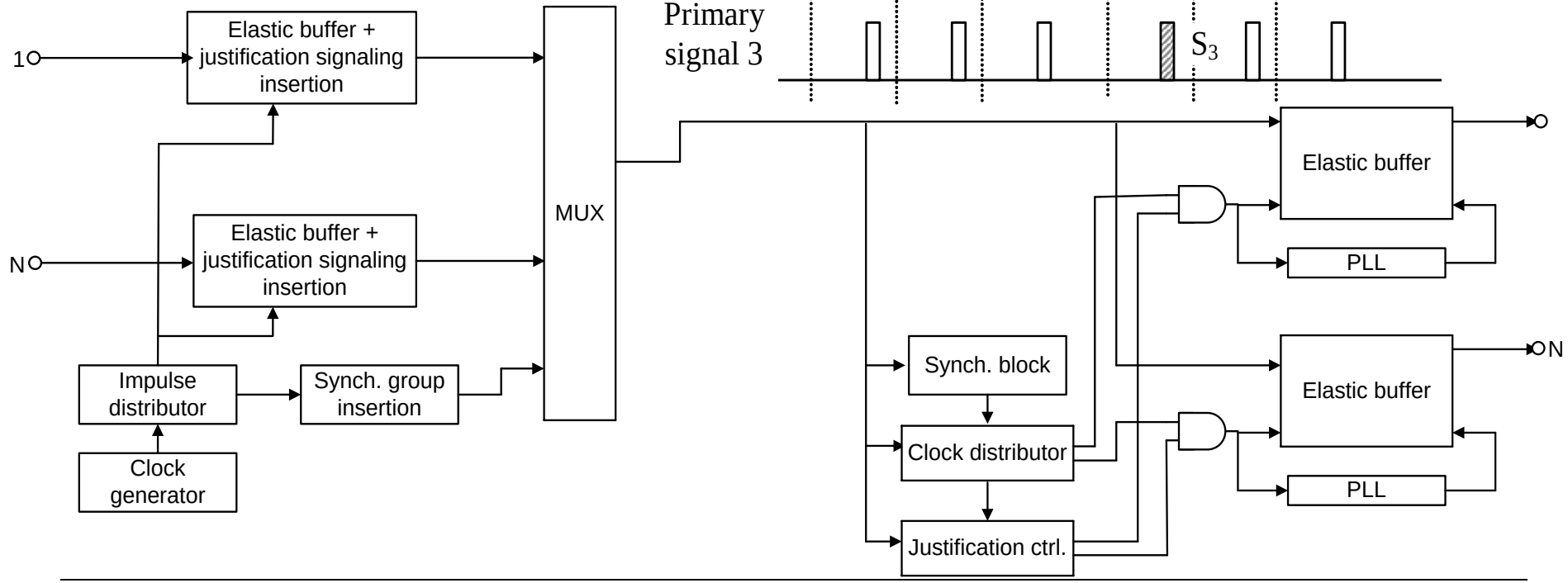


- Justification signaling insertion:
  - Individual insertion;
    - insertion of signaling justification bits is realized before multiplexing;
    - complex method at transmission; flexible and low complexity method at reception;
  - Common insertion;
    - the signaling information from all tributary signals are concentrated on a common path which is then multiplexed with data;
    - lower complexity at transmission, but higher complexity at reception.

Multiplexing of plesiochronous signals

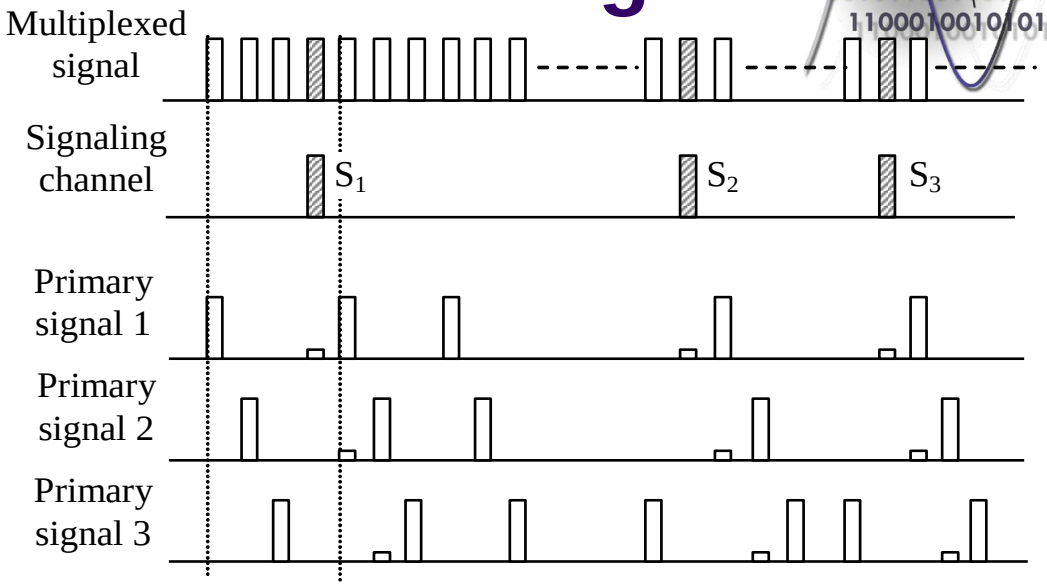
- Individual insertion of the justification signaling;
  - Signal diagram:
  - MUX and DEMUX block schematics:

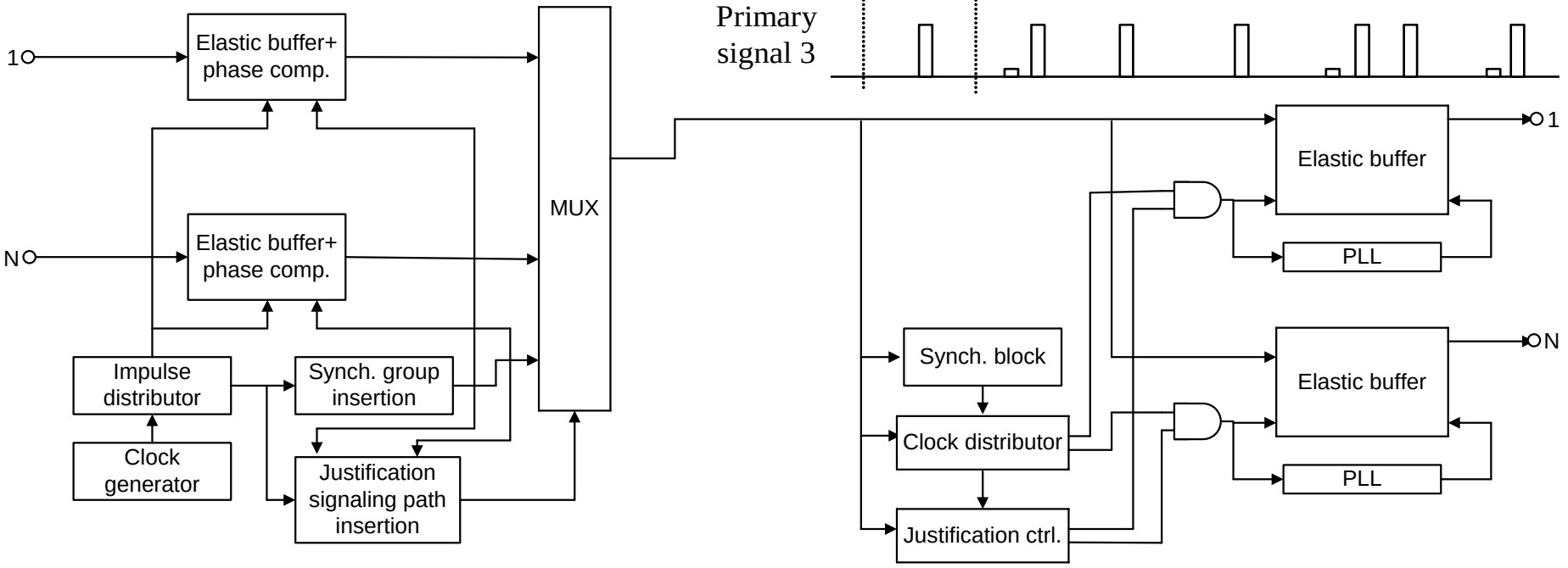




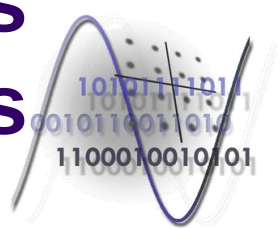
Multiplexing of plesiochronous signals

- Common insertion of the justification signaling;
  - Signal diagram:
  - MUX and DEMUX block schematics:





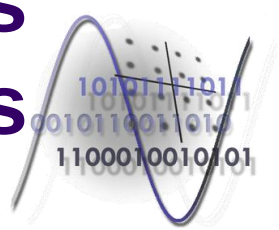
Multiplexing of plesiochronous signals



- The information related to the signaling commands is very important for the functioning of the multiplexing equipments;
  - if this information is erroneous other bits than the justification bits will be extracted from the received signal;
    - this will lead to loss of synchronization;
  - redundant coding of the signaling information and error correction of the signaling bits is used;
    - repetition codes are used usually (these bits are transmitted several times and the correct bits are decided based on a majority logic);
    - for ex. justification signaling: $c_1c_2c_3$ =1 1 1; absence of justification: $c_1c_2c_3$ = 0 0 0;
    - $c_1c_2c_3$ - justification signaling bits for one tributary/source.
- Computation of the justification signaling;
  - N_0 is the total number of symbols of a transmission frame;
  - N_s is the number of synchronization symbols;
  - n_0 is the number of information symbols;
  - η is the frame efficiency.

$$n_0 = N_0 - N_s \; ; \; \eta = \frac{n_0}{N_0}$$

Multiplexing of plesiochronous signals

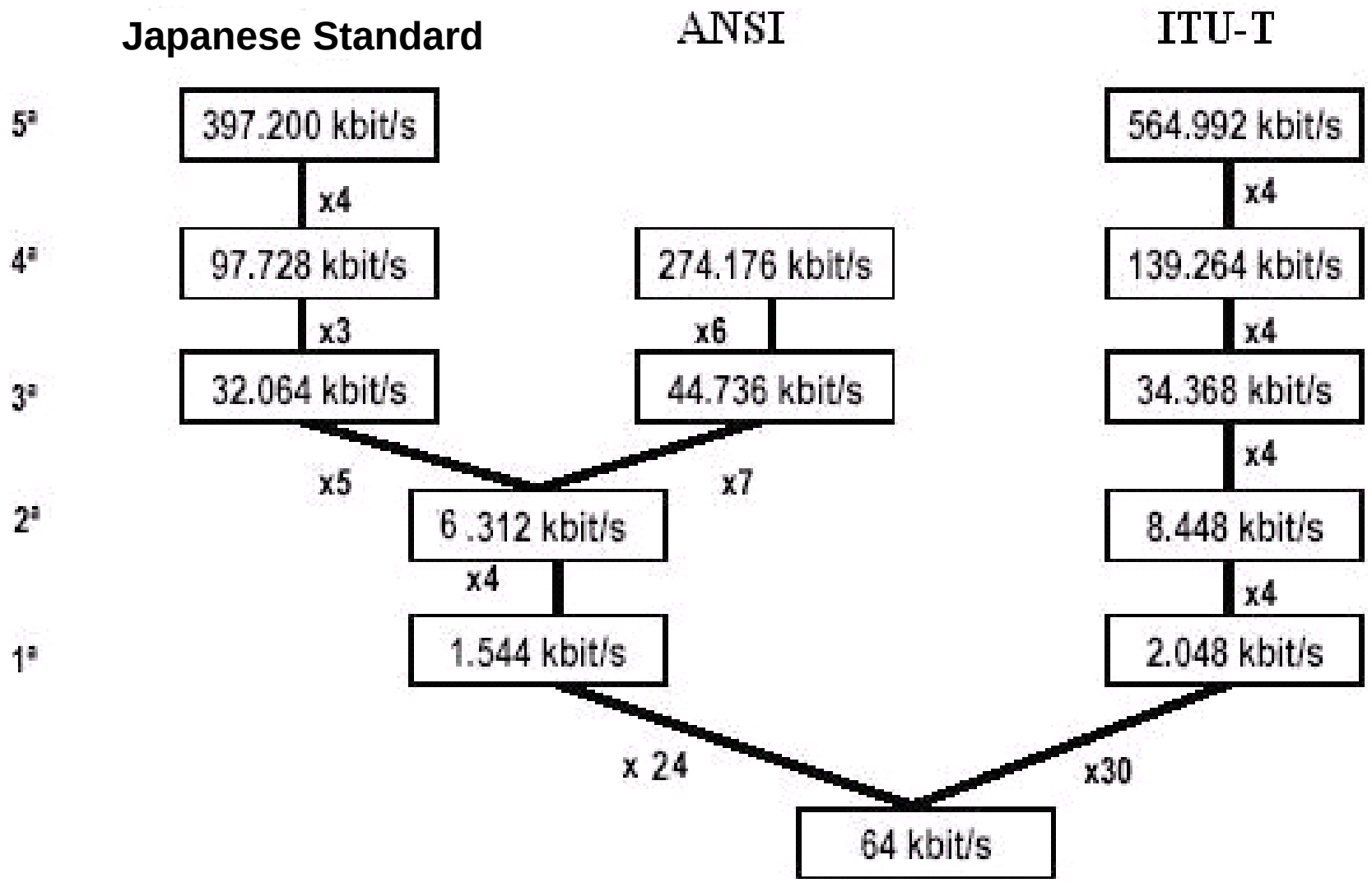


- f_{sn} is the nominal frequency of the locally generated clock;
- f_{pn} is the nominal value of the tributary signal rate;
  - the nominal frequency of the writing clock;
- f_{sn}' is the nominal reading frequency of the elastic buffer;
- f_d is the mean justification frequency;
- f_{dmax} is the maximum justification frequency;
  - obtained when the reading frequency attains the maximum permitted limit, and the writing frequency the minimum permitted limit.
- f_{dmin} is the minimum justification frequencyș
- f_{pmin} , f_{pmax} - minimum and maximum frequency of the tributary signal.

$$f_{sn}' = \eta \cdot f_{sn} \; ; \; f_d = f_{sn}' - f_{pn} > 0 \; ; \; f_{d\max} = \frac{f_{sn}}{N_0} \; ; \; f_{d\min} = 0$$

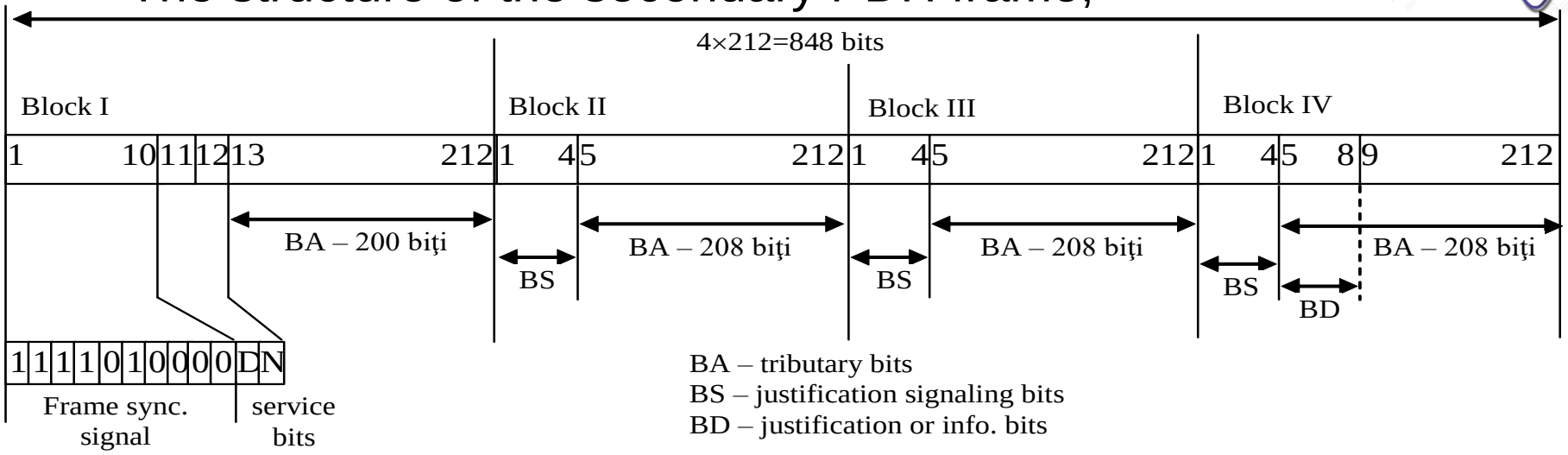
$$f_{pn\min} = f_{sn}' - f_{d\max} \; ; \; f_{pn\max} = f_{sn}' - f_{d\min} = f_{sn}'$$

The PDH multiplexing hierarchy

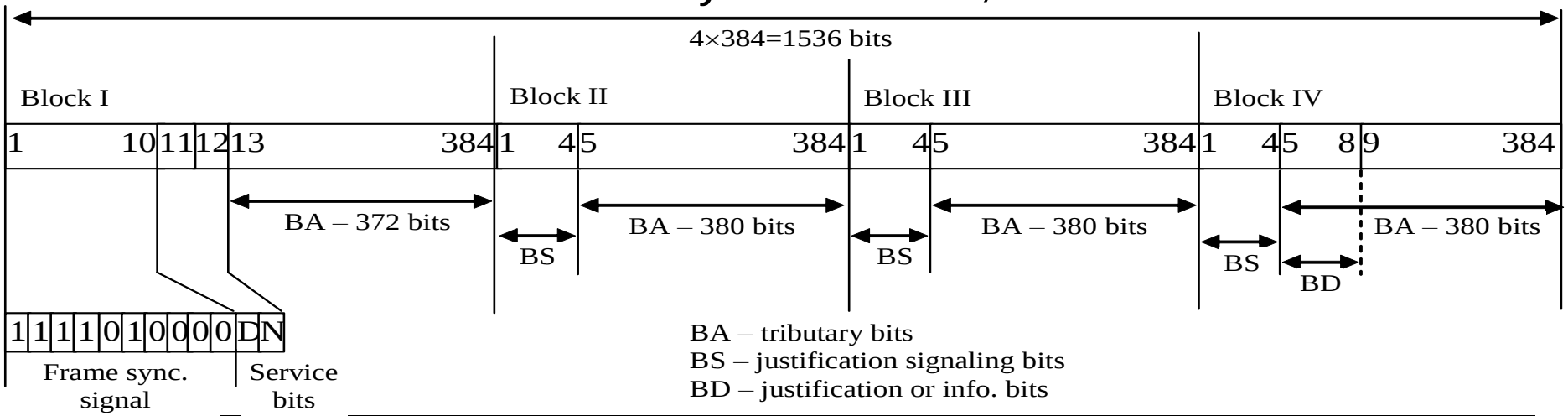


The PDH multiplexing hierarchy

- The structure of the secondary PDH frame;

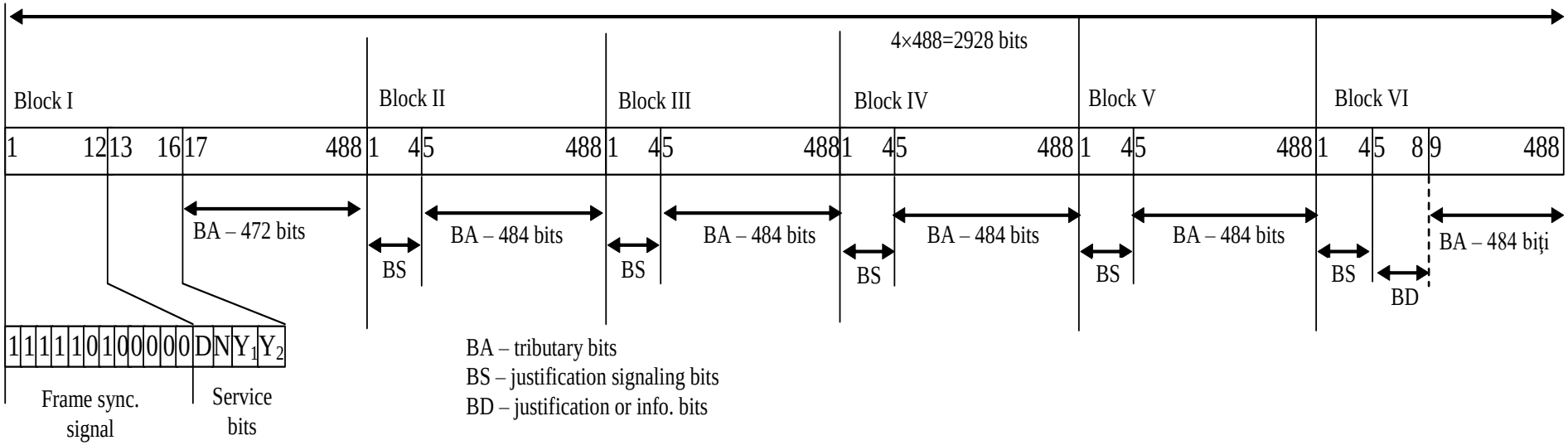


- The structure of the tertiary PDH frame;



The PDH multiplexing hierarchy

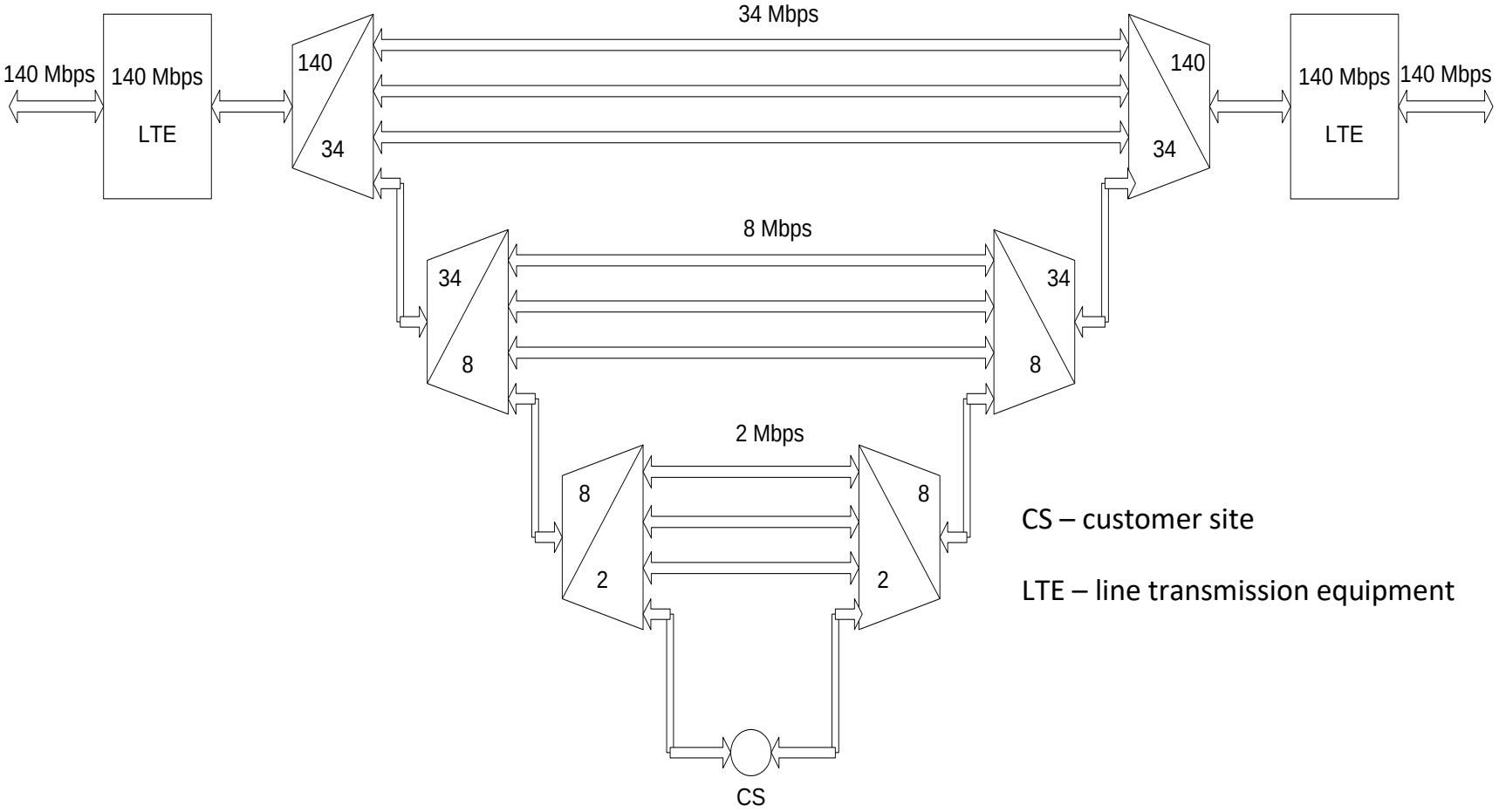
- The structure of the quaternary PDH frame;



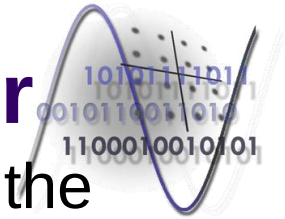
- Disadvantages of PDH systems:
  - limited management and reconfiguration capabilities;
  - low flexibility;
    - designed only for circuit switching (voice transmission);
    - it is relatively difficult to use this system for other services (for ex. packet data);
  - the insertion and extraction of a basic data stream requires the demultiplexig and re-multiplexing of the entire multiplex signal;

The PDH multiplexing hierarchy

- Ex.: insertion / extraction of a 2Mbps stream into / from a multiplex signal having the bit rate 140 Mbps;



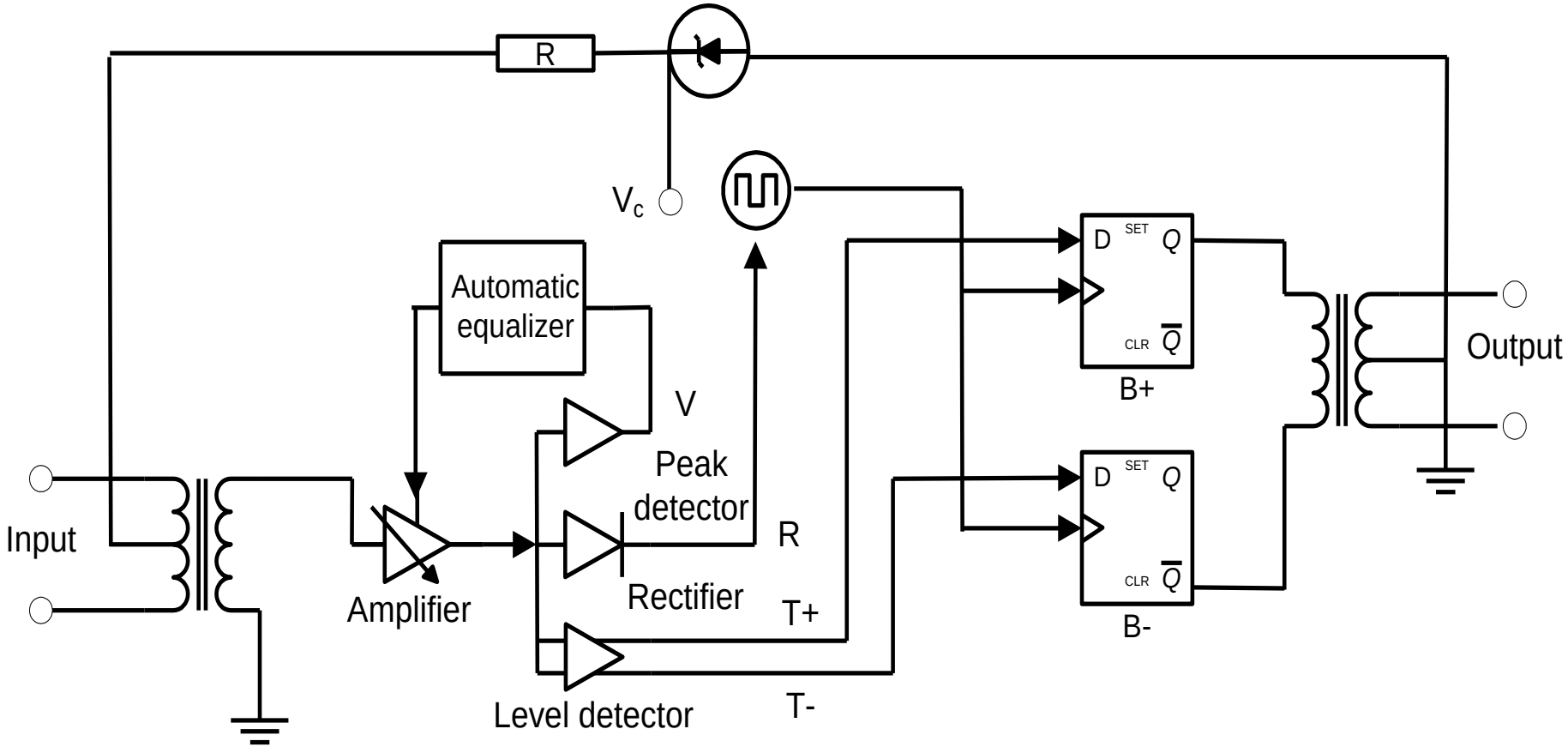
The digital regenerator



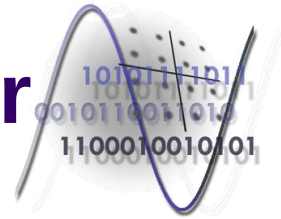
- The regenerator: retransmission relay, which realizes the following operations:
  - Recovers the information bits from the received signal;
  - Re-encodes these bits;
  - Forwards the re-encoded signal on the line.
- The role of the regenerator in a digital system:
  - Reduces the effects of the distortions and noises induced by the channel;
    - the level of linear and nonlinear distortions and that of the noises induced by the channel increases with the length of the transmission medium;
    - the level of the transmitted signal decreases with the length of the channel, due to attenuation;
      - placement of regenerators in several points along the channel (of the transmission line) makes possible to realize high speed transmissions on long channels, in the conditions of imposed bit error probability;
      - the input module of a multiplexer is a regenerator.

The digital regenerator

- Block schematic of a regenerator used in AMI coded transmissions on twisted wire;

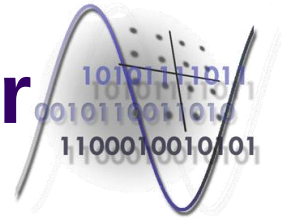


The digital regenerator



- The component blocks of the considered regenerator;
  - Linear input circuits having the following functions:
    - connection to the line;
    - filtering of the received signal in order to reduce the power of the noise;
    - amplification of the received signal up to a constant level;
    - equalization of the received signal in order to reduce the distortions induced by the channel.
  - Linear output circuits having the following roles:
    - connection to the line;
    - amplification of the transmitted signal up to an imposed constant level.
  - Decision and regeneration circuits:
    - regeneration of the impulses received on the line;
      - it is compared the received and equalized signal with reference thresholds in moments when the amplitude of the signal (line impulse) is maximum;
    - transmission the regenerated impulses to the output circuit;
      - the signal is not decoded; only, the line impulses are regenerated.

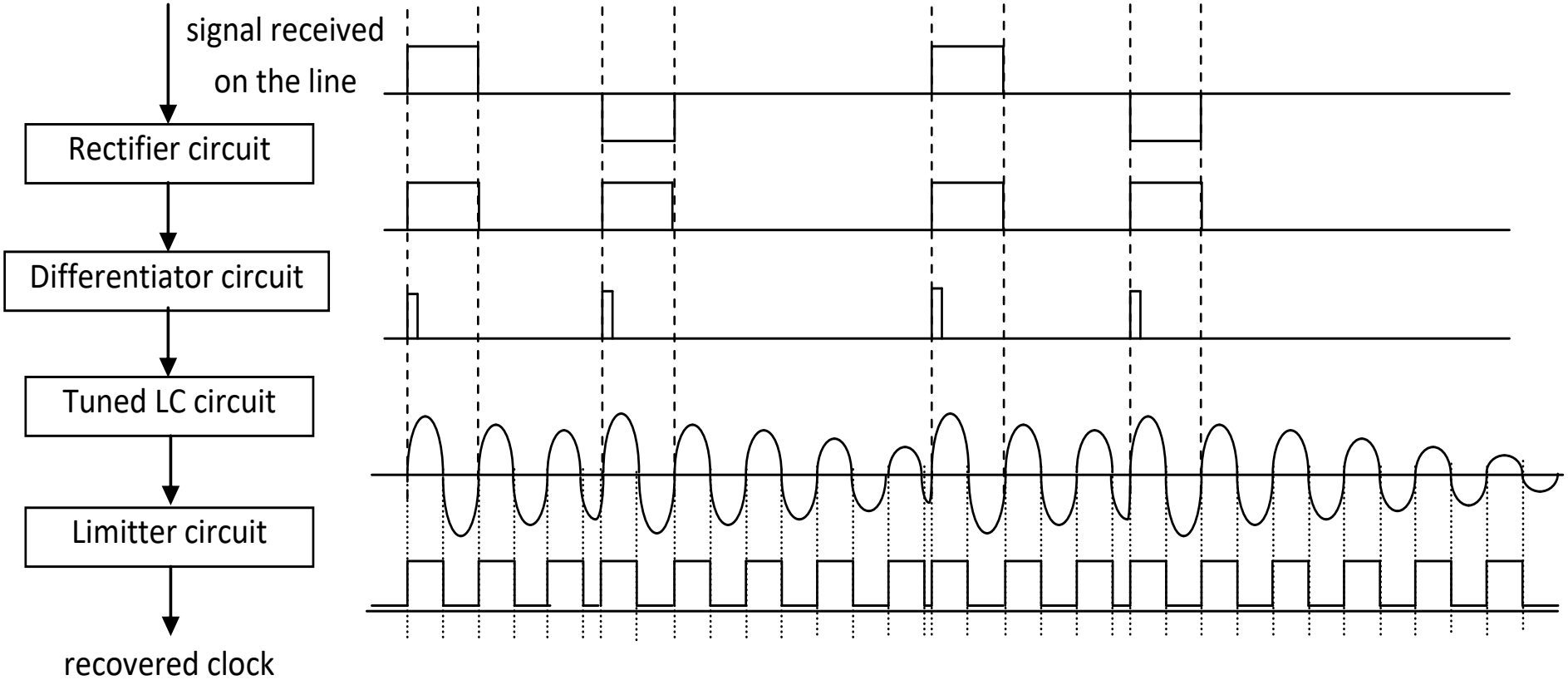
The digital regenerator



- Clock recovery circuit:
  - recovers the clock from the received signal;
  - the recovered clock is used to sample the impulses received on the line and to regenerate these impulses - impulses with imposed width are obtained;
- Auxiliary circuits:
  - remote power supply;
  - fault localization;
  - protection from overcurrent and overvoltage.
- Functioning of the regenerator:
  - the rectified impulses are applied to the clock recovery circuit;
  - the peak-to-peak value of the impulses commands the automatic equalizer and the line preamplifier;
  - the equalized input signal is compared with two thresholds at moments given by transitions of the recovered clock;
  - the logical values obtained after the sampling are stored in the B+ and B- latches and are applied to the output circuit.

The clock recovery

- A simple clock recovery circuit is the so-called clock filter:
  - The block schematic and the signal diagram describing the functioning:



The clock recovery

- Functioning of the clock filter:
  - the equalized and amplified (received) impulses are rectified and after that are differentiated:
    - the impulses generated, having the same polarity, mark the edges (zero crossings) of the received signal;
    - the frequency and phase of these impulses are identical with the average frequency and phase of the transmission clock.
  - the impulses generated are applied to an LC filter tuned on the frequency of the local clock; the signal obtained after the tuned circuit is limited in amplitude;
    - the tuned circuit is a narrow BPF which extracts the fundamental of the impulses obtained after the differentiator circuit;
    - after the limiter the regenerated local clock is obtained.
  - the signal (oscillations) generated by the tuned circuit is damped between two consecutive impulses;
    - the damping increases with the distance (in time) between impulses.
  - the frequency of the signal generated by the tuned circuit is not identical with the frequency of the transmitter clock;
    - there are not generated impulses at each bit edge due to the zero levels from the AMI coded signal.

The clock recovery

- the free oscillation frequency of the tuned circuit is not identical with the frequency of the transmitter clock;
  - phase hits (signal discontinuities) appear in the signal generated by the tuned circuit in each moment when impulses are applied to its input.

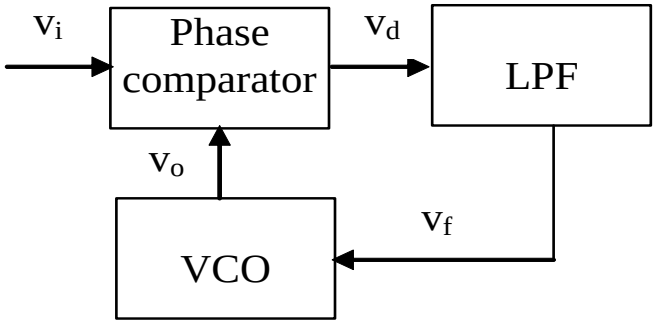
- The clock filter is a simple clock recovery circuit, but has relatively reduced performances in what concerns the precision of the frequency and phase of the recovered clock;
- The circuit can be used in base band transmission systems with 2 or 3 levels on the line, like the telephone transmission systems;
  - in the case of these systems less restrictive conditions are imposed to the recovered clock (due to the reduced number of levels on the line);
- The in – out phase transfer function of the clock filter:

$$C(s) = \frac{1}{1 + s/B}$$

  - $s=j\omega$, $B=\omega_0/2Q$ is the half of the bandwidth of the band pass filter (circuit) tuned on the clock frequency.

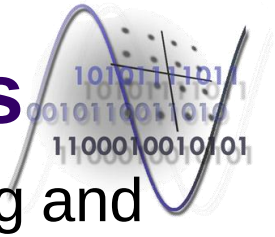
The clock recovery

- Improvement of the clock filter performances can be obtained by applying the signal generated by the limiter to a PLL circuit;
  - the PLL circuit reduces significantly the frequency and phase variations of the signal obtained after the tuned circuit or after the limiter.
- Block schematic of the PLL (Phase Locked Loop) circuit;



- Functioning:
  - the phase comparator compares the phases of the received and locally generated signals and generates a command voltage to the voltage-controlled oscillator;
  - the command voltage is filtered by a low pass filter in order to suppress the high frequency components;
  - the phase comparator is a multiplier circuit in analog implementations.

The jitter in digital systems



- The notion of jitter differs very much in the case of analog and digital systems:
  - In analog systems the jitter is due to the frequency multiplexing systems;
    - it represents a parasitic phase modulation characterized by:
      - amplitude (maximum value of the phase deviation);
      - frequency (frequency of the phase change).
  - In digital systems the jitter means the modification of the significant moments of the digital signal relatively to the ideal values;
    - there are significant differences between the jitter sources in the two type of systems;
    - in digital systems the jitter has two variants, namely:
      - short time variations of the significant moments;
        - this phenomenon is called effectively jitter;
      - long time phase variations – the „wander” phenomenon;
        - these are slow variations of the significant moments of the digital signal relatively to their ideal positions.

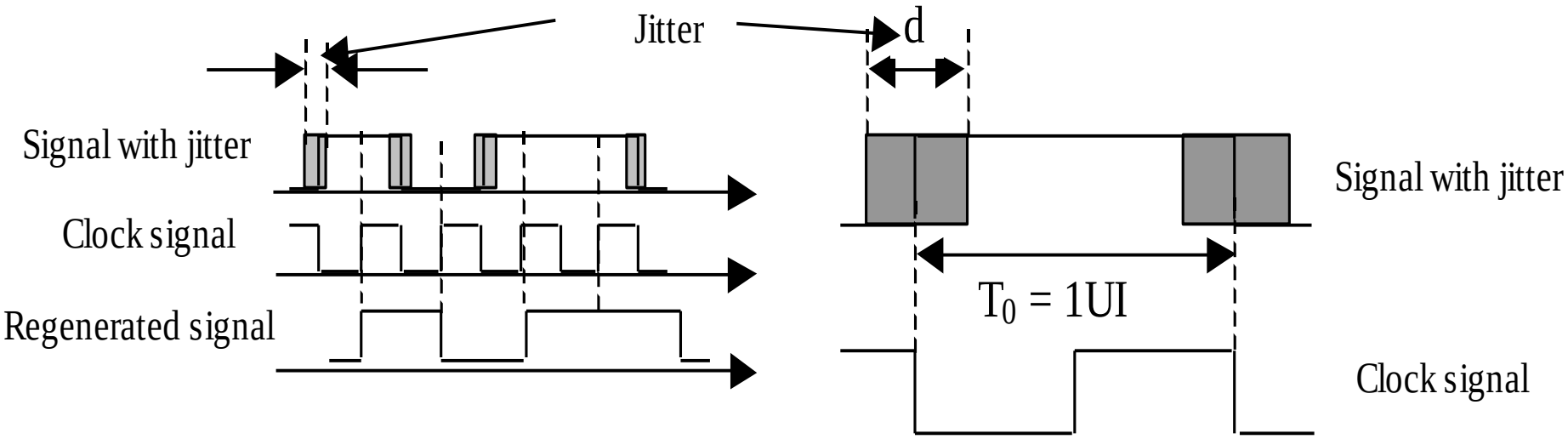
The jitter in digital systems

- The difference between the two type of phase variations (jitter/wander) is related only to the frequency range;
  - doesn't exist a clear definition of the frequency limit between jitter and wander;
    - as a rule of thumb, phase variations with frequency below 10Hz are called wander.
- Jitter phenomenon observed at the output of digital sections;

  - the digital signal before regeneration is characterized by modifications of the symbol edges relatively to the ideal position - reference is the clock signal;
  - if the clock signal does not present any jitter, then the regeneration process, by sampling at the middle of the signal elements, might ensure a jitter free recovery of the digital signal;
  - the maximum peak-to-peak trip of the signal transitions before regeneration is equal with the duration T_0 of a signal element:
    - called Unit Interval UI;
  - the overrun of this value leads to erroneous decisions;
    - the peak-to-peak amplitude of the jitter can be expressed also in percents.

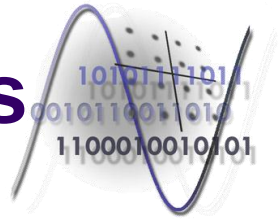
The jitter in digital systems

- Suppression of the jitter by ideal regeneration – fig. a);
- Definition of the jitter peak to peak value – fig. b;



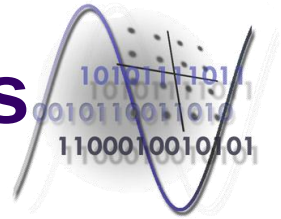
- Has to be noticed that in data transmissions to the jitter term corresponds the usual term of total telegraphic distortion, expressed in percents;
  - the two phenomenons have a common connotation.

The jitter in digital systems



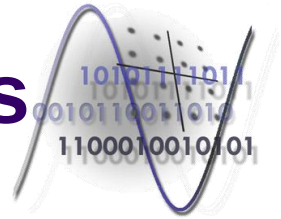
- Jitter tolerance;
  - The maximum value of the jitter which does not induces erroneous decisions;
  - Differs according to the frequency in the following way:
    - at low frequencies it is possible to exceed the limit of 1 UI without generating erroneous decisions;
      - the recovered clock absorbs almost completely this jitter, by following the slow phase variations of the received signal and realizing a correct sampling;
        - the system can tolerate a phase variation higher than 1 UI (even much higher).
    - the clock recovery circuits have a low pass type phase transfer characteristic according to the frequency;
      - only low frequency jitter components appear in the regenerated signal;
    - at high frequencies of the jitter, the recovered clock (from the digital signal) cannot follow the jitter;
      - the peak-to-peak amplitude of the jitter cannot exceed 1 UI, being in reality fractions of UI.

The jitter in digital systems



- The effects of the jitter and wander consist in the following:
  - It is modified (decreased) the reserve of the digital transmissions to other imperfections of the channel (for ex. noise);
  - When exceeding a given limit a significant increase of the error probability on digital sections is induced;
    - this effect is reflected in voice channels as impulse noise and background noise.
  - The apparition of an analog jitter in the analog voice channel;
    - this jitter appears in the D/A conversion process in PCM systems due to the jitter affecting the clock, jitter which is transmitted as a parasitic position modulation to the impulses with amplitude modulation (PAM) obtained after the D/A converter.

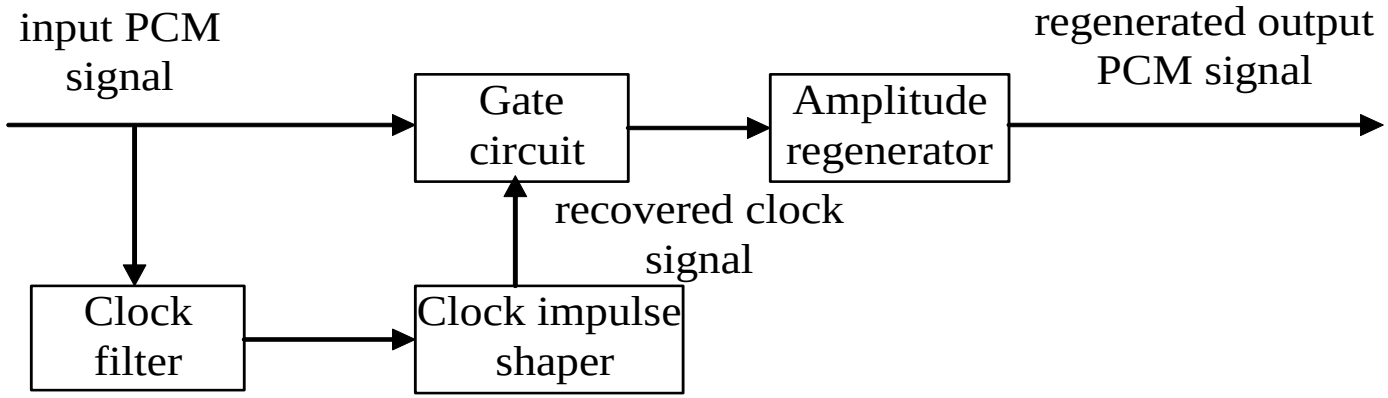
The jitter in digital systems



- The jitter can be classified as:
  - Systematic variations;
    - phase variations dependent on the structure of the digital signal (pattern-dependent variations);
    - these phase variations appear due to several identical and correlated interconnected digital units;
      - the effect is significantly cumulative.
  - Nonsystematic variations:
    - this type of jitter supposes the absence or low correlation degree of the different jitter sources;
    - these variations has a stochastic (or semi-stochastic) character and do not depend on the transmitted digital sequence (pattern-independent variations);
    - this type of jitter has a low influence on the quality of transmission;
      - the effect is noncumulative or is weakly cumulative.

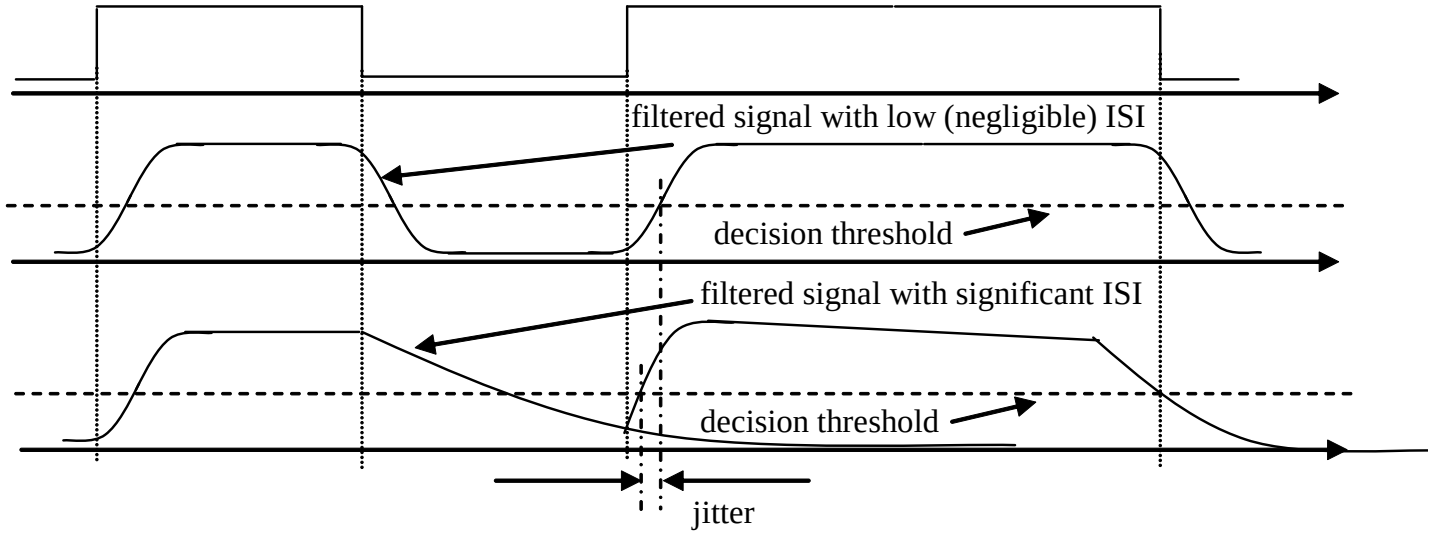
The origin of the jitter

- The most important jitter sources:
  - **The digital regenerator:**
    - a regenerator reconstructs the received digital signal using a clock signal extracted from the received signal;
    - due to the imperfect recovery this clock signal is affected by a parasitic phase modulation which is integrally transmitted to the regenerated signal as a jitter;
    - in the regeneration process each regenerator distorts the clock signal and through this induces jitter in the output signal;
      - this jitter is added with the jitter generated in other units of the regenerator chain.
  - The basic idea of digital signal regeneration:

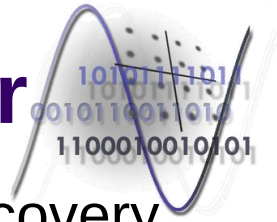


The origin of the jitter

- The imperfections affecting the clock recovery process:
  - Intersymbol Interference (ISI);
    - the attenuation and group delay distortions induced by insufficiently equalized transmission lines modify the shape of the received impulses;
      - it results a distortion of the signal elements and an ISI phenomenon appears;
        - superposition of the adjacent symbols;
    - a jitter phenomenon appear after limiting the received digital signal;
      - this jitter is strongly dependent on the signal pattern;
      - this jitter is transferred also on the recovered clock signal.



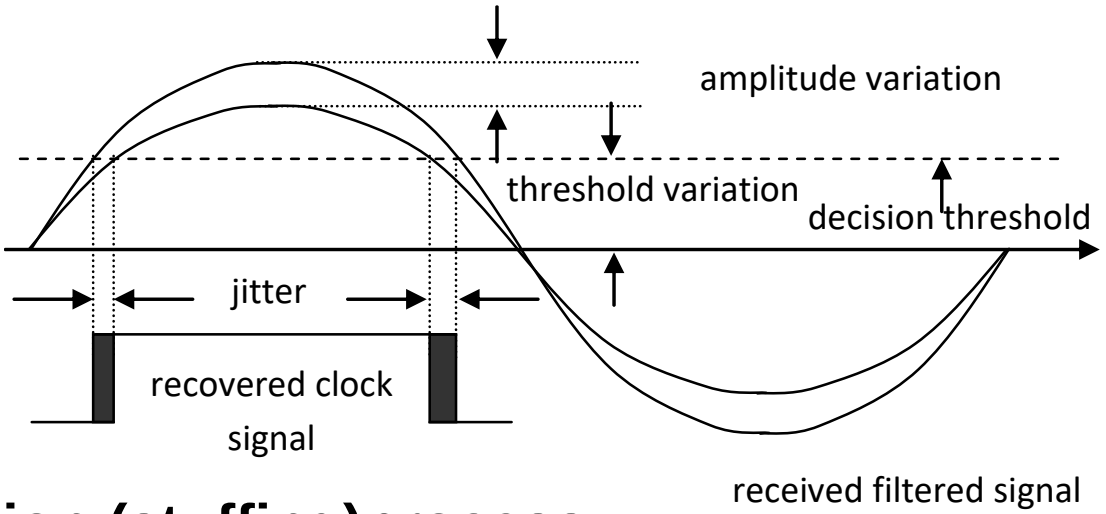
The origin of the jitter



- The ΔF error of the resonance frequency of the clock recovery circuit;
  - the clock recovery device acts as a narrow band pass filter tuned on the clock frequency;
  - when the synchronization impulses are missing the oscillations generated by the clock recovery circuit are damped;
  - if there is a ΔF difference between the resonance frequency of the tuned circuit and the clock frequency of the received signal, the resynchronization after a time period when there are no synchronization impulses is generating a phase shift in the recovered clock signal;
    - it is a signal pattern dependent jitter.
- The MA/MΦ conversion;
  - it is generated by the amplitude comparator from the impulse regenerator block (the amplitude regenerator);
    - the jitter appears due to change of the comparison threshold and / or of the received signal amplitude.

The origin of the jitter

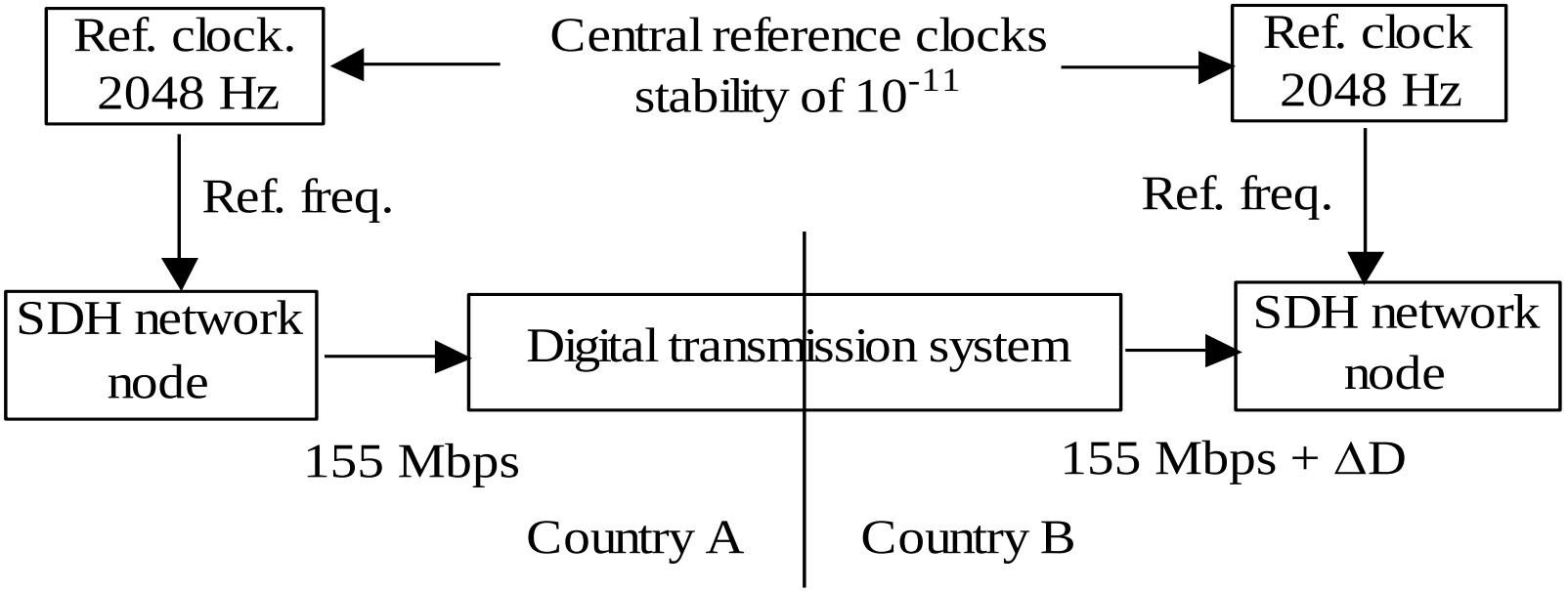
- The MA/MΦ conversion phenomenon and the associated jitter;



- **The justification (stuffing)process;**
  - the jitter associated to the justification (stuffing) process appears at the output of the multiplexing equipments of superior order, when the multiplexing process operates on several plesiochronous tributaries;
  - this jitter is composed of two components, namely:
    - justification jitter: when the justification process is performed immediately at request;
    - waiting jitter: defined as a low frequency jitter;
      - it is related to the waiting time between the justification request and the completion of this request.

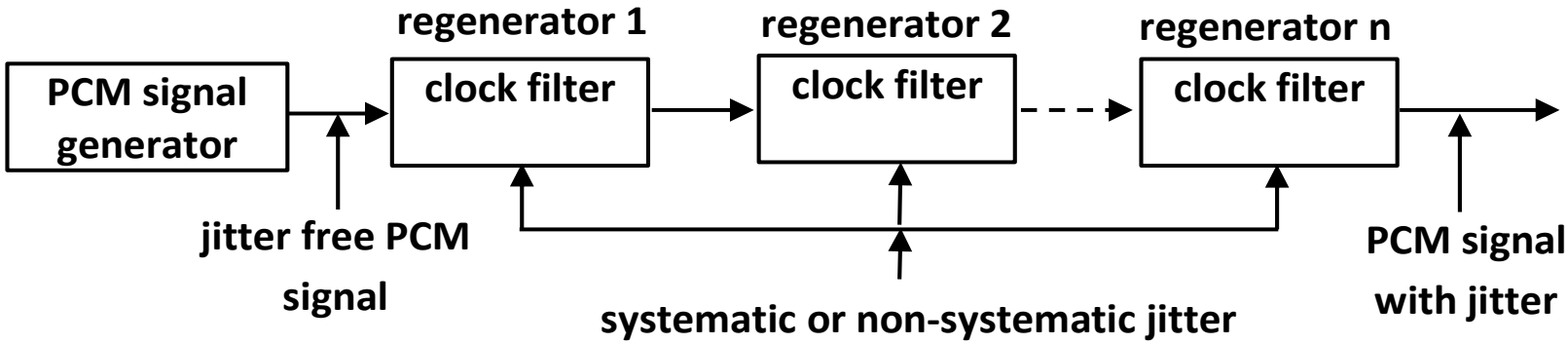
The origin of the jitter

- **The wander;**
  - Can appear due to several reasons, the most important being:
    - modification of the transmission medium characteristics;
    - variations of the frequency of the clock generators of network nodes.
  - The generation of the wander;



The accumulation of the jitter

- There are considered two possible situations, namely:
  - **1. Chain of cascaded regenerators:**
    - the jitter character is preponderantly systematic (dependent on the digital signal sequence)
    - the main cause: the imperfections of the clock recovery circuits;



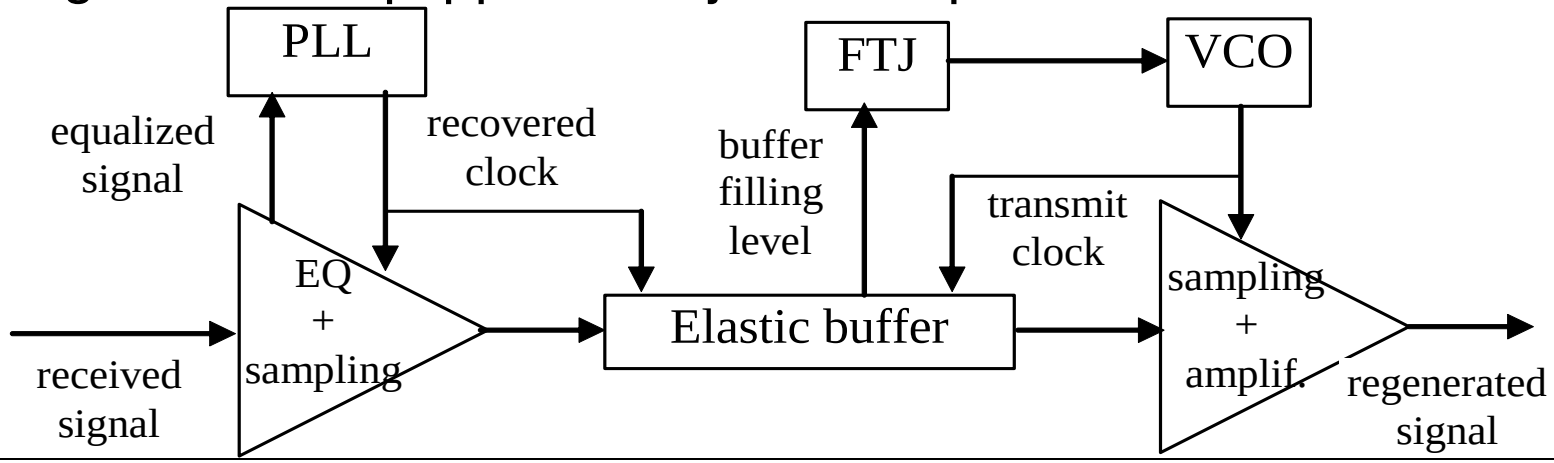
  - Jitter accumulation on a regenerator chain with non-correlated jitter sources:
    - the summation law is: $J_N = J_1 \cdot \sqrt[4]{N}$
    - J_1 is the effective value of the jitter generated by each regenerator, J_N is the global effective value of the jitter;
    - this situation has a minor importance in digital transmissions.

The accumulation of the jitter

- Jitter accumulation on a regenerator chain with correlated jitter sources : dependent on the bit sequence;
  - summation law of the systematic jitter: $J_N = J_1 \cdot \sqrt{2N}$
  - J_1 is the effective value of the jitter generated by each regenerator;
  - the values of J_1 are situated usually in the 0,4 – 1,5% UI range;
  - if PLL loops are used for clock recovery the summation law is: $J_N = J_1 \cdot \sqrt{2NA}$
    - where A is a factor dependent on the number of regenerators and on the PLL loop characteristics;
  - this situation has a major importance in digital transmissions;
  - probabilistic distribution of the jitter amplitude, close to the Gaussian distribution;
    - a ratio of peak-to-peak value / effective value of 12 – 15 is usual and corresponds to a low probability of exceeding the peak value.

The accumulation of the jitter

- Jitter reducing methods on a regenerator chain:
  - utilization in regenerators of transformation devices which operate on the signal sequence:
    - pseudo-random sequence generators, scramblers, addition to the signal of his own delayed sequences;
  - utilization of buffer memories in regenerators, memories which absorb the sudden variations of the regenerated clock;
    - devices which decrease the jitter level;
    - called „jitter reducers” or “jitter compensators”;
    - the transmit clock is controlled by the filling level of the buffer memory.
- Regenerator equipped with jitter compensator;



The accumulation of the jitter

- Jitter accumulation in systems which include scrambler and jitter compensator devices;
  - in these systems the regenerators act as uncorrelated jitter sources;
  - the summation law is: $J_M = J_S \cdot \sqrt[4]{K \cdot N}$
  - J_S is the effective jitter of a system, K is a constant with values located between 1 and 2 (K=2 for N high), N is the number of digital systems.

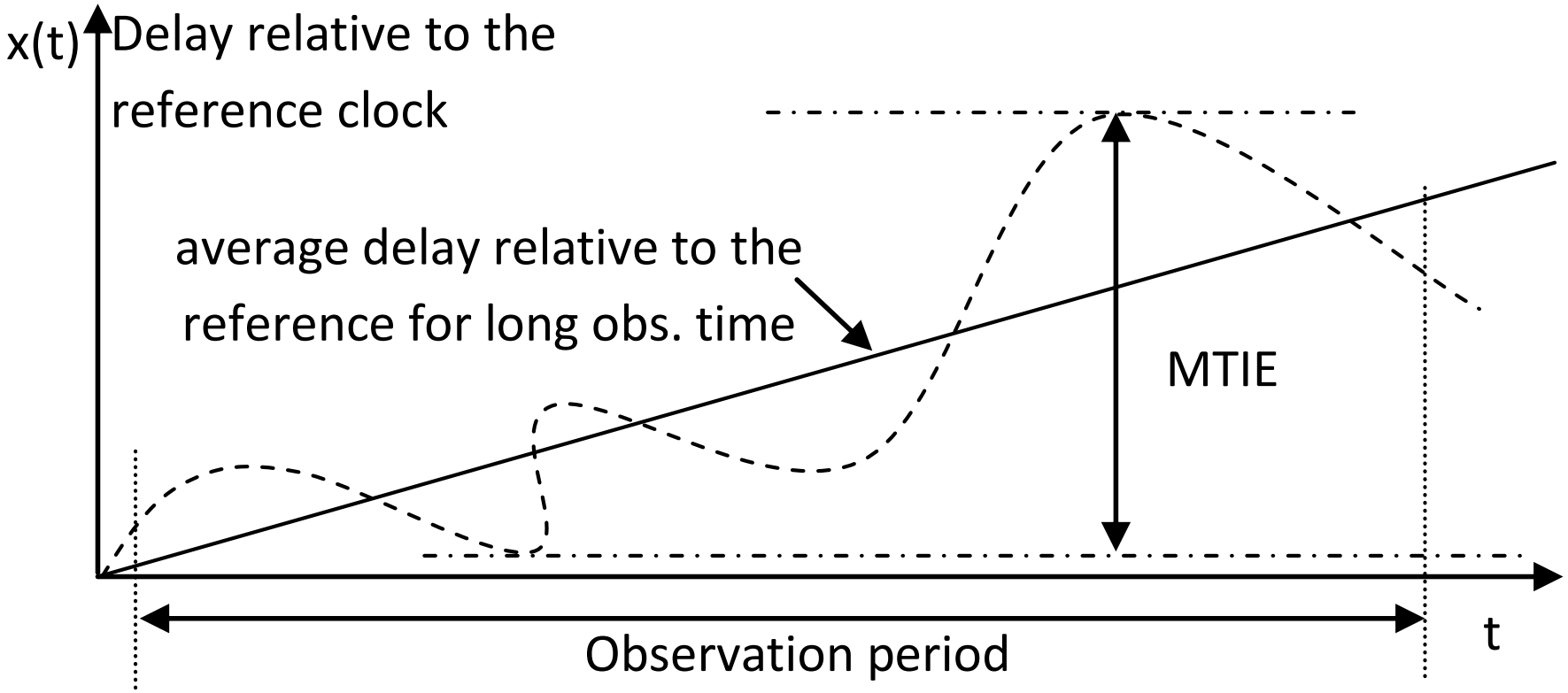
- **2. Multiplexing – demultiplexing equipments:**
  - appears an accumulation of the waiting jitter: $J_S \cdot \sqrt[4]{N} \le J_M \le J_S \cdot \sqrt{N}$
  - J_M : the effective value of the accumulated jitter;
  - J_S : the jitter of individual equipment;
  - N: the number of multiplexing equipment.

Jitter performances

- Limits for wander;
  - The wander is a slow phenomenon generated by the:
    - transmission medium characteristics;
    - the aging of the clock regenerators;
  - The wander could generate the clock slide phenomenon;
    - it is defined the MTIE (Maximum Time Interval Error) parameter:
      - the peak-to-peak variation of the received signal delay relatively to an ideal signal (i.e., a reference clock) in time interval S;
      - for S>10^4s we have: $TIE = \left(10^{-2} \cdot S + 10000\right) ns$
  - The case of independently synchronized networks:
    - the TIE value between the input signal and the synchronization signal of the equipment which ends the connection can exceed the maximum value imposed for the wander and it is possible to appear clock slides (generating errors) with a frequency between 1 and 70 days.

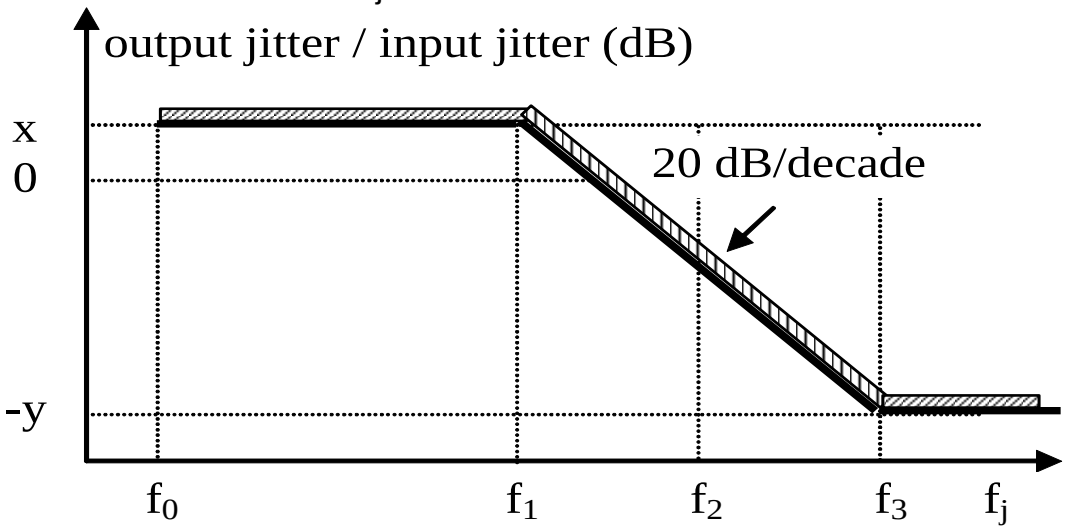
Jitter performances

- Definition of the MTIE parameter associated to wander;



Jitter performances

- Jitter transfer characteristic of digital equipment;
  - The transfer characteristic $H(f_j)$ of the jitter, represents the ratio between the jitter at the output and at the input of the equipment expressed in dB, according to the frequency, at a specified rate;
    - usually are attenuated the jitter components situated above a given frequency;
    - the general characteristic $H(f_j)$ is of low pass type;



- The maximum jitter at the output of the digital equipment;
- The maximum jitter at the output of the digital sections.

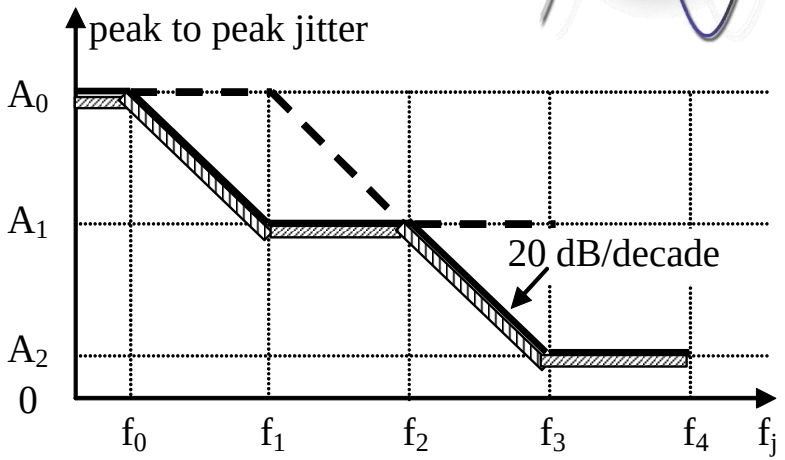
Jitter performances

- Jitter performances of plesiochronous digital transmissions with different bit rates;
  - The performances refer to maximum allowed limits for jitter and wander amplitude;
  - Limits imposed for the maximum amplitude of the jitter;

Jitter type → / Bit rate (kbps) ↓	Jitter measured in wide band		Jitter measured in narrow band	
	Peak to peak maximum value in UI	Measurement frequency band	Peak to peak maximum value in UI	Measurement frequency band
64	0,25	20Hz÷20kHz	0,05	3kHz÷20kHz
2048	1,5	20Hz÷100kHz	0,2	18kHz÷100kHz
8448	1,5	20Hz÷400kHz	0,2	3kHz÷400kHz
34368	1,5	100Hz÷800kHz	0,15	10kHz÷800kHz
139264	1,5	200Hz÷3500kHz	0,075	10kHz÷3500kHz

Jitter performances

- Maximum allowed peak to peak values for jitter and wander;
  tolerance to jitter and wander;



- peak to peak jitter – frequency characteristic:

Parameter values → / bit rate (kbps) ↓	Peak to peak jitter value (UI)			Frequency (Hz)				
	A_0	A_1	A_2	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)
64	1,15	0,25	0,05	$1{,}2\times10^{-5}$	20	600	3	20
2048	36,9	1,5	0,2	$1{,}2\times10^{-5}$	20	2400 (93)	18 (0.7)	100
8448	152	1,5	0,2	$1{,}2\times10^{-5}$	20	400 (10700)	3 (80)	400
34368		1,5	0,15		100	1000	10	800
139264		1,5	0,075		200	500	10	3500