Course 10-11. Multiplexing of plesiochronous signals. The PDH multiplexing hierarchy. The digital jitter

- Multiplexing of digital signal → the interleaving of N sources having f_c bit rate in a digital stream having a bit rate f_m, greater or equal with $N \cdot f_c$;
  - at reception demultiplexing implies the recovery of the N sources, using auxiliary circuits located at the transmission and at the reception side (Transm. ctrl. and Rec. ctrl.)

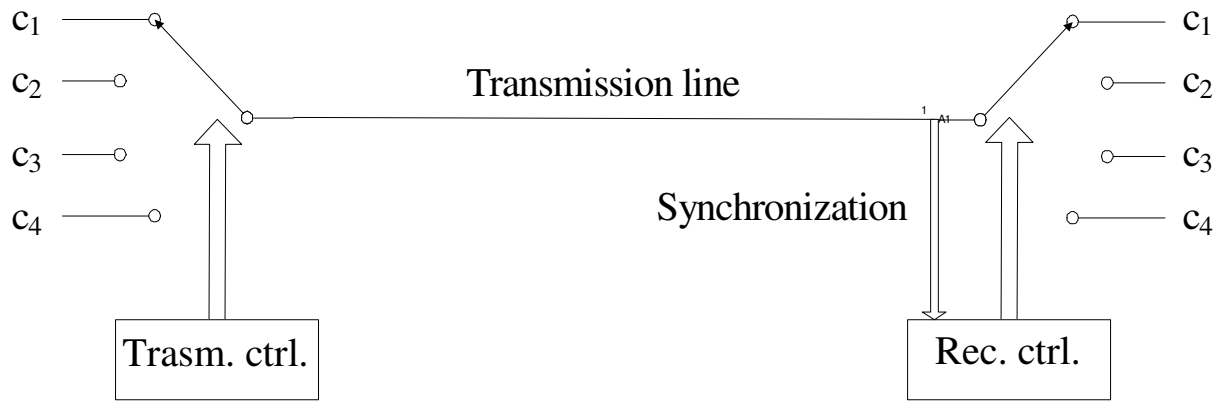

Fig. 1 Multiplexing and demultiplexing of digital signals

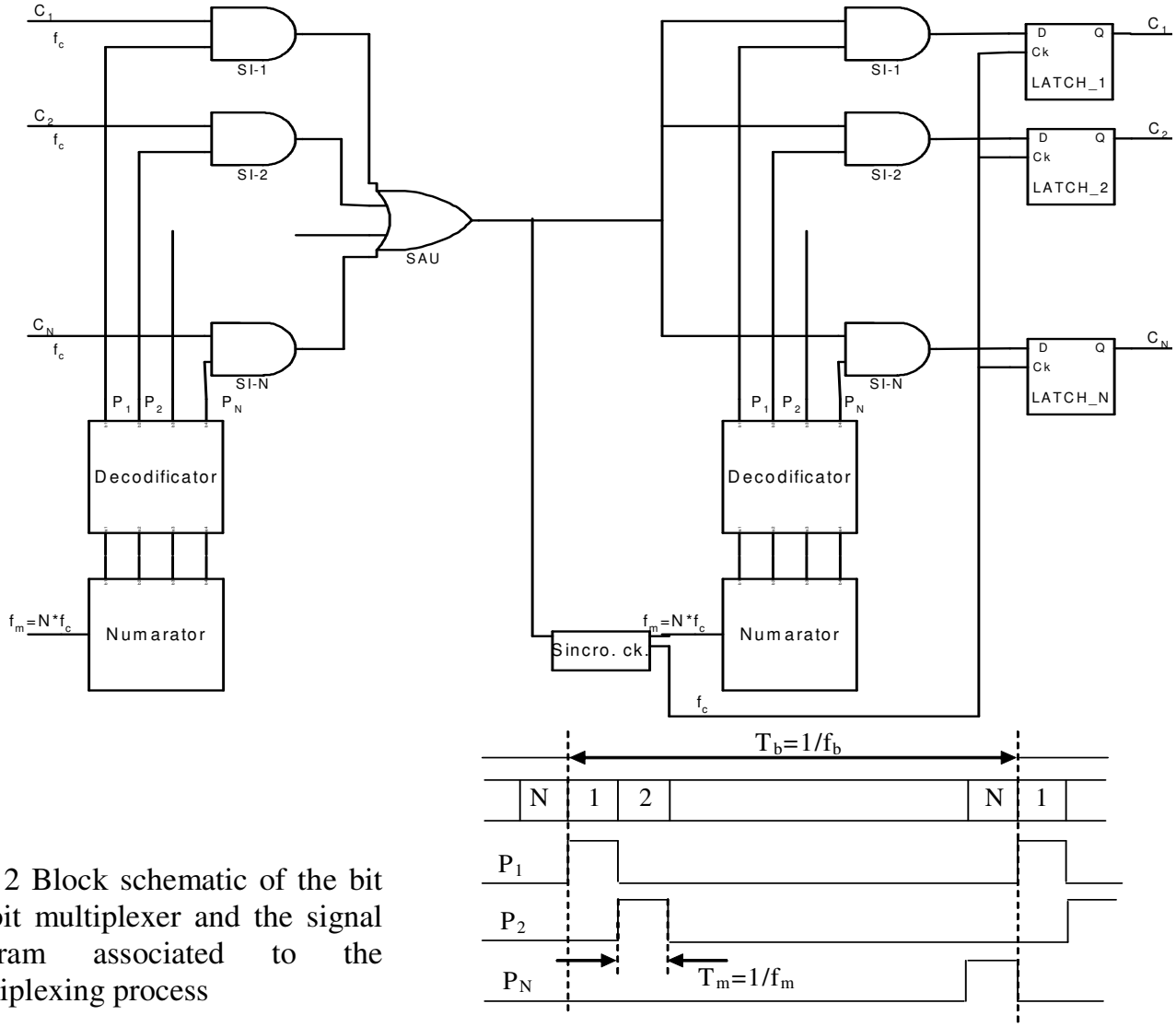

Fig. 2 Block schematic of the bit by bit multiplexer and the signal diagram associated to the multiplexing process

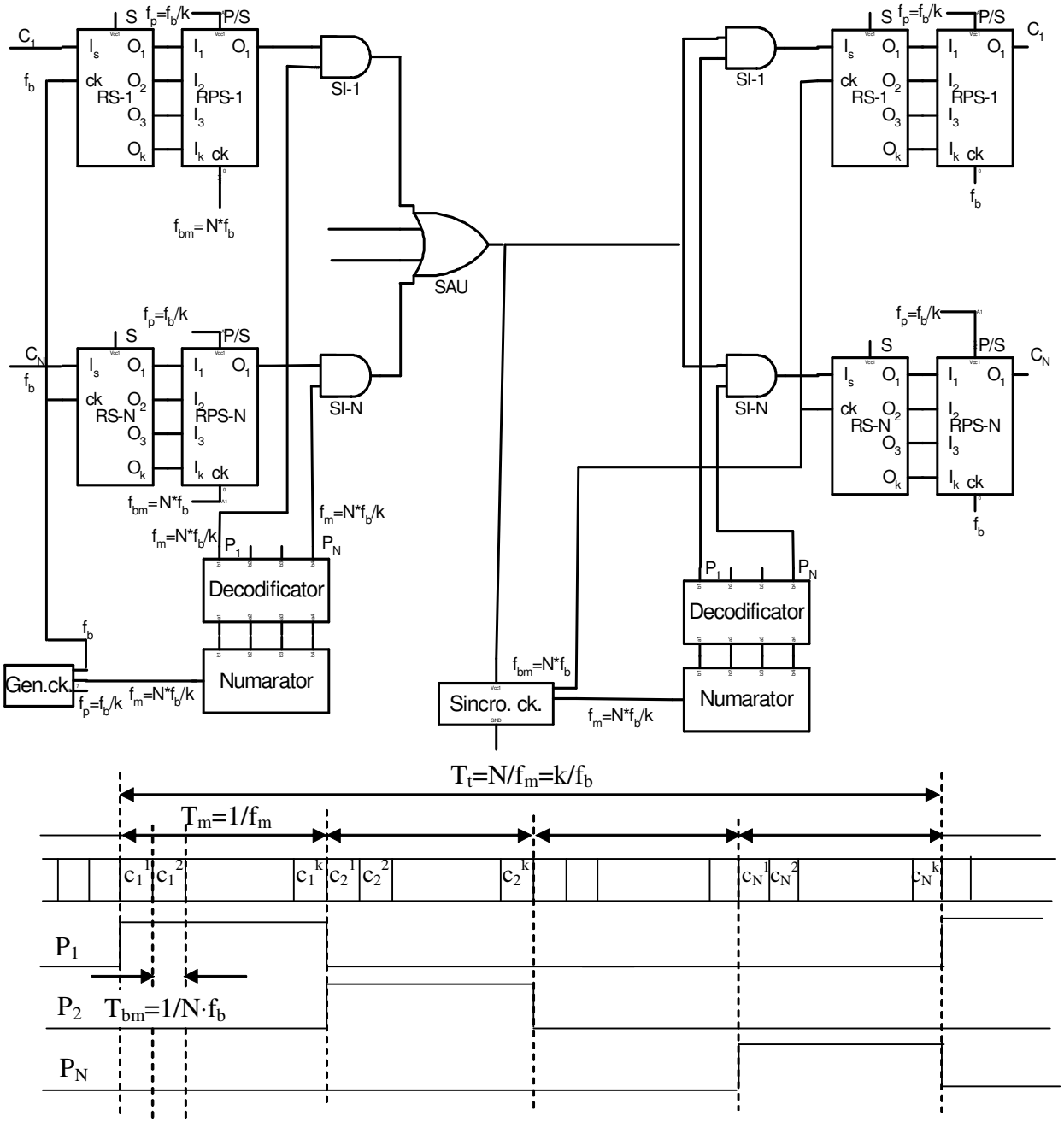

Fig. 3 Block schematic of the channel by channel multiplexer and the signal diagram associated to the multiplexing process

- Classification of digital signals from the point of view of their generation and the relation between their clock signals:
  - Isochronous signal – the time interval between two significant moments is theoretically equal with a unitary time interval or with a multiple of this;
  - Non-isochronous signals – the time interval separating two significant moments it is not necessarily related to a unitary interval or to a multiple of this; the symbols of a non-isochronous binary signal do not have the same duration.
  - Homochronous signals – isochronous signals with the same rate and constant phase relation; can be divided in:

❖ Mesochronous signals – isochronous signals with the same rate and non-constant phase relation – constant average phase relation.

❖ Synchronous signals – isochronous signals with the same rate and constant phase relation.

- Heterochronous signals – isochronous signals with different rates and variable phase relation; plesiochronous signals – signals with the same nominal rate, all the variations of this rate being maintained between specified limits – for ex. signals with identical nominal rates from different sources.

- **Multiplexing of plesiochronous signals**
- Multiplexing of the plesiochronous digital signals can be done in two possible ways:
  - Generation of signals with high stability of the clock frequency and use of some buffers – very high price and periodical lose of information;
  - Use of the justification (stuffing) method – without information loss; the functioning principle is presented in fig. 4;

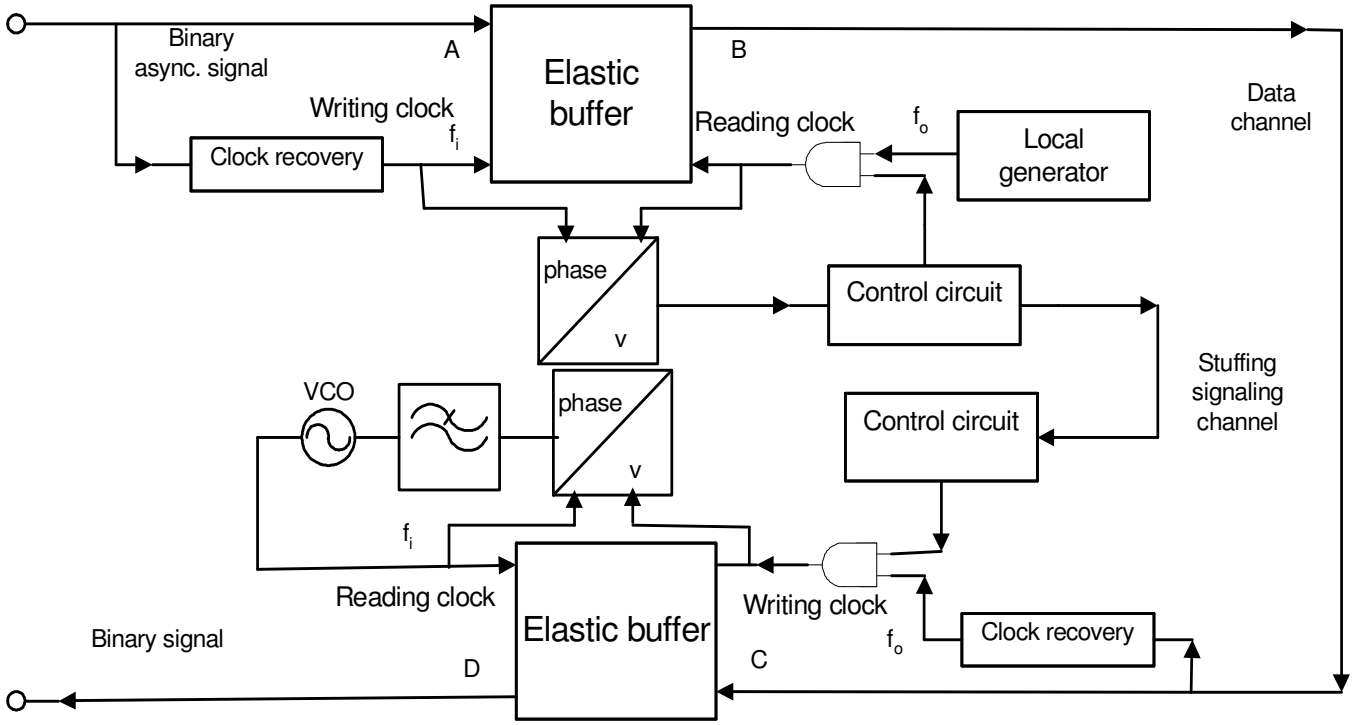

Fig. 4 Multiplexing of plesiochronous digital signals – rate adaptation blocks at transmission and reception side

- the asynchronous binary signal is written in the elastic memory with a specific clock frequency, f_i;
- the reading of the memory and the transmission of the signal in the channel is done with a higher clock frequency $f_o > f_i$ and appears a clean out tendency of the elastic memory content, which is prevented by the phase comparator;

- when a threshold phase difference value is exceeded, the phase comparator gives a blocking commands of the reading impulse – it is created a break in the line signal (one stuffing impulse) which decreases the phase difference between the clock signals;
- the justification (stuffing) is signaled to the reception side on a link multiplexed with the data signal → the signaling of the justification (stuffing) is necessary to inform the receiver about the exact moment and location of the justification (stuffing), information necessary for suppression of the justification (stuffing) bits in the receiver;
- only the information bits are written in the memory at the reception side with a frequency f_o, the memory being read with a frequency f_i;
  - the extraction of the justification (stuffing) impulses generates a jitter in the output signal – this jitter is controlled by a PLL loop which reduces the effects of the jitter.

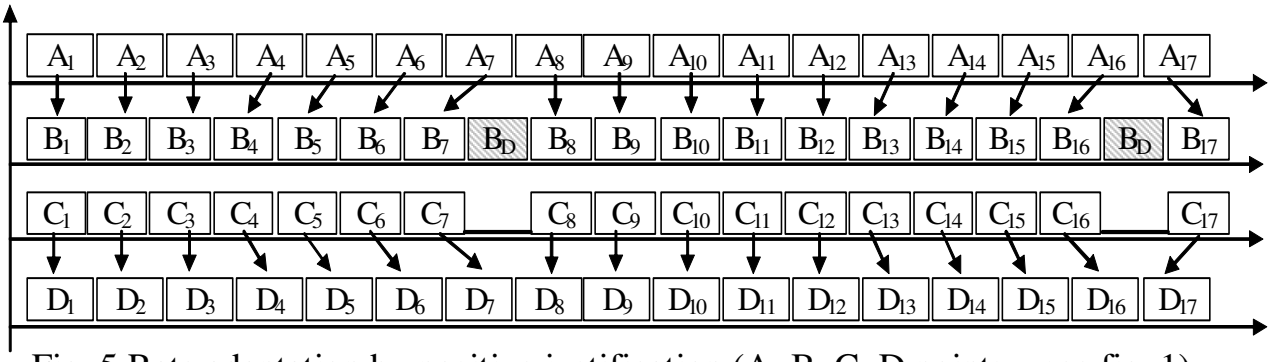

Fig. 5 Rate adaptation by positive justification (A, B, C, D points – see fig. 1)

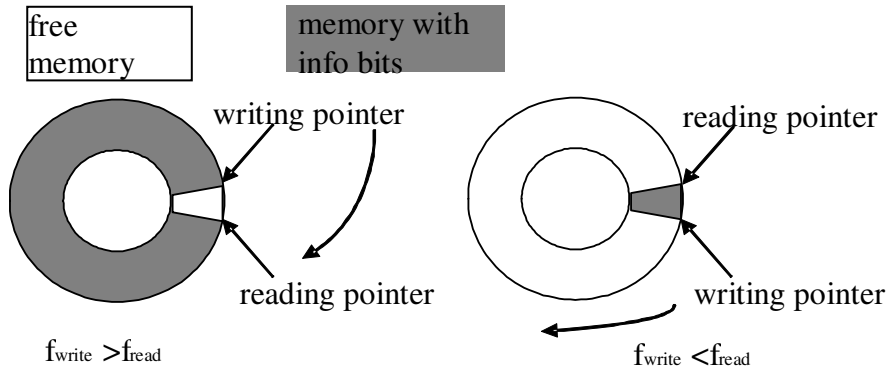

Fig. 6 Rate adaptation using elastic buffers

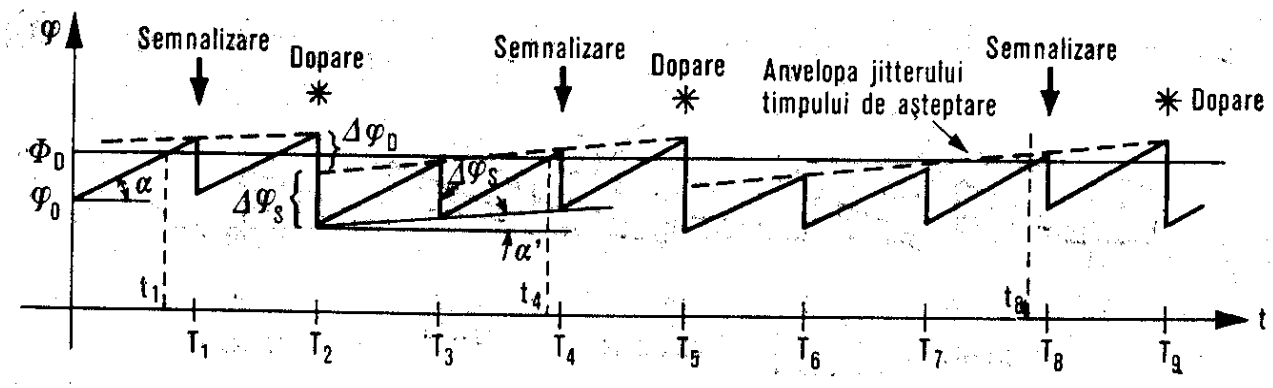

Fig. 7 Phase variations in the case of positive justification

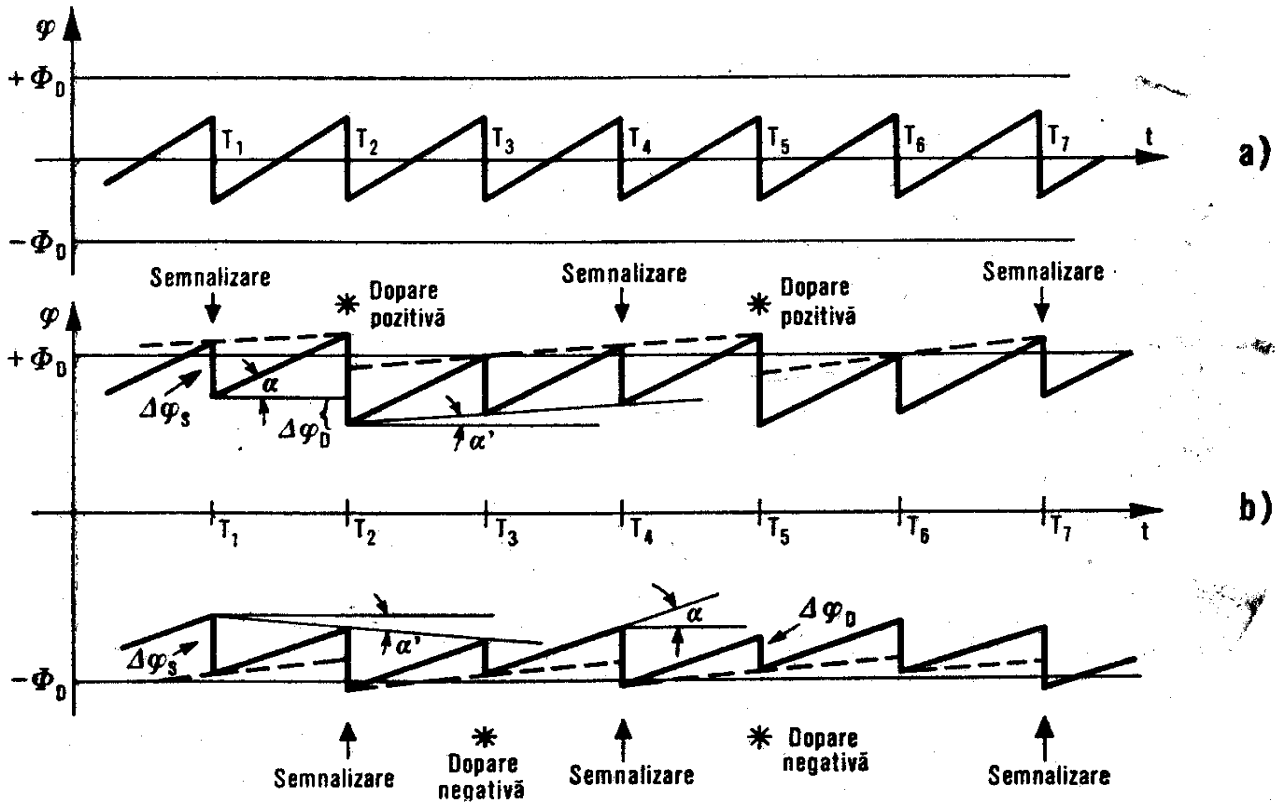

Fig. 8 Phase variation in the case of positive-negative justification

- The problem of justification signaling insertion can be solved in two ways:
  - individual insertion, in which case the insertion of signaling and justification bits is realized before multiplexing – flexible and low complexity method at reception;
  - common insertion, in which case the signaling information of the all tributary signals are concentrated on a common path which is then multiplexed with data in an imposed interval of the transmission frame – higher implementation simplicity but lower flexibility method.

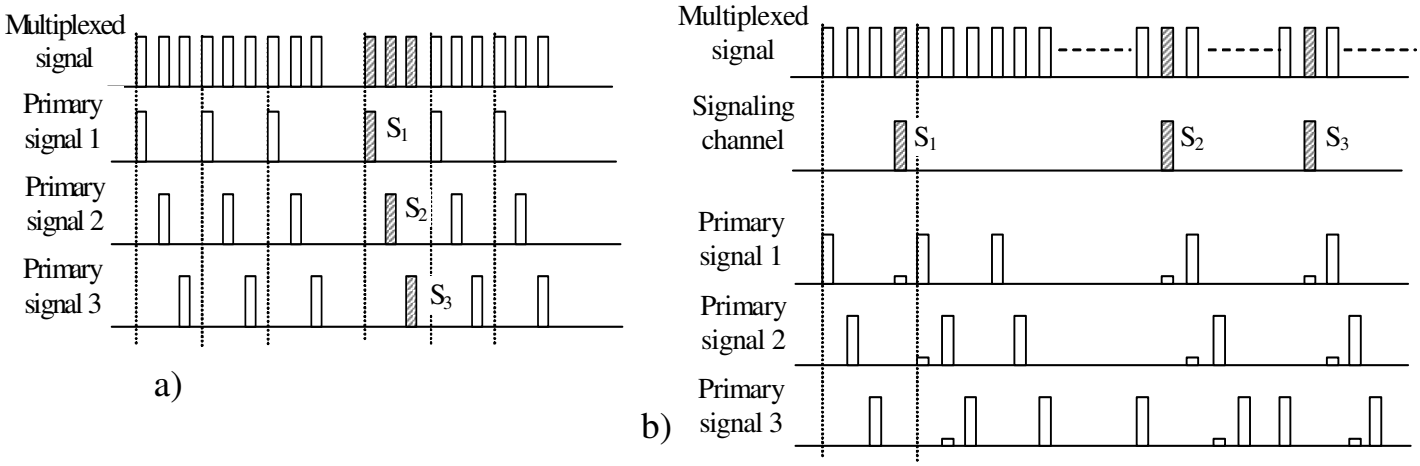

Fig. 9 Justification signaling insertion a) individual insertion; b) common insertion

- The information related to the signaling commands is very important for the functioning of the multiplexing equipments;

- if this information is erroneous other bits than the justification bits will be extracted, fact which will lead to de-synchronizations → redundant coding of the signaling information and error correction of the signaling bits is used –repetition codes are used usually (these bits are transmitted several times and the correct bits are decided based on a majority logic).

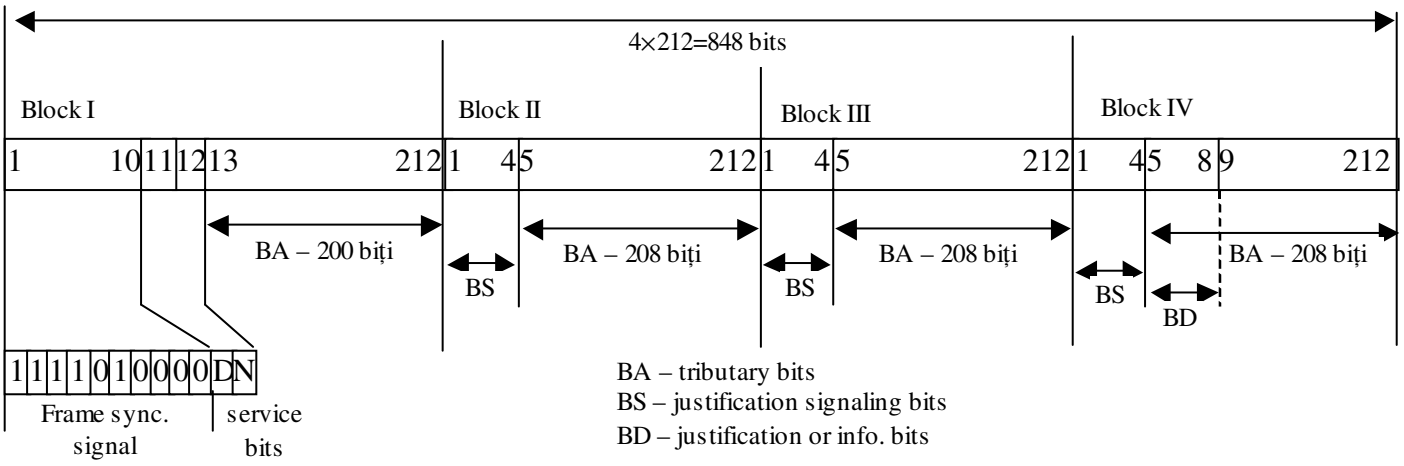

Fig. 10.1 Structure of the secondary PDH frame

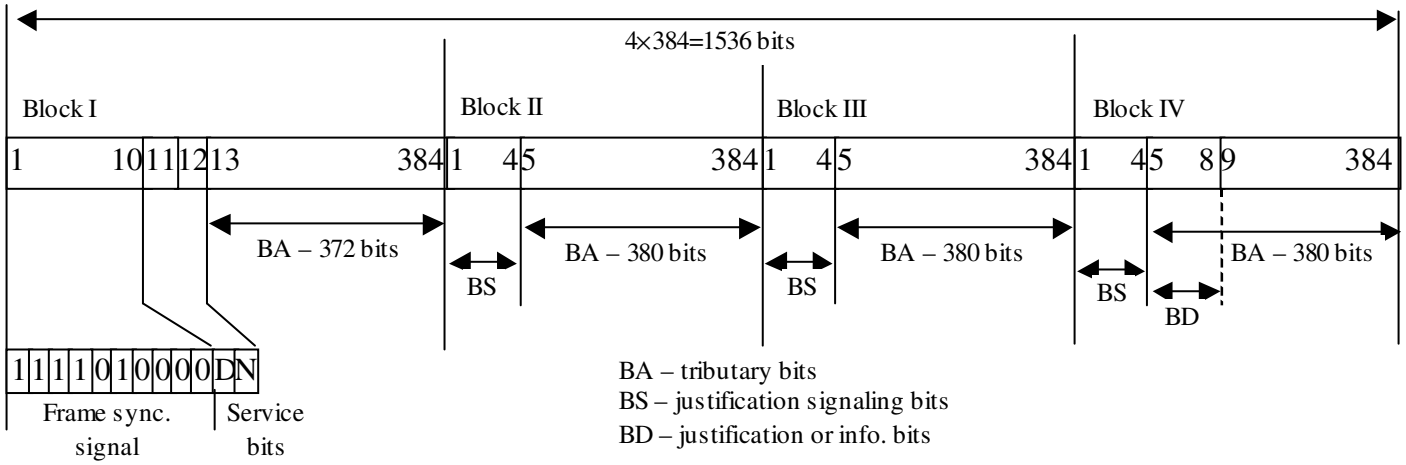

Fig. 10.2 Structure of the tertiary PDH frame

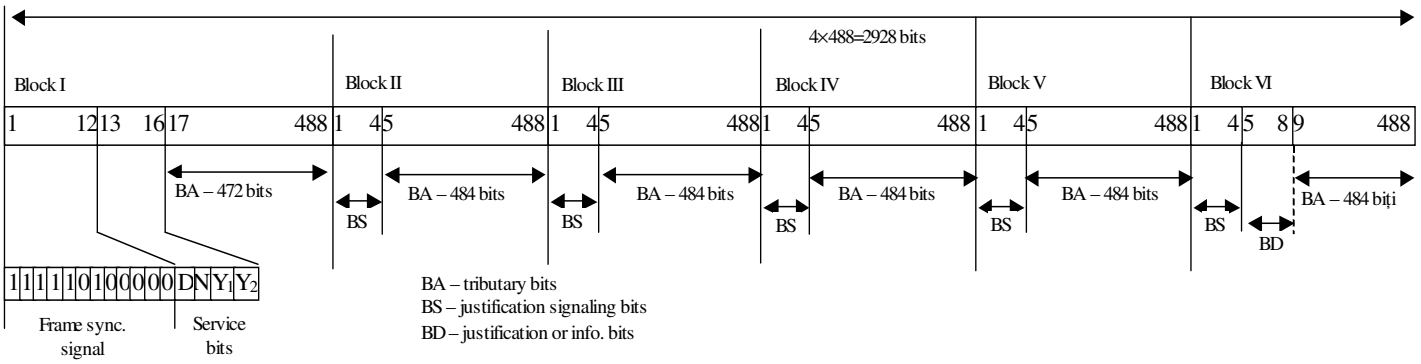

Fig. 10.3 Structure of the quaternary PDH frame

- Let be N_0 the total number of symbols of a transmission frame, N_s, the number of synchronization symbols, n_0, the number of information symbols – results: $n_0 = N_0 - N_s$; $\eta = \frac{n_0}{N_0}$ (1) , where η is the information efficiency;

  - if f_s is the frequency of the locally generated clock with f_{sn} nominal value and f_{pn} is the nominal value of the tributary signal rate (the nominal frequency of the writing clock), then the nominal reading frequency of the elastic memory is f_{sn}', and the mean justification frequency is f_d:

$$f_{sn}' = \eta \cdot f_{sn} \; ; \; f_d = f_{sn}' - f_{pn} > 0 \; ; \; f_{d\max} = \frac{f_{sn}}{N_0} \qquad (2)$$

  - f_{dmax} is the maximum justification frequency obtained when the reading frequency attains the maximum permitted limit, and the writing frequency, the minimum permitted limit.
  - Justification signaling $c_1c_2c_3$ =1 1 1, absence of justification $c_1c_2c_3$ = 0 0 0

- **PDH multiplexing hierarchy**

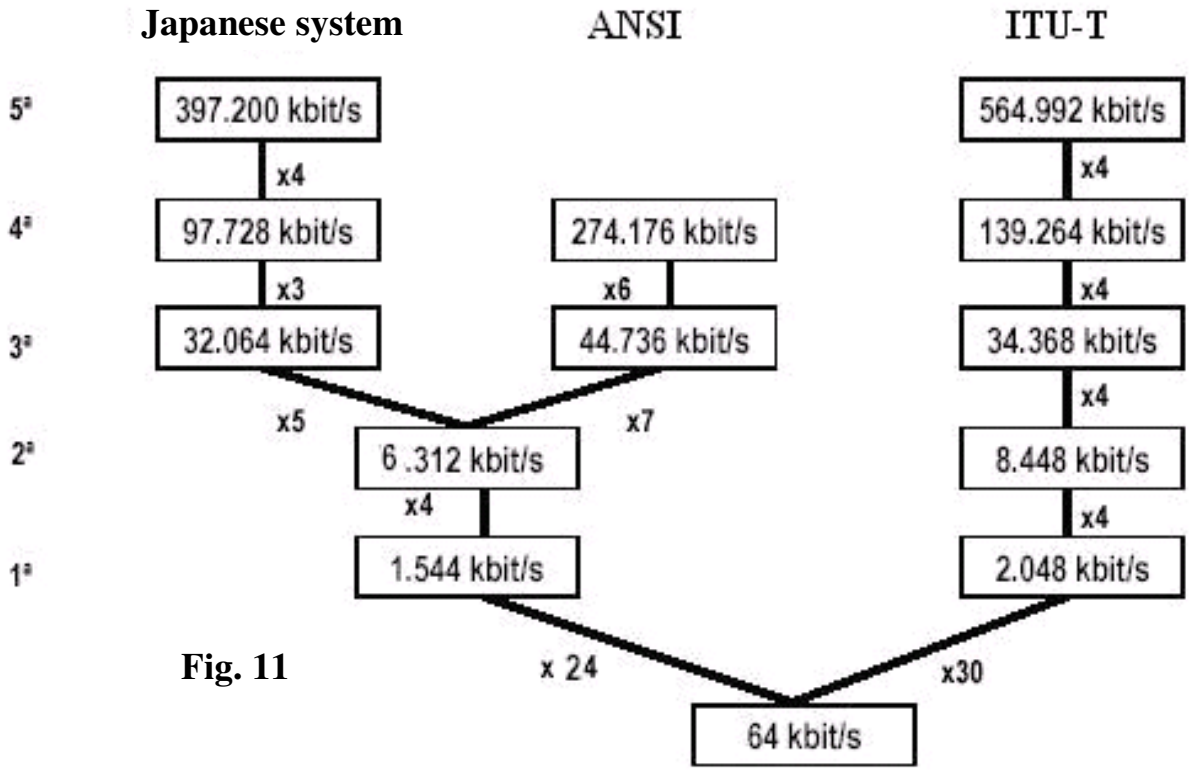

Fig. 11

- Disadvantages of PDH systems:
  - limited management and reconfiguration capabilities
  - low flexibility ; designed only for circuit switching (voice transmission) - relatively difficult to use this system for other services (for example high speed packet data)
  - the insertion and extraction of a basic data stream requires the demultiplexig – remultiplexing of the entire multiplex signal – i.e. the insertion / extraction of a 2Mbps data stream in / from a 140Mbps multiplex signal

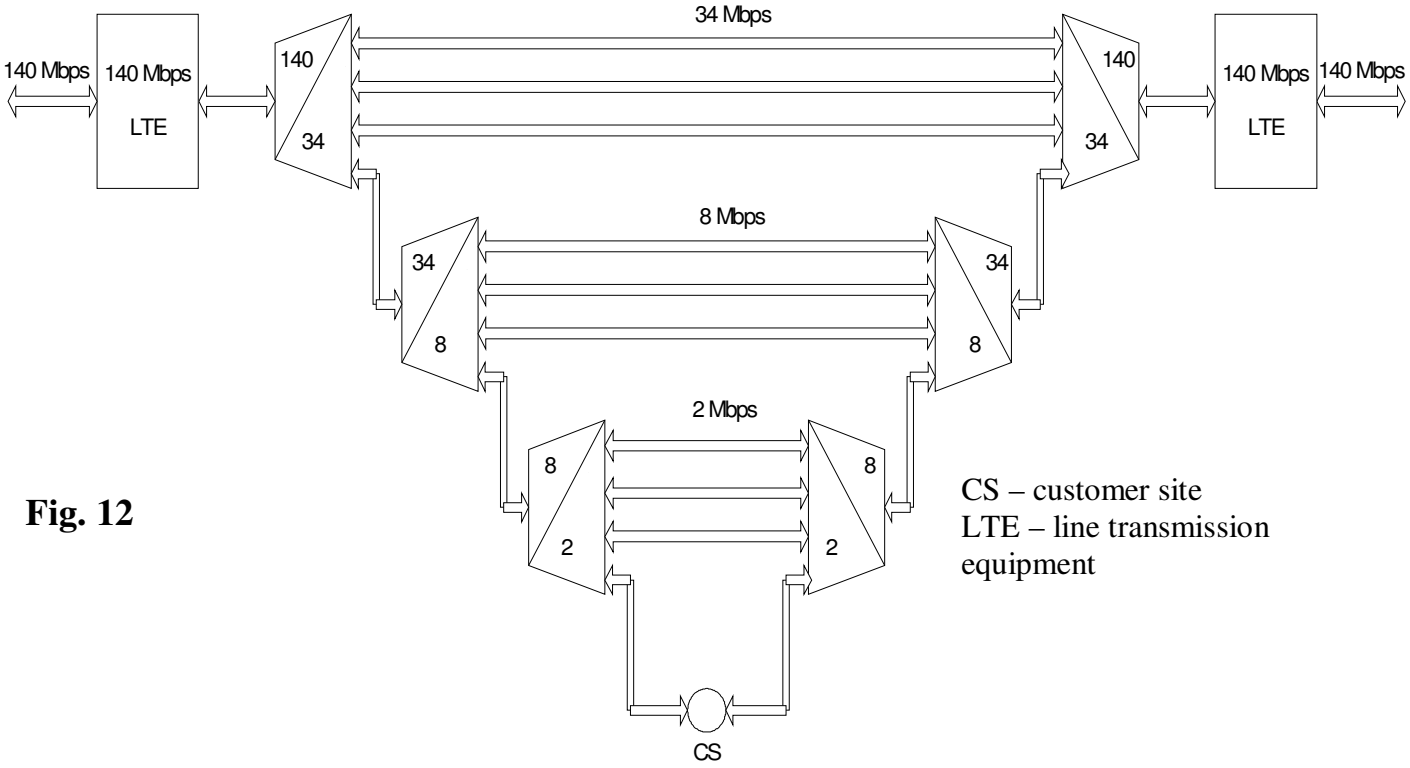

Fig. 12

CS – customer site
LTE – line transmission equipment

- **Frame synchronization**
  - in transmission systems with time division multiplexing it is necessary the identification at the reception of the multiplexing order of the involved tributaries; it is necessary also the identification of the first bit of the frame;
    - in multiplexed digital signal it is inserted a special code group named synchronization group, relatively to which is defined the order of the multiplexed tributaries;
    - the process by which is achieved the alignment between the transmission and reception side of a digital transmission system, by which is maintained and restored the alignment, in the case of losing this, it is called *cyclic or group synchronization*;
    - in some situations could be necessary the use of two levels of synchronization, namely: word synchronization and frame synchronization (it is characteristic for the primary PCM multiplex).

- Cyclic synchronization is achieved by increasing the redundancy of the transmitted signal by the insertion of the synchronization group;
- conditions imposed to the synchronization sequence:
  - the synchronization group must be chosen in such a way to reduce as much as possible the simulations (of this sequence) by the transmitted data;
  - the recognition (detection) probability of these sequences must be high in the presence of bit errors;
- There are two types of allocation methods of the synchronization sequence, namely: distributed allocation and concentrated allocation;
  - the choice of a given method depends on the technological complexity, error performances and the synchronization time;
    - the first type is proper for channels with high level of bit errors - especially the case of error packets $\Rightarrow$ the synchronization is reestablished faster (after the loss of this) in the presence of packet errors; the complexity of the method is higher; for low error probability the synchronization time is larger.
    - the second type is more sensitive to bit errors – especially to packet errors, but the complexity of the method is lower and the synchronization time is lower for low error probability.

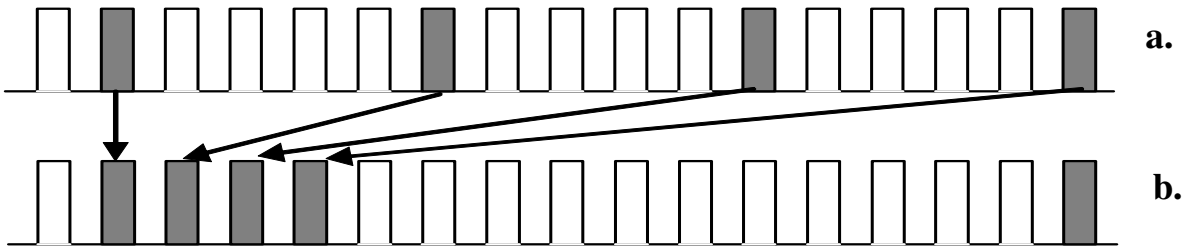

Fig. 13 Allocation methods of the synchronization sequence (group)
a) distributed allocation ; b) concentrated allocation

- The synchronization devices must fulfill the following requirements:
  - synchronization time at the connection establishment and after the loss of synchronization (generically called synchronization search time) as small as possible;
  - minimum synchronization information in a frame in the condition of an acceptable synchronization search time;
  - the detection probability of the synchronization signal must be high in the situation of bit errors – the time between two losses of the synchronization must be as large as possible;
  - synchronization equipment simple as possible and reliable as possible;
- The synchronization device at the reception side has the following functions:
  - establishment of the synchronization at the beginning of the transmission;
  - control of the synchronization state during the transmission;
  - identification of the states when the synchronization is missing;
  - reestablishment of the synchronization after the loss of this;

- The structure and the position of the synchronization device inside the receiver is presented in fig. 14; three blocks can be identified with the following functions:

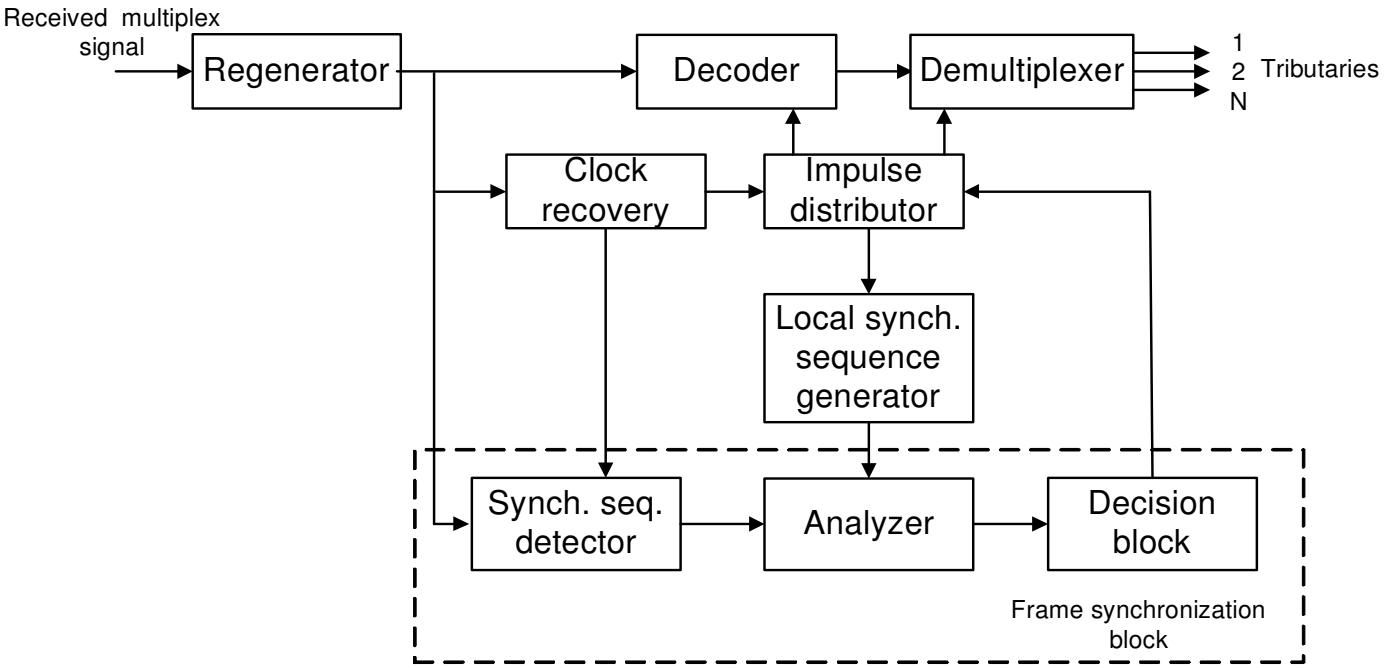

Fig. 14 Block schematics of the cyclic synchronization circuit and the position of the circuit inside the receiver

- Three blocks can be identified with the following functions:
  - **The detector** of the synchronization group evaluates the received digital signal, separating the code groups (groups of information bits) having similar structure with the synchronization group;
    - the synchronization group is separated based on the maximum correlation between the received signal and the synchronization group generated in the detector;
      - it is possible to do a serial evaluation – bit by bit processing, it is simple to implement – or a parallel evaluation – storage of a transmission cycle and processing after that;
      - the detector can extract code groups which are not the synchronization group – simulations (of the synchronization group) produced by the transmitted bits, having a probabilistic appearance; the decrease of the number of false synchronizations is achieved by other blocks of the synchronization device;

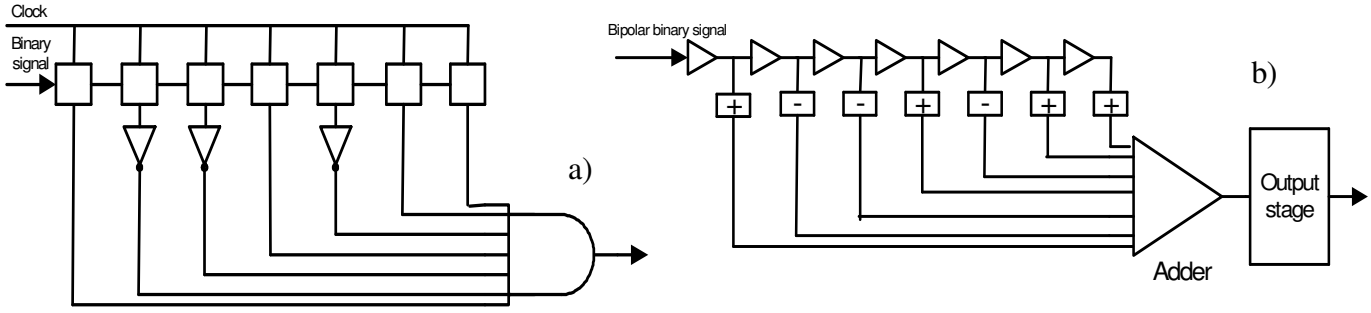

Fig. 15 Possible block schematics of the synchronization group detector circuit
a) digital implementation ; b) analog implementation

- **The analyzer** – compares the synchronization group extracted from the received signal with the locally generated synchronization group; takes decisions on the correspondence between the two signals according to the following criterions:
  - the repetition period, necessary to verify if the synchronization group is a real one or it is a simulation by the information signal;
  - the apparition time of the synchronization group - it is verified if the local synchronization group appears simultaneously whit the extracted synchronization group;
    - the analyzer output signal – error or no synchronization error – reflects the two enunciated criterions.
- **The decision circuit** – takes decisions on the analyzer output according to a criteria named *synchronization strategy*;
  - using the generated command signal the system pass through the states of synchronism search, synchronism verification and synchronism;

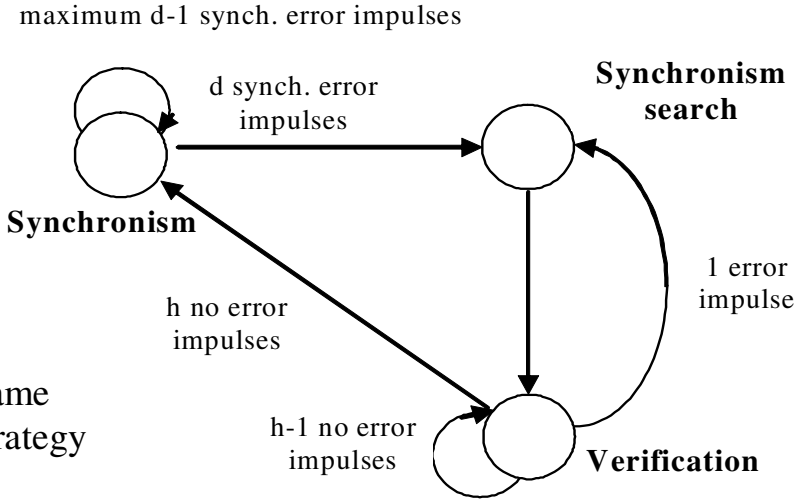

Fig. 16 General frame synchronization strategy

Cyclic synchronization methods

- **Cyclic synchronization by delay of the clock impulses**
  - in the synchronism state the signal obtained at the output of the synchronization group detector appears in the same moment and with the same periodicity as the local synchronization group – the decision circuit allows the passing of the clock to the impulse distributor;
  - in the synchronism searching state - the analyzer input signals do not satisfy the periodicity and apparition time conditions - an interdiction signal is generated by the decision circuit (in the apparition moment of the locally generated synchronization group) which blocks the gate circuit (and the clock access to the impulse distributor) a clock period $\Rightarrow$ the cycle of the local impulse distributor is extended with 1 bit period – the searching process keeps going until the synchronism state is decided by the analyzer;
  - very low probability of false synchronization but very high synchronization time;

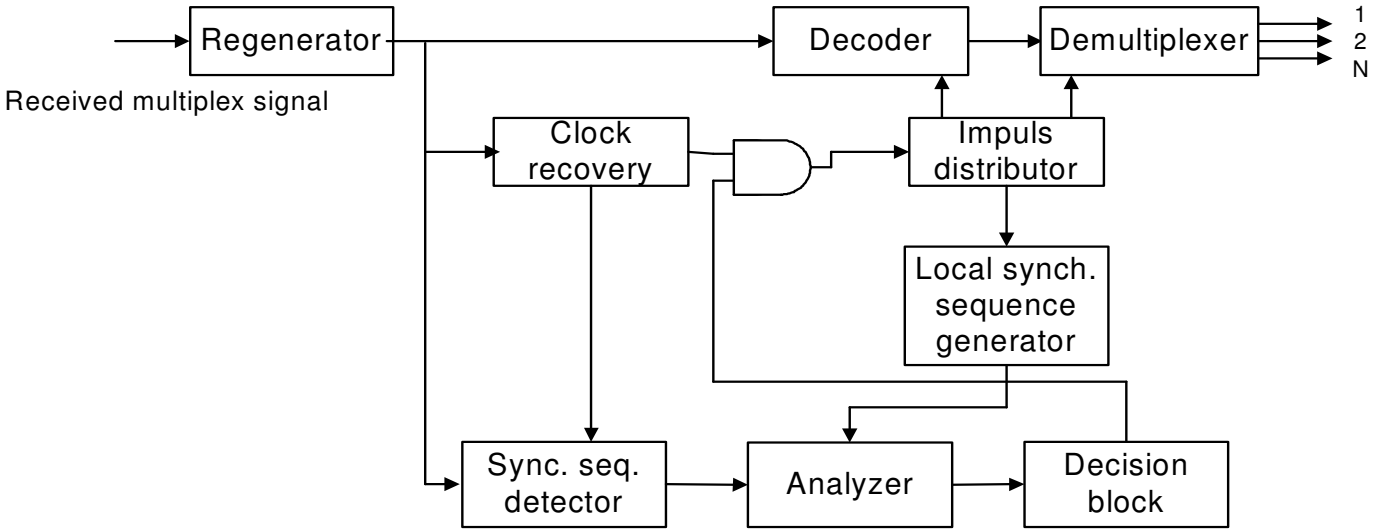

Fig. 17 Block schematic of the cyclic synchronization circuit based on the impulse delay method

- In fig. 18 it is presented the synchronism searching algorithm in the case of cyclic synchronization based on delay of the clock impulses; there are two types of cycles:

❖ Extended cycles specific to normal functioning in searching state, cycles with a T_c+T_b duration – by these cycles it is decreased the time difference between the received and the local synchronization group with one clock period at every moment, when the local synchronization group is applied to the analyzer;

❖ Supplementary cycles due to the apparition of false synchronization groups in the received signal, groups detected by the synchronization group detector – slow down the synchronization search process;

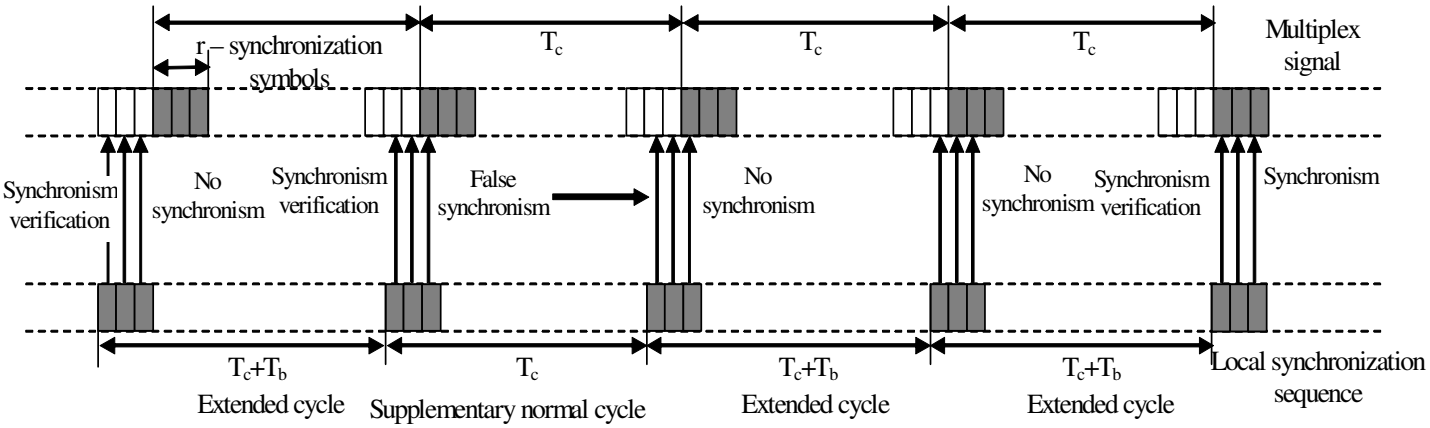

Fig. 18 Functioning principle of cyclic synchronization algorithm based on delay of the clock impulses

- **Cyclic synchronization by sliding** – ensures a substantial increase of synchronization speed; it is not generated a local synchronization sequence, the detection moment of the received synchronization group is compared with the state of the decoder and demultiplexer impulse distributor – see fig. 19 - the block schematic of the frame synchronization circuit; the probability of false synchronizations is higher relatively to the method based on delay of the clock impulses.

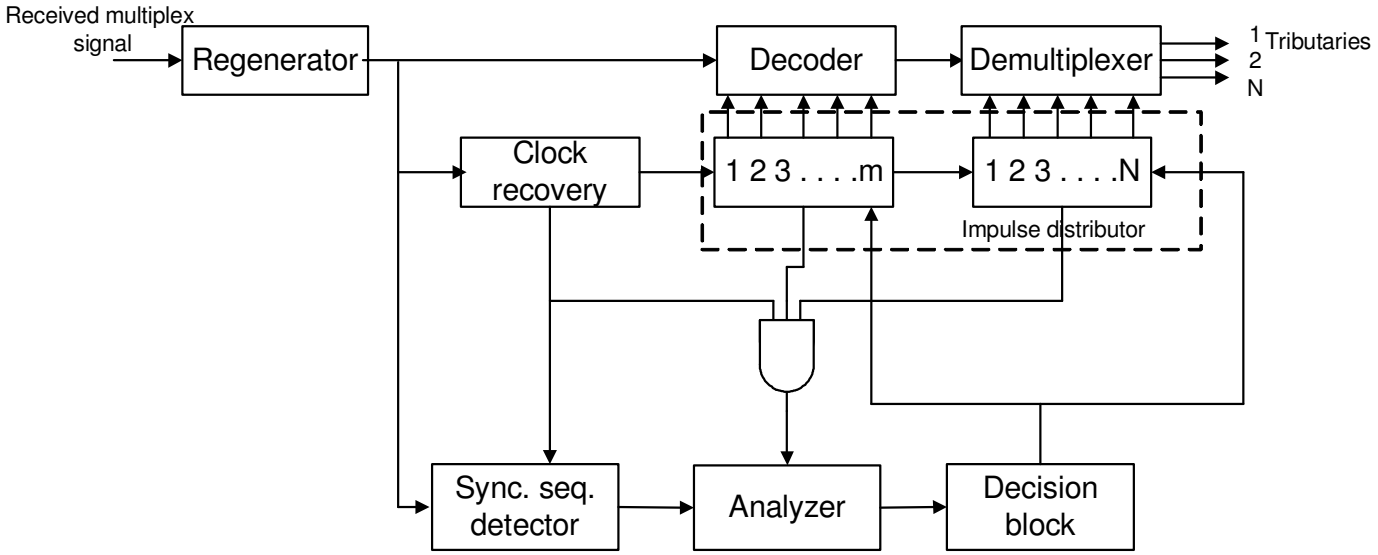

Fig. 19 Block schematic of the cyclic synchronization circuit based on the sliding method

- ❖ in the synchronism state the impulse from the AND gate, obtained by the coincidence between the clock impulse, impulse **m** of the decoder impulse distributor and the impulse **N** of demultiplexer impulse distributor is in phase with the impulse generated by the synchronization group detector;
- ❖ the loss of the synchronization means the absence of the coincidence between impulses at the output of the AND circuit and the synchronization group detector – in synchronism search state it is generated a restart command of the impulse distributors at each detection of the synchronization group → the impulse distributors are forced in synchronism position;
- ❖ in synchronism state false synchronizations could appear only due to bit errors in the received signal;
  - around the synchronization group of length r, appears a region of length r-1, where it is verified both the information signal and the synchronization group – this is the region more exposed to false detection of the synchronization group – zone is called coverage zone and has a major importance in choosing the synchronization group structure.

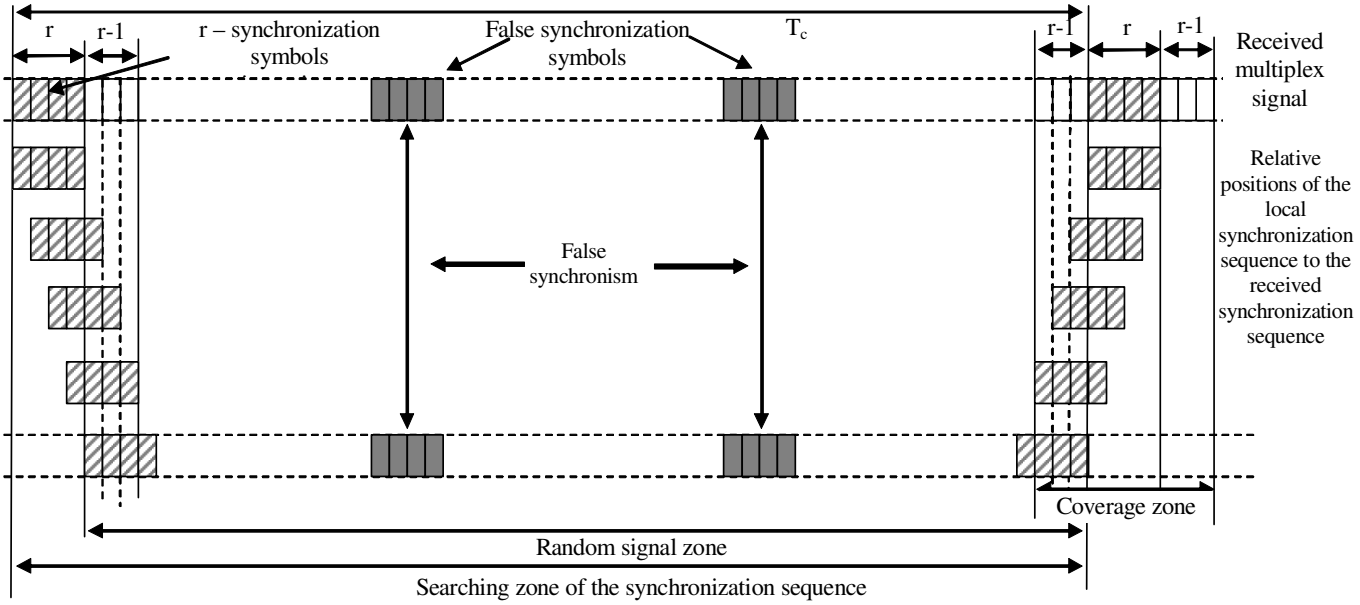

Fig. 20 Functioning principle of cyclic synchronization algorithm based on sliding

- The notion of jitter differs very much in the case of analog and digital systems;

❖ in the case of analog systems the jitter is due to the frequency multiplexing systems and it represents a parasitic phase modulation characterized by a given amplitude (maximum value of the phase deviation) and by a given frequency (frequency of the phase change);

❖ in the case of digital systems the jitter means the modification of the significant moments of the digital signal relatively to their ideal position; there are significant differences between the causes which induce jitter in the two type of system; in digital systems the jitter has two variants namely:

- short time variations of the significant moments – this phenomenon is called effectively jitter.
- long time phase variations – the „wander" phenomenon – they are slow variations of the significant moments of the digital signal relatively to the ideal position; the difference between the two type of phase variations is connected only to the frequency range – does not exist a clear definition of the frequency limit between jitter and wander; as a rule of thumb, phase variations with frequency below 10Hz are called wander.

o The jitter phenomenon can be observed at the output of any digital section when at the opposite side is applied a digital signal; it can be observed on an oscilloscope synchronized with the recovered clock (fig. 21)

Fig. 21 Jitter phenomenon, which can be observed at the output of digital sections

o The digital signal before regeneration is characterized by the modifications of the bit edges relatively to the ideal position, having as reference the clock signal;

- if the clock signal does not present any jitter, then the regeneration process by sampling at the middle of the signal elements might ensure a jitter free recovery of the digital signal (see fig. 22).

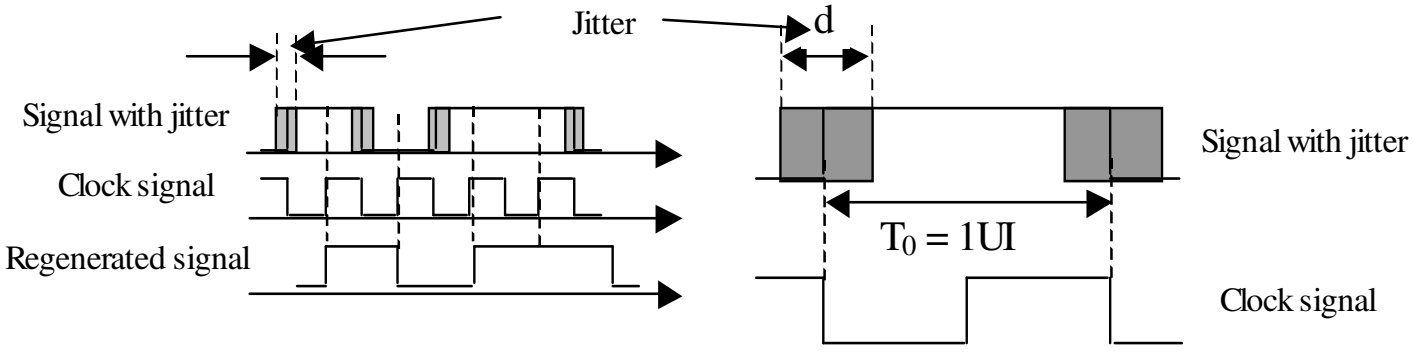

Fig. 22 Suppression of the jitter by ideal regeneration – fig. a ; Definition of the jitter peak to peak value – fig. b

o The maximum peak to peak trip of the signal transitions before regeneration is equal with the duration T_0 of a signal element, called unit interval UI (Unit Interval);

- The overrun of this value leads to erroneous decisions; the peak to peak amplitude of the jitter can be expressed also in percents;
- The use of the unit interval for jitter and wander evaluation makes this evaluation independent of the binary rate and of the shape of the transmitted impulses (NRZ or RZ);
- Must be noticed that in data transmissions to the jitter term corresponds the usual term of total telegraphic distortion, expressed in percents; the two phenomenon's have a common connotation.
- The tolerance to the jitter, meaning the maximum value of the jitter which does not induce erroneous decisions differs according to the frequency in the following way:
  - at low frequencies it is possible to exceed the limit of 1 UI without the apparition of erroneous decisions, because the recovered clock absorbs almost completely this jitter, following the slow phase variations of the received signal and making a correct sampling; so in this case the system can tolerate a phase variation higher than 1 UI (even much higher);
  - the described aspect results from the property of the clock recovery devices – these devices have a low pass type transfer characteristic according to the frequency –low frequency jitter components appear in the regenerated signal;
  - at high frequencies of the jitter, the recovered clock (from the digital signal) cannot follow the jitter and the peak-to-peak amplitude of this cannot exceed 1 UI, being in reality fractions of UI.
- The effects of the jitter and wander consist in the following:
  - it is modified (decreased) the reserve of the digital transmissions to other imperfections of the channel (for ex. noise).
  - exceeding a given limit induces a significant increase of the error probability on digital sections; this effect is reflected in voice channels as impulse noise and background noise.
  - the apparition of an analog jitter in the analog voice channel; this appears in the D/A conversion process on PCM systems due to the jitter affecting the clock, jitter which is transmitted as a parasitic position modulation to the impulses with amplitude modulation obtained after the D/A converter.

- The jitter can be classified as:

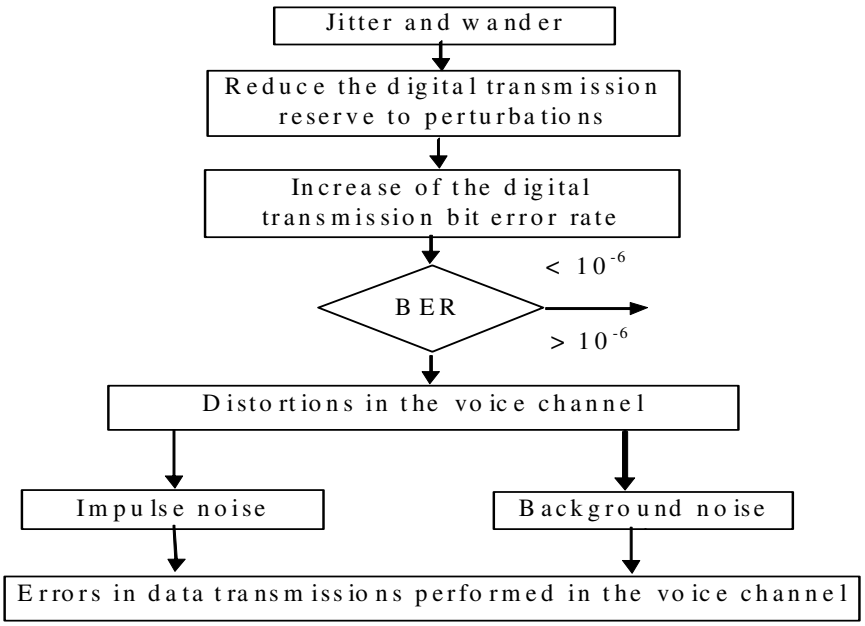

Fig. 23 Effects of the jitter and of the wander on voice and data transmissions realized in the telephone channel

- Systematic variations – phase variations dependent on the structure of the digital signal („pattern-dependent variations"); these phase variations appear due to several identical and correlated interconnected digital units; the effect is pronounced cumulative.
- Non-systematic variations – this type of jitter supposes the absence or low correlation degree of different jitter sources; these variations has a stochastic (or semi-stochastic) character and do not depend on the transmitted digital sequence („pattern-independent variations"); this type of jitter has a low influence on the quality of transmission.

- **Origin of the jitter**

- There are several jitter sources, the most representatives being the followings:

- **The digital regenerator** – a regenerator reconstructs the received digital signal at the input using a clock signal extracted from the received signal (see fig. 24);

  - due to the imperfect recovery this clock signal is affected by a parasitic phase modulation which is integrally transmitted to the regenerated signal as a jitter;

  - in the regeneration process each regenerator distorts the clock signal and through this induces jitter in the output signal – this jitter is added, afterwards with the jitter generated in other units of the regenerator chain.

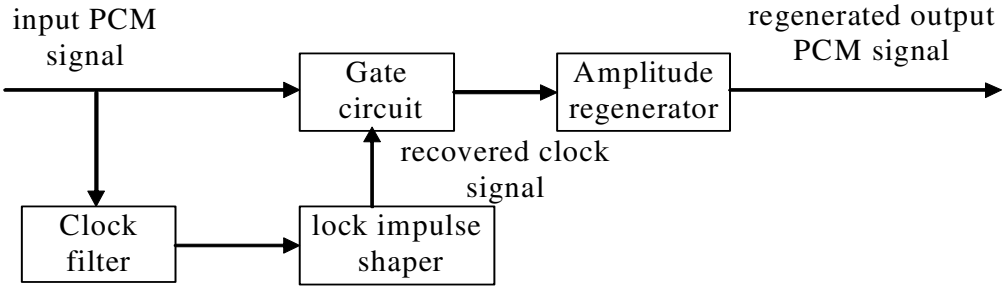

Fig. 24 Principle schematic of a regenerator and the basic idea of digital signal regeneration

- The sources generating the jitter at the output of a regenerator are dependent especially of the structure of input signal sequence; in the case of an ideal regenerator the signal diagram does not have any effect on the phase of the clock signal, but the regeneration takes place in the presence of some imperfections.

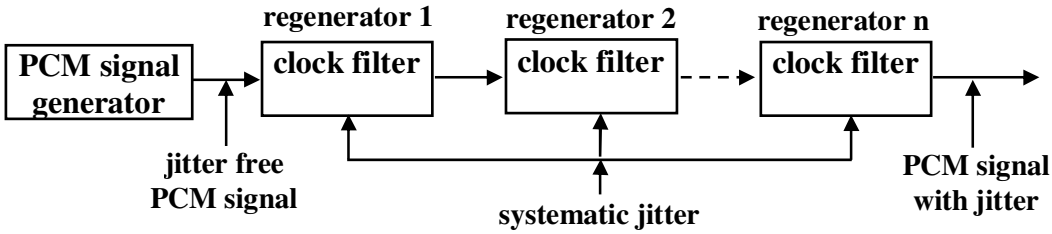

Fig. 25 Jitter accumulation on a regenerator chain

- **The justification (stuffing) process** – the jitter associated to the justification (stuffing) process appears at the output of the multiplexing equipments of superior order, when the multiplexing process operates on several plesiochronous tributaries;
- The mentioned jitter is considered composed of two jitter components, namely:
  - ❖ justification jitter present when the justification process can appear immediately at request;
  - ❖ waiting jitter which is defined as a low frequency jitter, because it is related to the waiting time between the justification request and the completion of this request;
  - ❖ due to the fact that the two definitions are connected and hard to separate it can be accepted a single notion, that of waiting jitter (see fig. 7 and 8).
- **The wander** – can appear due to several reasons, the most importants being: modification of the transmission medium characteristics, variations of the frequency of the clock generators of network nodes (see fig. 26)

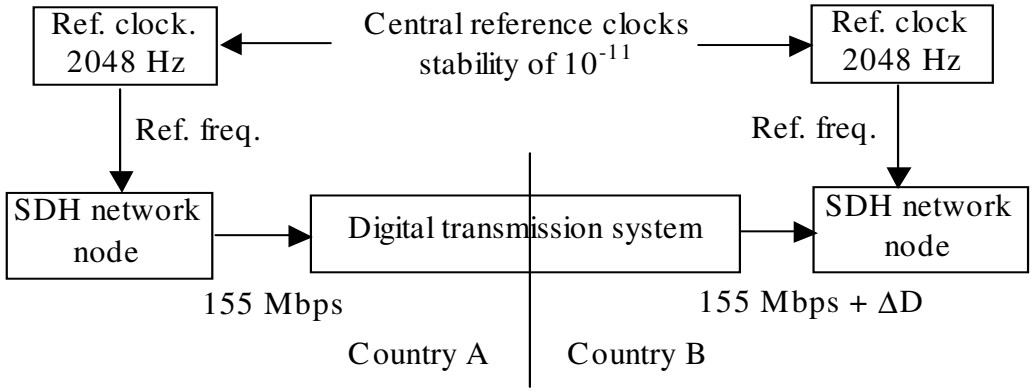

Fig. 26 The „wander" phenomenon

- **Accumulation of the jitter in digital networks** – two situations are considered, namely:
  - Cascaded chain of regenerators: the jitter character is preponderantly systematic (dependent on the digital signal sequence) the main cause being the imperfections of the clock recovery circuits;

- the jitter transfer function between the input and the output of a regenerator is a LPF type and is given by the expression: $C(s)=\frac{1}{1+B\cdot s}$ (3), where s=jω , B=ω_0/2Q is the half of the clock extracting filter bandwidth.

- Random accumulation of the jitter on a regenerator chain: non-correlated sources (i.e. random noise); the summation law is: $J_N = J_1 \cdot \sqrt[4]{N}$ (4), where J_1 is the effective value of the jitter generated by each regenerator, J_N is the global effective value of the jitter; minor importance.

- Systematic jitter accumulation generated on a chain of regenerator: correlated sources (dependent on the bit sequence), summation law of the systematic jitter: $J_N = J_1 \cdot \sqrt{2N}$ (5), where J_1 is the effective value of the jitter generated by each regenerator; the values of J_1 are situated usually in the 0,4 – 1,5% UI range;

  - if PLL loops are used the summation law is: $J_N = J_1 \cdot \sqrt{2NA}$ (6), where A is a factor dependent on the number of regenerators and on the PLL loop characteristics;

  - major importance; probabilistic distribution of the jitter amplitude close to the Gaussian distribution; a ratio of peak to peak value / effective value of 12 – 15 is usual and corresponds to a low probability of exceeding the peak value.

- Jitter decreasing methods on a regenerator chain: the use in regenerators of transformation devices which operate on the signal sequence (for ex. pseudo-random sequences, scramblers, addition of the signal with his own delayed version);

  - another possible solution is the use of buffer memories in regenerators, memories which absorb the sudden variations of the regenerated clock (see fig. 27) (the devices which decrease the jitter level are called „jitter reducers" or "jitter compensators"); the transmit clock is controlled by the filling level of the buffer memory.

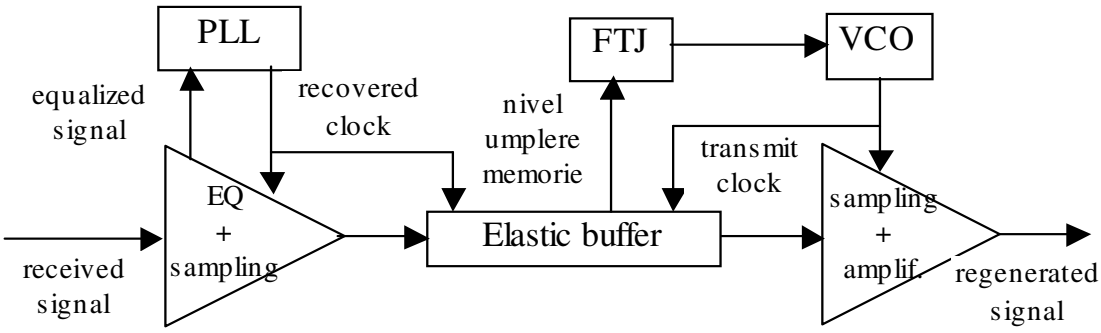

Fig. 27 Regenerator equipped with jitter compensator

- The jitter accumulation in the case of alternate transmission of two signal diagrams: the effect is the apparition of a low frequency jitter proportional with the number of regenerators, the peak value being given by: $J = d \cdot N$ (7), where d is the jitter generated by a single regenerator in the given situation; this solution is not used in general in practice.

- **Jitter accumulation in systems which contain scrambler and jitter compensator**
  - Systems which contain scrambler and descrambler devices – this regenerators act as uncorrelated jitter sources; the summation law is: $J_M = J_S \cdot \sqrt[4]{K \cdot M}$ (8), where J_S is the effective jitter of a system, K is a constant with values located between 1 and 2 (K=2 for M high), M is the number of regenerators.
  - Systems which contain scrambler/descrambler and jitter reducer devices – it is valid the previous relation with the remark that J_S is small.
- **Jitter accumulation due to the multiplexing – demultiplexing equipments**
  - Appears an accumulation of the waiting jitter; the effective value of the accumulated jitter J_M according to the individual equipments jitter, J_S, and the number of multiplexing equipments is given by: $J_S \cdot \sqrt[4]{N} \le J_M \le J_S \cdot \sqrt{N}$ (9)
- **Jitter performances which defines the quality of the digital networks**
  - Jitter limits (see table 1)

Jitter type → / Bit rate (kbps) ↓	Jitter measured in large band		Jitter measured in narrow band	
	Peak to peak maximum value in UI	Measurement frequency band	Peak to peak maximum value in UI	Measurement frequency band
64	0,25	20Hz÷20kHz	0,05	3kHz÷20kHz
2048	1,5	20Hz÷100kHz	0,2	18kHz÷100kHz
8448	1,5	20Hz÷400kHz	0,2	3kHz÷400kHz
34368	1,5	100Hz÷800kHz	0,15	10kHz÷800kHz
139264	1,5	200Hz÷3500kHz	0,075	10kHz÷3500kHz

Tab. 1 Jitter performances of plesiochronous digital transmissions with different bit rates

- Limits for wander – the wander is a slow phenomenon generated by the transmission medium characteristics and by the aging of the clock regenerators; could generate the clock slide phenomenon;
  - the MTIE (Maximum Time Interval Error) parameter is defined – the peak to peak variation of the synchronized signal delay relatively to an ideal signal (i.e. a reference clock) in time interval S (see fig. 28); for $S>10^4$s we have: $TIE = \left(10^{-2} \cdot S + 10000\right) ns$ (10);

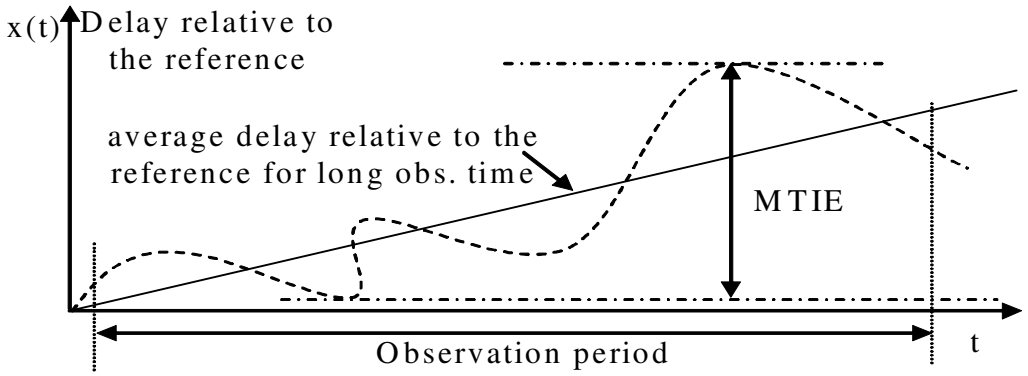

Fig. 28 Definition of the MTIE parameter associated to „wander”

- in the case of independently synchronized networks, the TIE value between the input signal and the synchronization signal of the equipment which ends the connection can exceed the maximum value imposed for the wander and it is possible to appear clock slides (generating errors) with a frequency between 1 and 70 days;

- tolerance to the jitter and to the wander of the digital equipments (see fig. 29 and tab. 2)

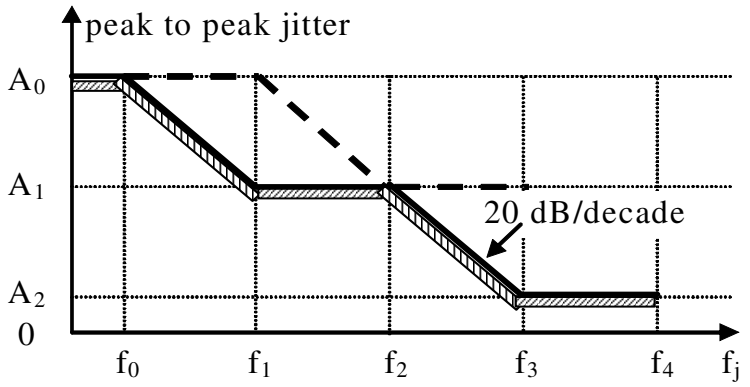

Fig. 29 Maximum allowed peak to peak values of the jitter and „wander". Peak to peak jitter – frequency characteristic

Parameter → values	Peak to peak jitter value (UI)			Frequency (Hz)				
bit rate (kbps) ↓	A_0	A_1	A_2	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_4 (kHz)	f_5 (kHz)
64	1,15	0,25	0,05	$1{,}2\times10^{-5}$	20	600	3	20
2048	36,9	1,5	0,2	$1{,}2\times10^{-5}$	20	2400 (93)	18 (0.7)	100
8448	152	1,5	0,2	$1{,}2\times10^{-5}$	20	400 (10700)	3 (80)	400
34368		1,5	0,15		100	1000	10	800
139264		1,5	0,075		200	500	10	3500

Tab. 2 Maximum allowed peak to peak values for jitter and „wander" in different frequency bands for plesiochronous digital transmissions with various bit rates

- The transfer characteristic of the jitter in the case of digital equipments – the $H(f_j)$ characteristic of the jitter, represents the ratio between the jitter at the output of an equipment and the jitter at the input, expressed in dB, according to the frequency, at a specified binary rate; in general are attenuated the jitter components situated above a given frequency – the general characteristic $H(f_j)$ is a low pass type (see fig. 30)

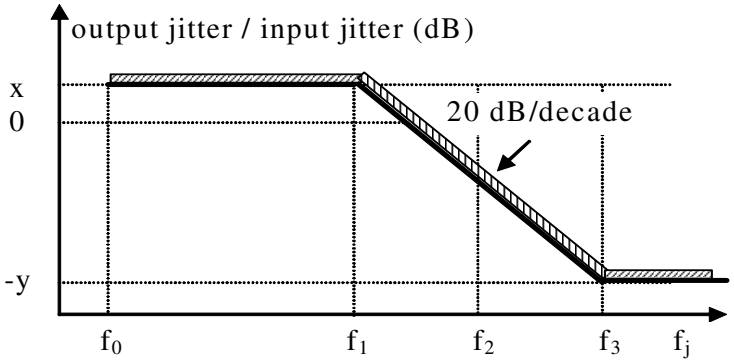

Fig. 30 Frequency transfer characteristic of the jitter

- The maximum jitter at the output of the digital equipments and the maximum jitter at the output of the digital sections.