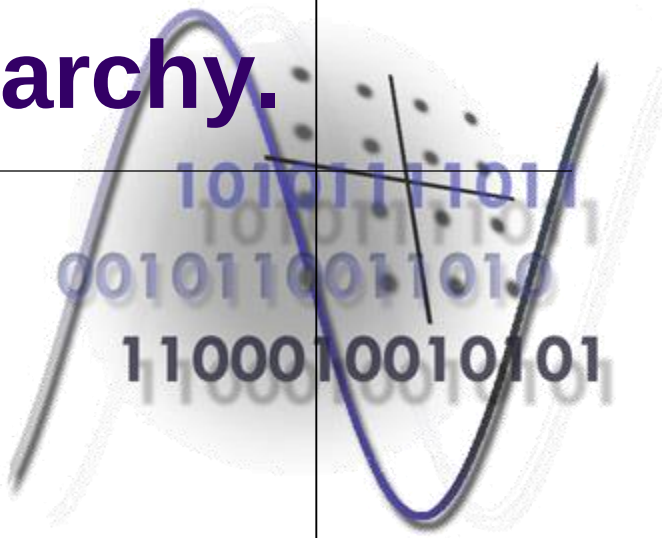
Course 10
The PDH multiplexing hierarchy.



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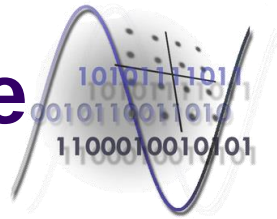
Content of the course

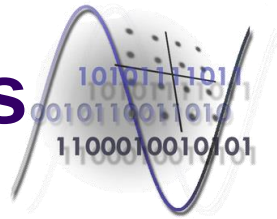


- Multiplexing of plesiochronous signals;
  - Clasification of digital signals;
  - Rate matching by justification;
  - The principle of positive justification;
  - Justification signaling insertion (multiplexing);
- The PDH multiplexing hierarchy;
  - PDH multiplexing systems;
  - PDH frame formats;
  - Disadvantages of the PDH system.
- Frame synchronization;
  - Synchronization sequence insertion methods;
  - Cyclic synchronization equipment;
  - Cyclic synchronization methods.

Multiplexing of digital signals

- Classification of digital signals from the point of view of their generation and the relation between their clock signals:
  - Isochronous signal:
    - the time interval between two significant moments is theoretically equal with a unitary time interval or with a multiple of this;
  - Anisochronous signals:
    - the time interval separating two significant moments it is not necessarily related to a unitary interval or to a multiple of this;
    - the symbols of a non-isochronous binary signal do not have the same duration.
  - Homochronous signals:
    - isochronous signals with the same rate and constant phase relation;
    - can be divided in:
      - Mesochronous signals – isochronous signals with the same rate and non-constant phase relation – constant average phase relation;
      - Synchronous signals – isochronous signals with the same rate and constant phase relation.

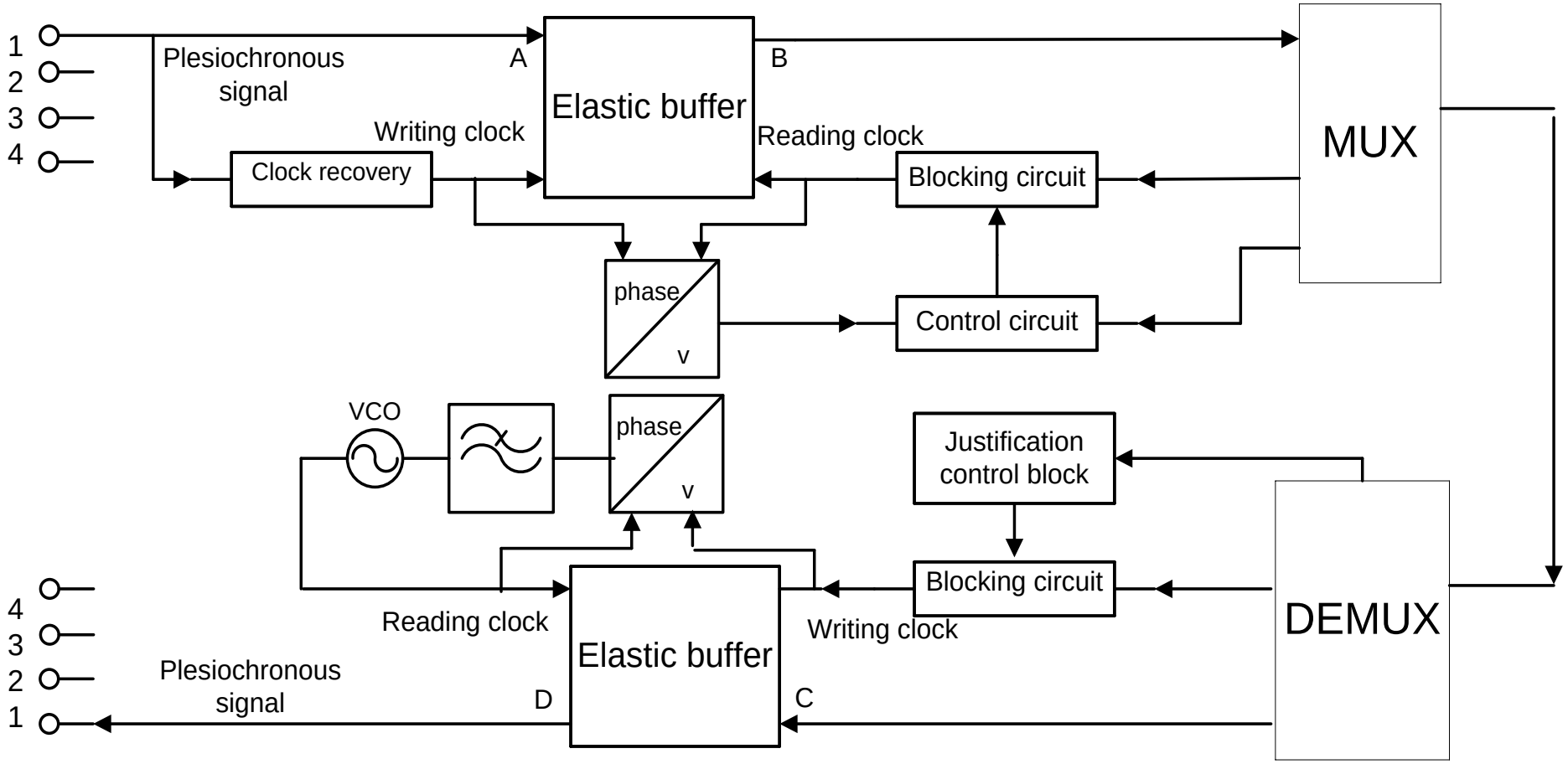
Multiplexing of digital signals



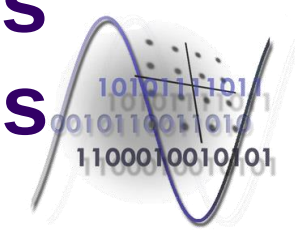
- Heterochronous signals:
  - isochronous signals with different rates and variable phase relation;
  - plesiochronous signals – signals with the same nominal rate, all the variations of this rate being maintained between specified limits;
    - for ex. signals with identical nominal rates from different sources.
- Multiplexing of plesiochronous digital signals
  - Can be achieved in two possible ways:
    - generation of signals with high stability of the clock frequency and use of some buffers;
      - very high price and periodical loss of information;
    - use of the justification (stuffing) method;
      - without information loss;

Multiplexing of plesiochronous signals

- Block schematic of PDH multiplexing – demultiplexing equipments;



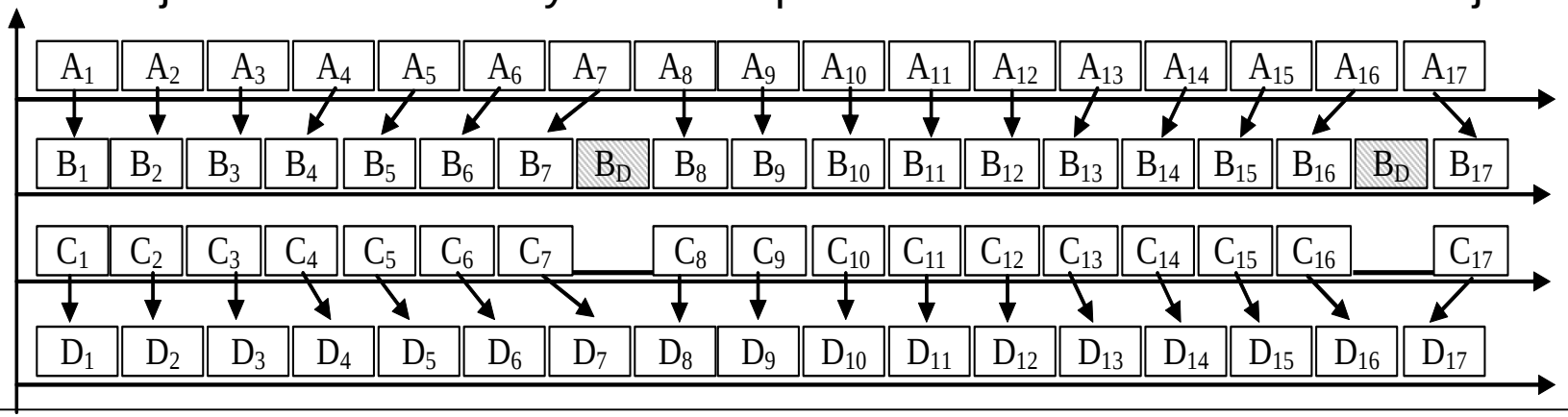
Multiplexing of plesiochronous signals



- Principle of the rate matching between the tributary and multiplexer based on positive justification;
  - The plesiochronous binary signal is written in the elastic memory with a specific clock frequency, f_i;
  - The reading of the memory and the transmission of the signal in the channel is realized with a higher clock frequency $f_o > f_i$;
    - appears a clean out tendency of the elastic/circular memory content;
    - it is detected by using a phase comparator (compares f_o and f_i);
  - When a phase difference threshold value is exceeded (between signals f_o and f_i), the phase comparator generates a blocking commands of the reading impulse;
    - it is created a break in the line signal (one stuffing impulse is inserted) which decreases the phase difference between the clock signals;
      - the stuffing impulse has no information.

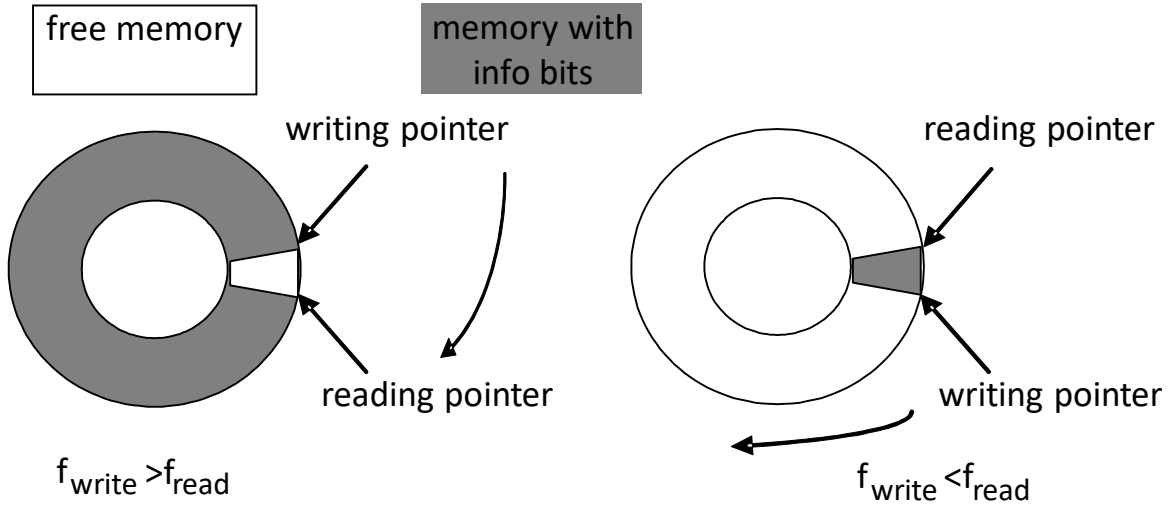
Multiplexing of plesiochronous signals

- The justification (stuffing) is signaled to the reception side on a link multiplexed with the data signal;
  - the signaling of the justification (stuffing) is necessary to inform the receiver about the exact moment and location of the justification (stuffing);
    - this information is necessary for suppression of the justification bits in the receiver;
- Only the information bits are written in the memory at the reception side with a frequency f_o, the memory being read with a frequency f_i;
- The extraction of the justification (stuffing) impulses generates a jitter in the output signal;
  - this jitter is controlled by a PLL loop which reduces the effects of the jitter.



Multiplexing of plesiochronous signals

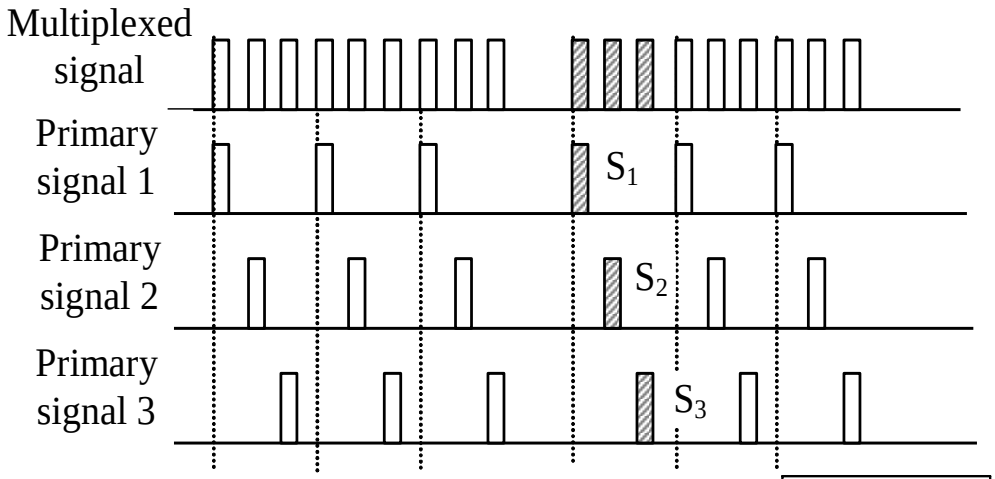
- Use of the elastic buffer for rate adaptation:

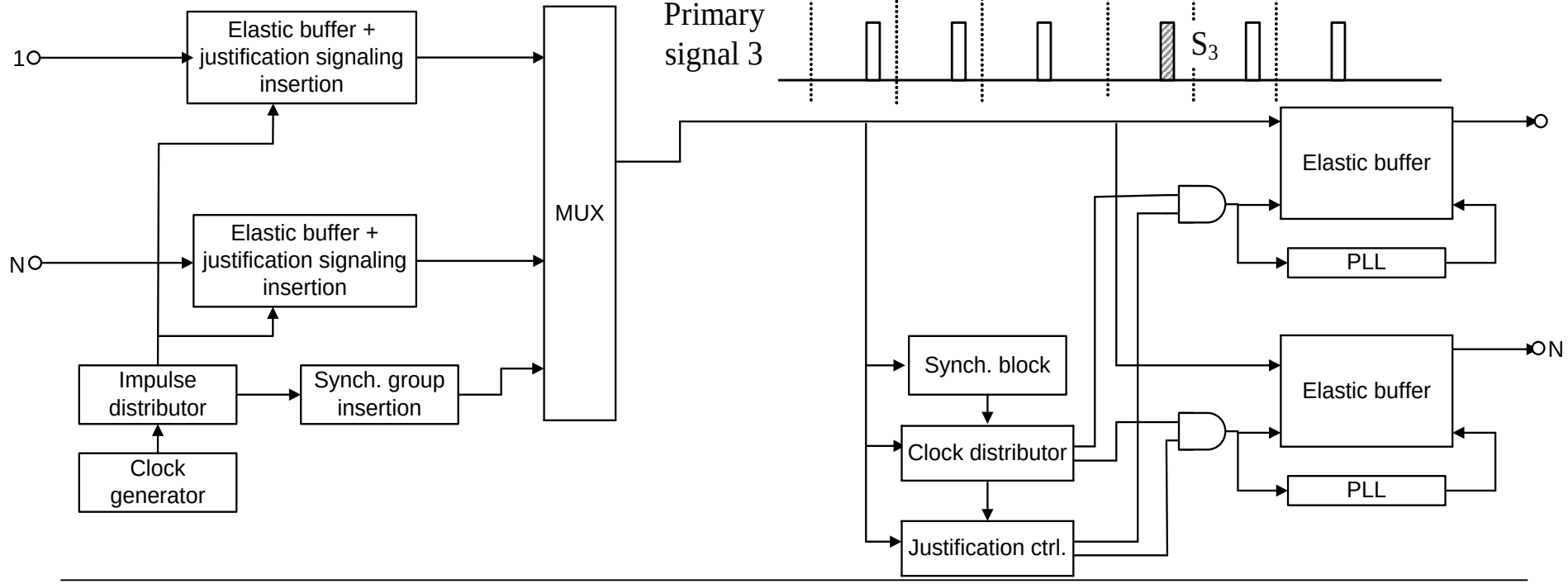


- Justification signaling insertion:
  - Individual insertion;
    - insertion of signaling justification bits is realized before multiplexing;
    - complex method at transmission; flexible and low complexity method at reception;
  - Common insertion;
    - the signaling information from all tributary signals are concentrated on a common path which is then multiplexed with data;
    - lower complexity at transmission side, but higher complexity at reception side.

Multiplexing of plesiochronous signals

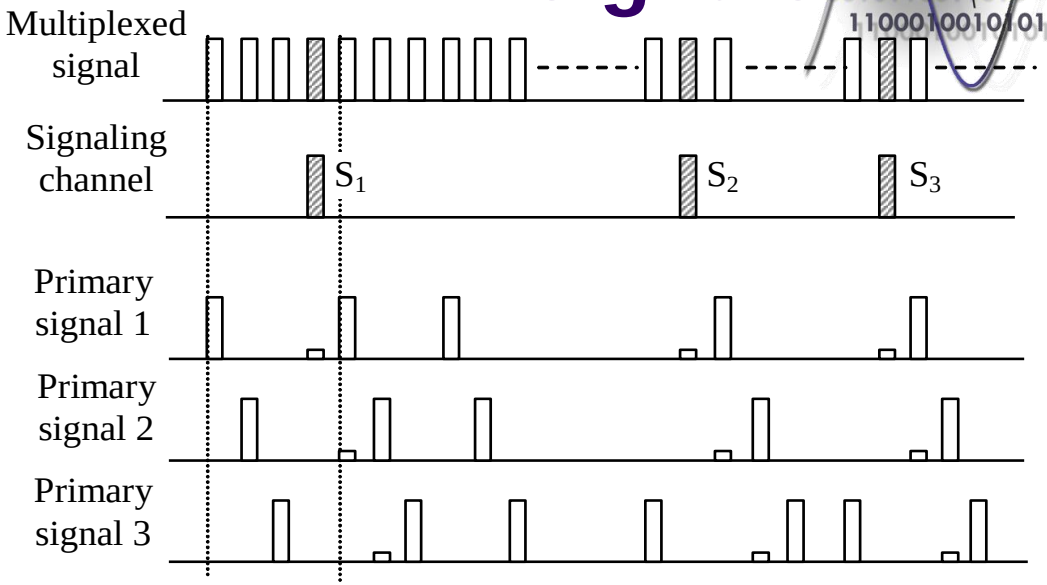
- Individual insertion of the justification signaling;
  - Signal diagram:
  - MUX and DEMUX block schematics:

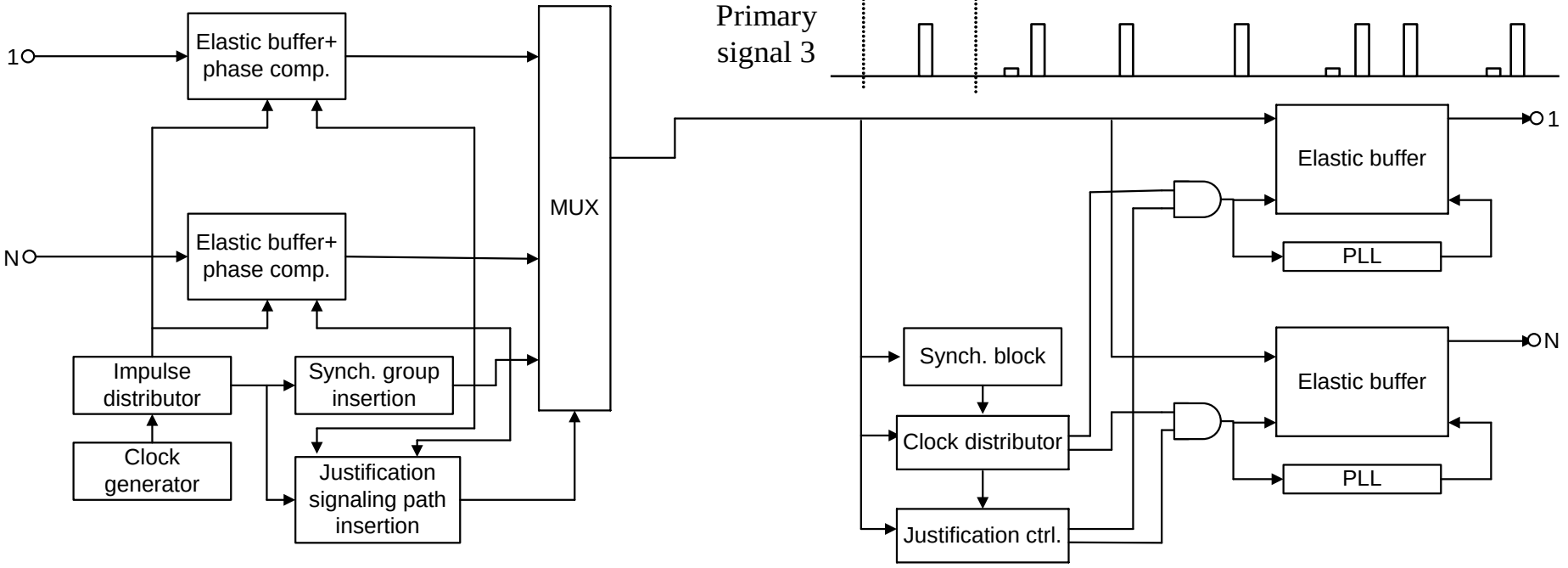




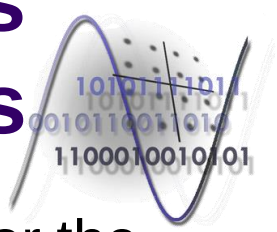
Multiplexing of plesiochronous signals

- Common insertion of the justification signaling;
  - Signal diagram:
  - MUX and DEMUX block schematics:





Multiplexing of plesiochronous signals



- The justification signaling information is very important for the functioning of the multiplexing equipments;
  - if this information is erroneous other bits than the justification bits will be extracted from the received signal;
    - this will lead to loss of synchronization;
  - redundant coding of the signaling information and error correction of the signaling bits is used;
    - repetition codes are used usually (these bits are transmitted several times and the correct bits are decided based on a majority logic);
    - for ex. justification signaling: $c_1c_2c_3$ =1 1 1; absence of justification: $c_1c_2c_3$ = 0 0 0;
    - $c_1c_2c_3$ - justification signaling bits for one tributary/source.
- Computation of the justification signaling;
  - N_0 is the total number of symbols of a transmission frame;
  - N_s is the number of synchronization symbols;
  - n_0 is the number of information symbols;
  - η is the frame efficiency.

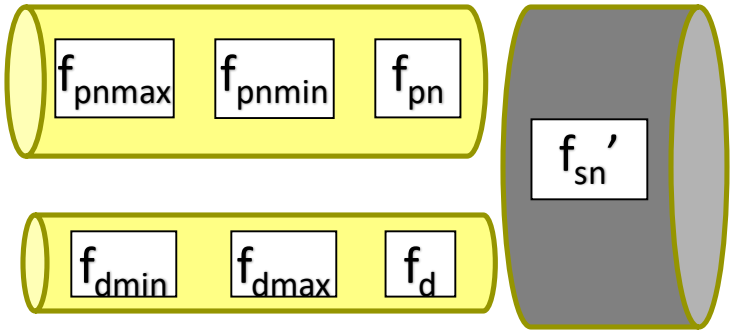
$$n_0 = N_0 - N_s \; ; \; \eta = \frac{n_0}{N_0}$$

Multiplexing of plesiochronous signals

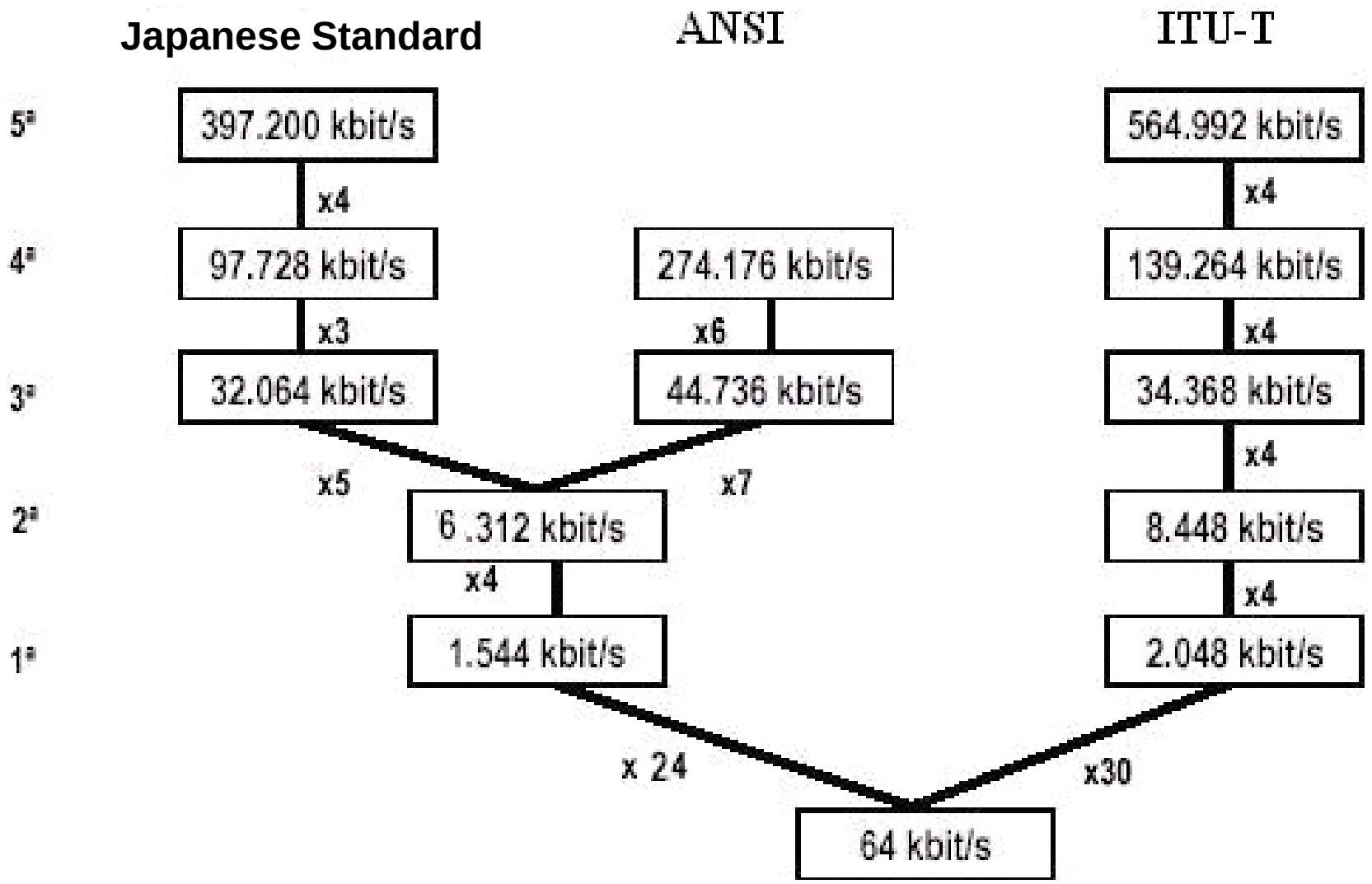
- f_{sn} is the nominal frequency of the locally generated clock;
- f_{pn} is the nominal value of the tributary signal rate;
  - the nominal frequency of the writing clock;
- f_{sn}' is the nominal reading frequency of the elastic buffer;
- f_d is the mean justification frequency;
- f_{dmax} is the maximum justification frequency;
  - obtained when the reading frequency attains the maximum permitted limit, and the writing frequency the minimum permitted limit.

$$f_{sn}^{'} = f_{sn};\ f_d = f_{sn}^{'} - f_{pn} \geq 0;\ f_{dmin} = 0;\ f_{dmax} = \frac{f_{sn}}{N_0}$$

$$f_{pnmax} = f_{sn}^{'} - f_{dmin};\ f_{pnmin} = f_{sn}^{'} - f_{dmax}$$

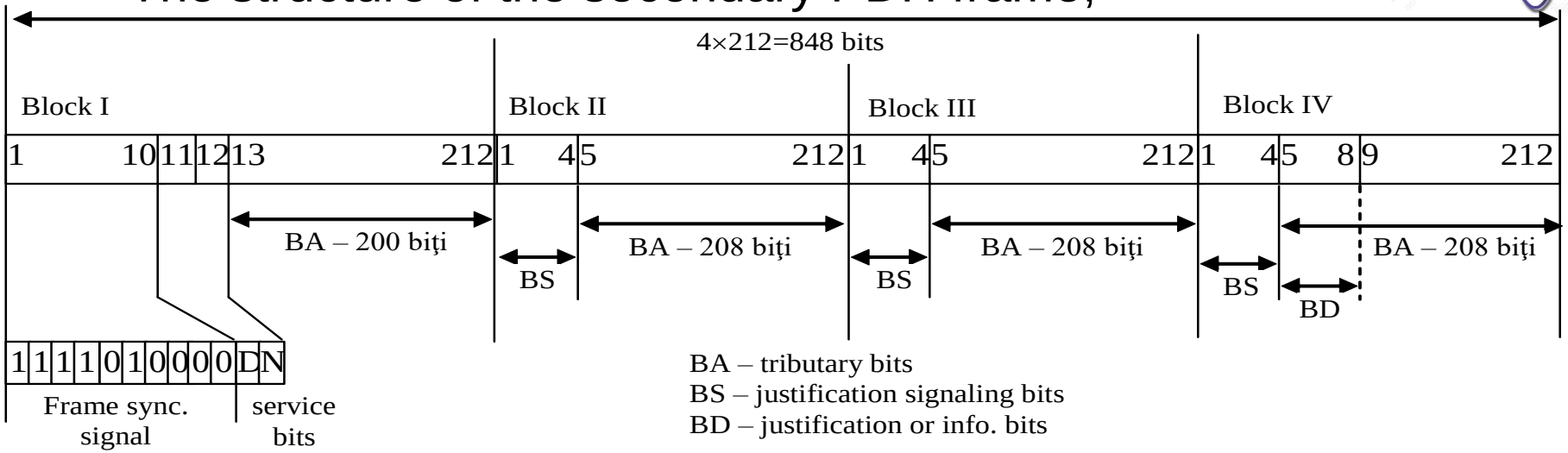


The PDH multiplexing hierarchy

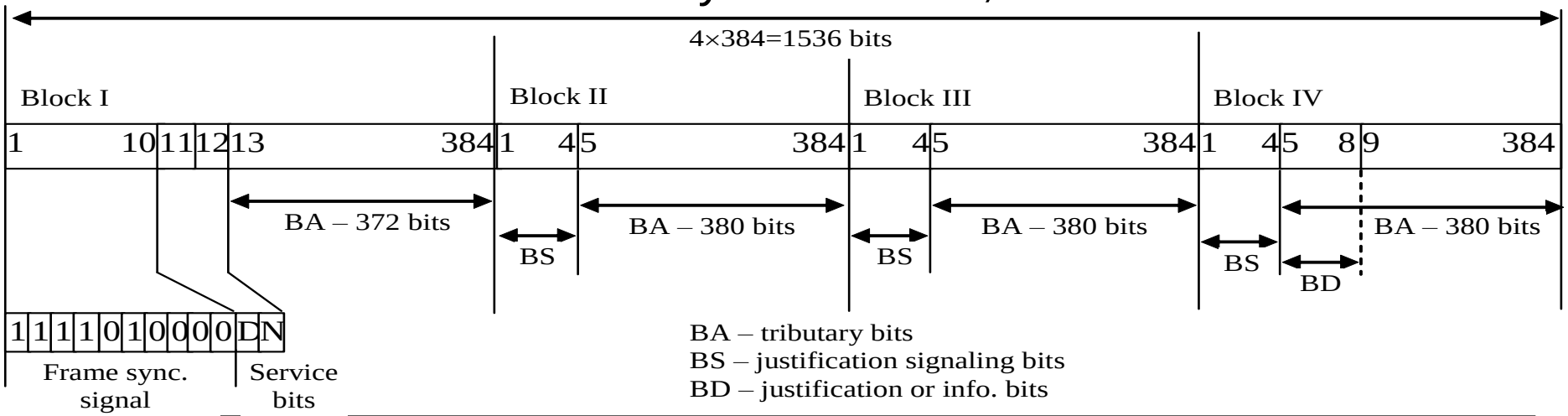


The PDH multiplexing hierarchy

- The structure of the secondary PDH frame;

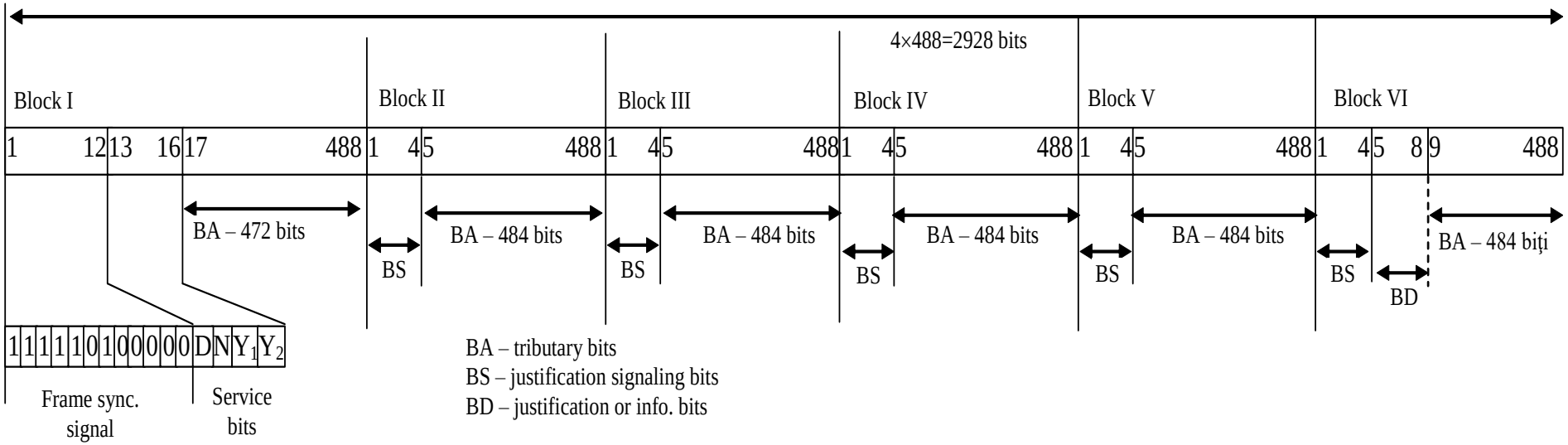


- The structure of the tertiary PDH frame;



The PDH multiplexing hierarchy

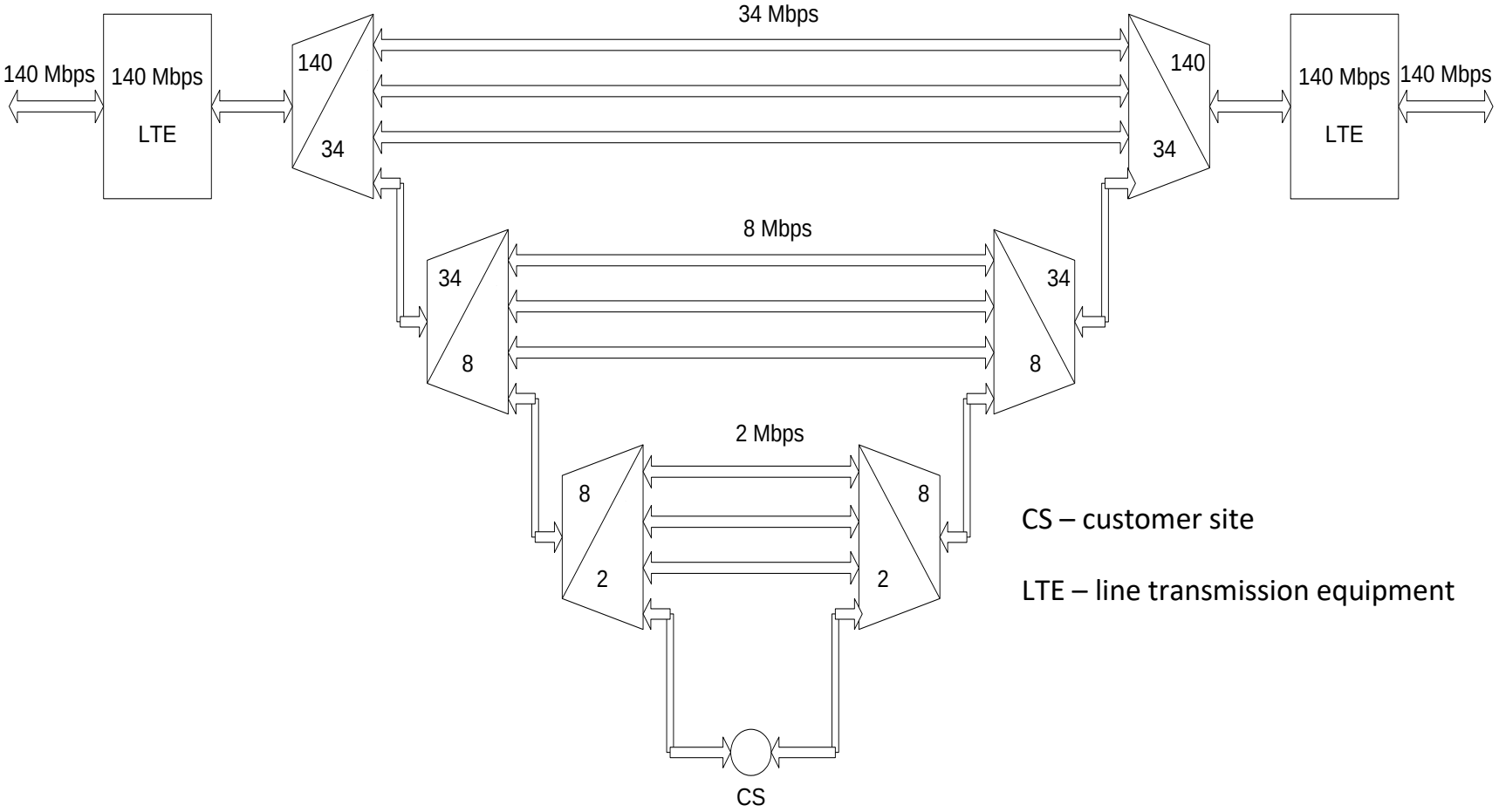
- The structure of the quaternary PDH frame;



- Disadvantages of PDH systems:
  - limited management and reconfiguration capabilities;
  - low flexibility;
    - designed only for circuit switching (voice transmission);
    - it is relatively difficult to use this system for other services (for ex. packet data);
  - the insertion and extraction of a basic data stream requires the demultiplexig and re-multiplexing of the entire multiplex signal;

The PDH multiplexing hierarchy

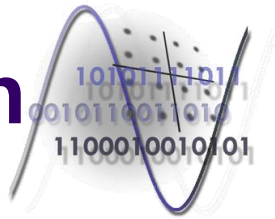
- Ex.: insertion / extraction of a 2Mbps stream into / from a multiplex signal having the bit rate 140 Mbps;



Frame synchronization

- In transmission systems with time division multiplexing it is necessary:
  - Identification at reception of the multiplexing order of the involved tributaries;
  - Identification of the first bit of the frame;
- In the multiplexed digital signal it is inserted a special code group/sequence named synchronization group;
  - Relatively to this sequence is defined the order of the multiplexed tributaries;
- The *cyclic* or *group synchronization* process;
  - It achieves the alignment between the transmission and reception side of a digital transmission system;
  - It is maintained and restored the alignment, in case of losing this;
    - in some situations could be necessary the use of two levels of synchronization, namely: frame and word synchronization (characteristic for the primary multiplex).

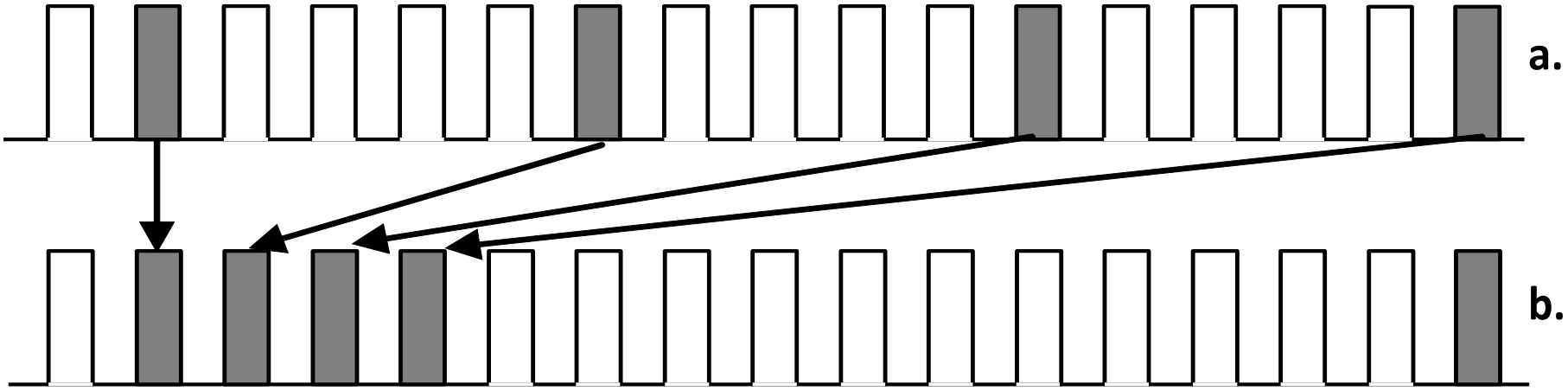
Frame synchronization



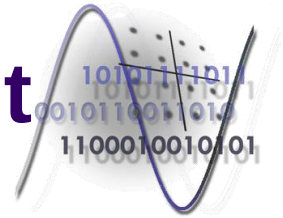
- Conditions imposed to the synchronization sequence:
  - To reduce as much as possible the simulations (of this sequence) by the transmitted data;
  - The recognition (detection) probability of these sequences must be high in the presence of bit errors;
- Methods for insertion of the synchronization sequence:
  - Distributed allocation;
    - is proper for channels with high level of bit errors (especially packet errors);
      - the synchronization is reestablished faster in the presence of packet errors;
    - the complexity of the method is higher;
      - for low error probability the synchronization time is larger.
  - Grouped allocation;
    - is more sensitive to bit errors – especially to packet errors;
    - the complexity of the method is lower;
      - the synchronization time is lower for low error probability.

Frame synchronization

- The choice of a given method depends on:
  - the technological complexity;
  - error performance;
  - the synchronization time.
- Synchronization group insertion methods:
  - a) distributed insertion ; b) grouped insertion.



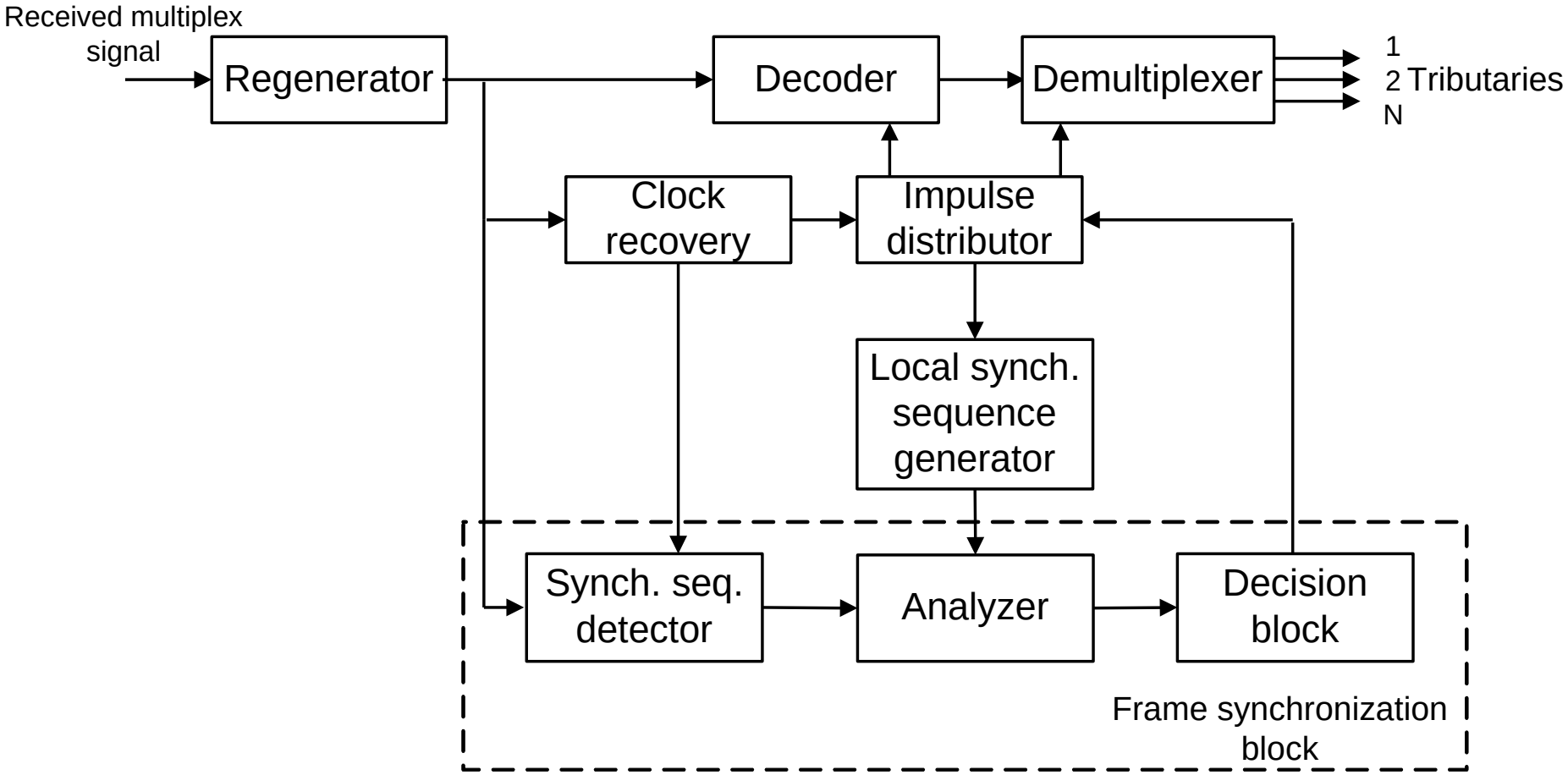
The synchronization equipment



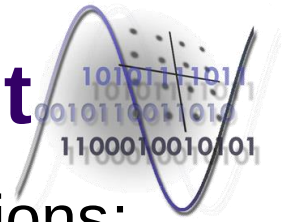
- The synchronization devices must fulfill the following requirements:
  - synchronization time at the connection set up and after the loss of synchronization as small as possible;
  - minimum synchronization information in a frame in the condition of an acceptable synchronization search time;
  - the detection probability of the synchronization signal must be high in the condition of bit errors;
    - the time between two losses of the synchronization must be as large as possible;
  - the synchronization equipment must be as simple and reliable as possible;
- The synchronization device has the following functions:
  - establishment of the synchronization at the beginning of the transmission;
  - control of the synchronism state during the transmission;
  - identification of the states when the synchronization is missing;
  - reestablishment of the synchronization after the loss of this.

The synchronization equipment

- Block schematic of a cyclic synchronization circuit;
  - Positioning of the synchronization device inside the receiver;



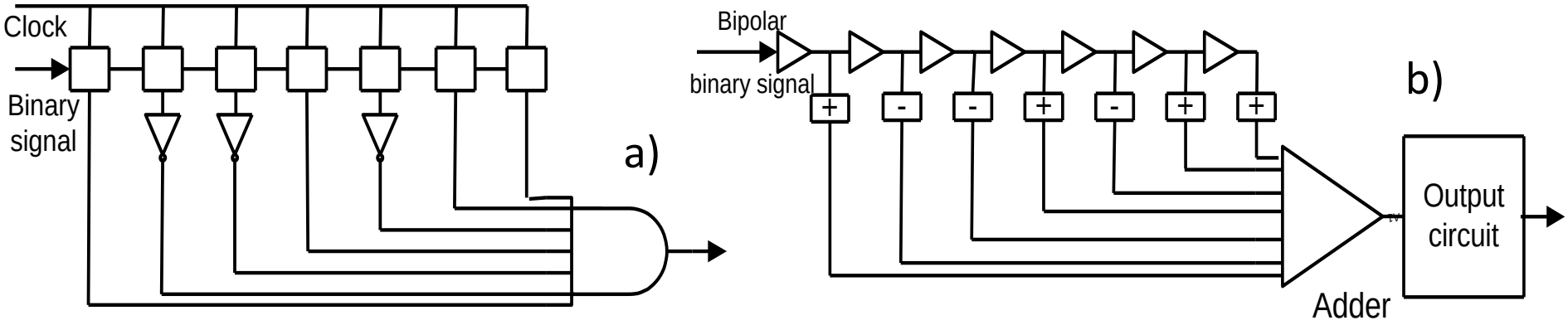
The synchronization equipment



- Three blocks can be identified with the following functions:
  - **The detector** of the synchronization group:
    - evaluates the received digital signal and separates the code groups (groups of information bits) having similar structure with the synchronization group;
    - the synchronization group is separated based on the maximum correlation between the received signal and the synchronization group stored in the detector;
    - there are two possibilities for evaluation of the received signal:
      - serial evaluation – bit by bit processing;
        - it is simple to implement;
      - parallel evaluation - storage of a transmission cycle and processing after that;
    - the detector can extract code groups which are not the synchronization group;
      - simulations (of the synchronization group) produced by the transmitted bits, having a probabilistic characteristic;
      - the decrease of the number of false synchronizations is achieved by other blocks of the synchronization device;
        - has to be established an appropriate detection/decision threshold.

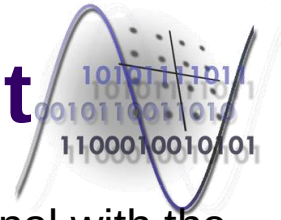
The synchronization equipment

- Block schematics of the synchronization group detector circuit;



- a) simple implementation;
  - does not allow the detection of the synchronization group in the presence of bit errors;
- b) more complex implementation;
  - allows the detection of the synchronization group in the presence of bit errors;

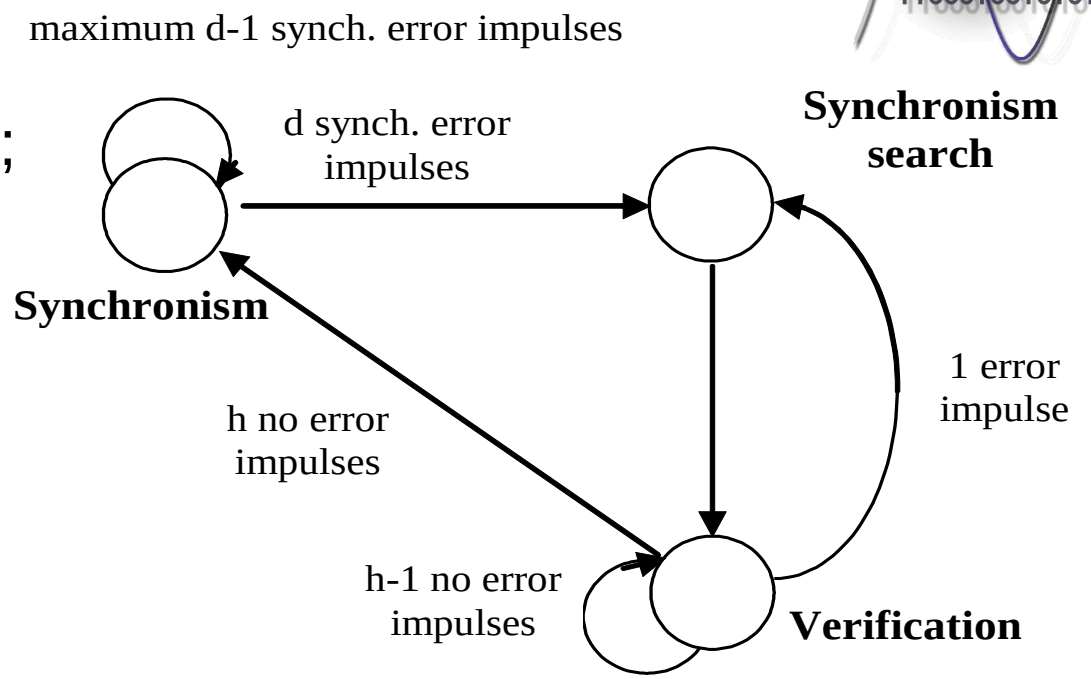
The synchronization equipment



- **The analyzer;**
  - it compares the synchronization group extracted from the received signal with the locally generated synchronization group;
  - takes decisions on the correspondence between the two signals according to the following criterions:
    - the repetition period, necessary to verify if the synchronization group is a real one or it is a simulation by the information signal;
    - the apparition time of the synchronization group - it is verified if the local synchronization group appears simultaneously whit the extracted synchronization group;
  - the analyzer output signal:
    - error or no synchronization error – reflects the two enunciated criterions.
- **The decision circuit;**
  - takes decisions on the synchronism state based on the analyzer output according to a criteria named *synchronization strategy*;
  - using the command signal generated the system pass through the states of synchronism search, synchronism verification and synchronism;
  - works based on a synchronization strategy which targets:
    - decrease of the synchronization loss probability due to false detections and errors;
    - detection of the synchronism state, as exactly as possible, after loss of synchronization.

The synchronization equipment

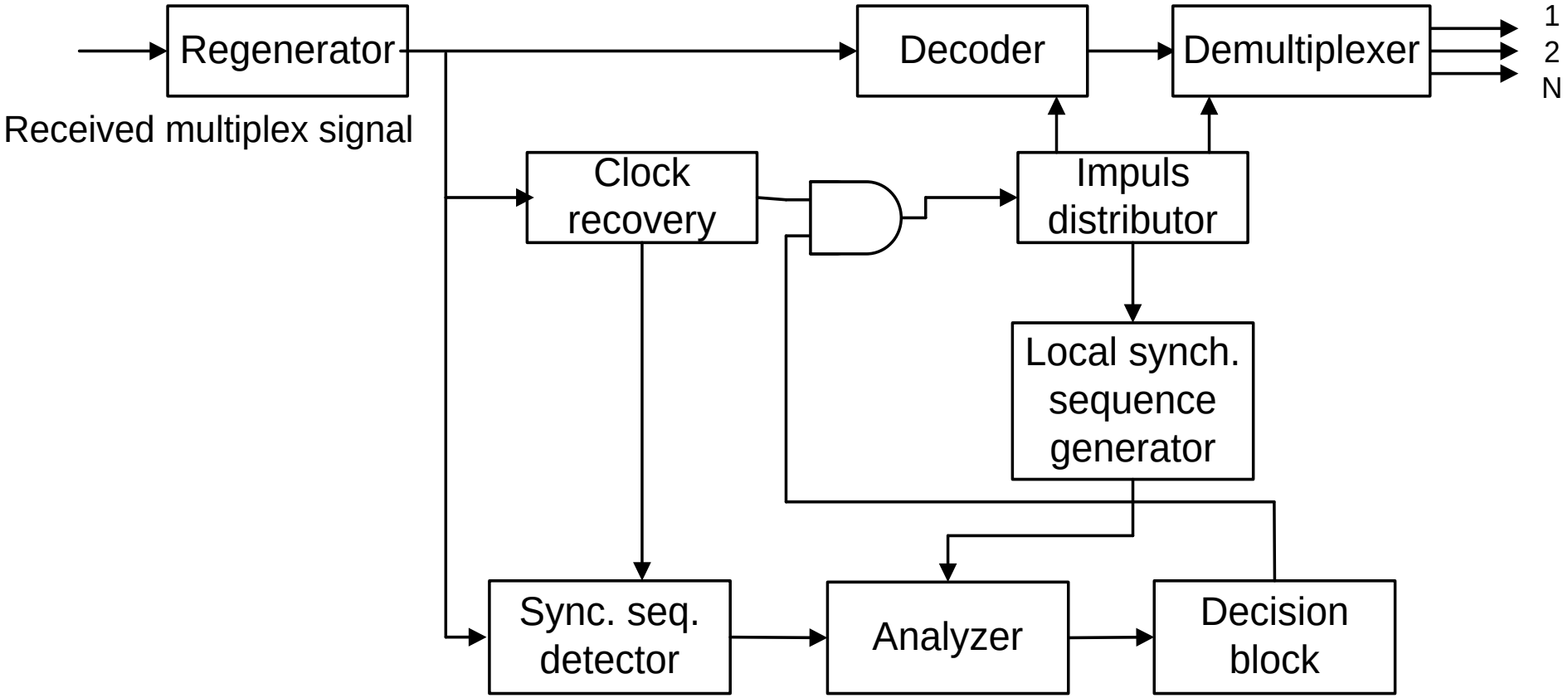
- General strategy of frame synchronization;



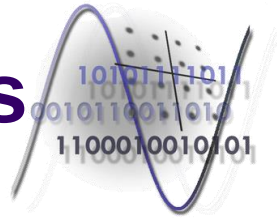
- if the circuit is in the synchronism state it is necessary to appear *d* consecutive false detections of the synchronization group in order to pass in the synchronism search state;
- in order to go back in the synchronism state there are necessary *h* correct detections of the synchronization group;
- any false detection of the synchronization group determines the transition from the synchronism verification state in the synchronism search state.

Cyclic synchronization methods

- Cyclic synchronization by delay of the clock impulses;
  - Block schematic of the cyclic synchronization circuit based on the impulse delay method;



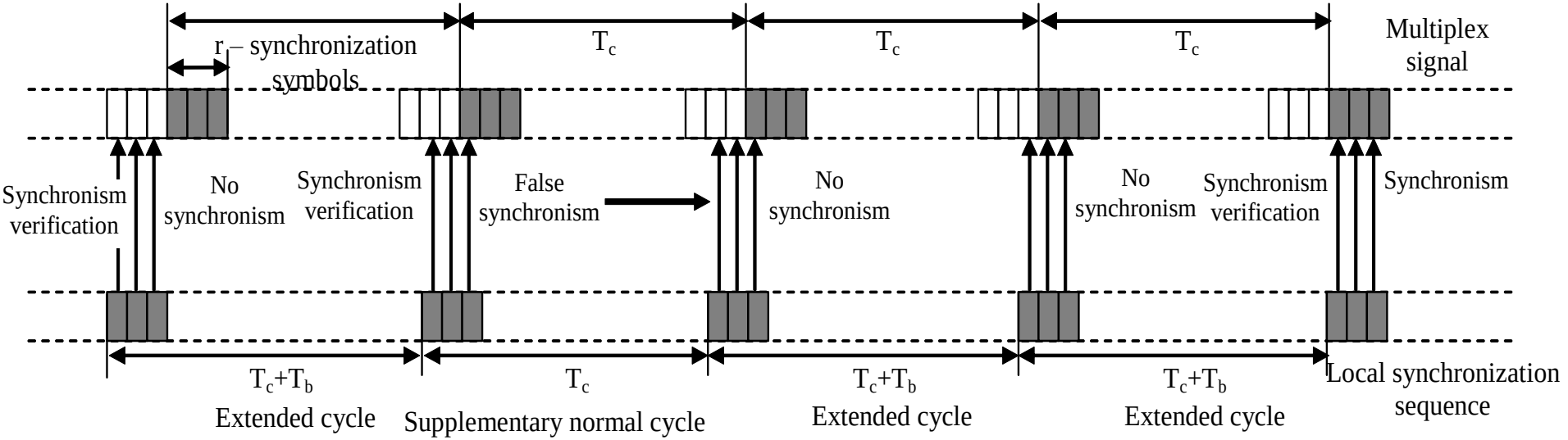
Cyclic synchronization methods



- Functioning:
  - in the synchronism state:
    - the signal obtained at the output of the synchronization group detector appears in the same moment and with the same periodicity as the local synchronization group;
    - the decision circuit allows passing of the clock to the impulse distributor.
  - in the synchronism search state;
    - the analyzer input signals do not satisfy the periodicity and apparition time conditions;
    - an interdiction signal is generated by the decision circuit (in the apparition moment of the locally generated synchronization group) which blocks the gate circuit (and the clock access to the impulse distributor) a clock period ;
    - the cycle of the local impulse distributor is extended with one bit period;
    - the searching process keeps going until the synchronism state is decided by the analyzer;
  - very low probability of false synchronization but very high synchronization time;

Cyclic synchronization methods

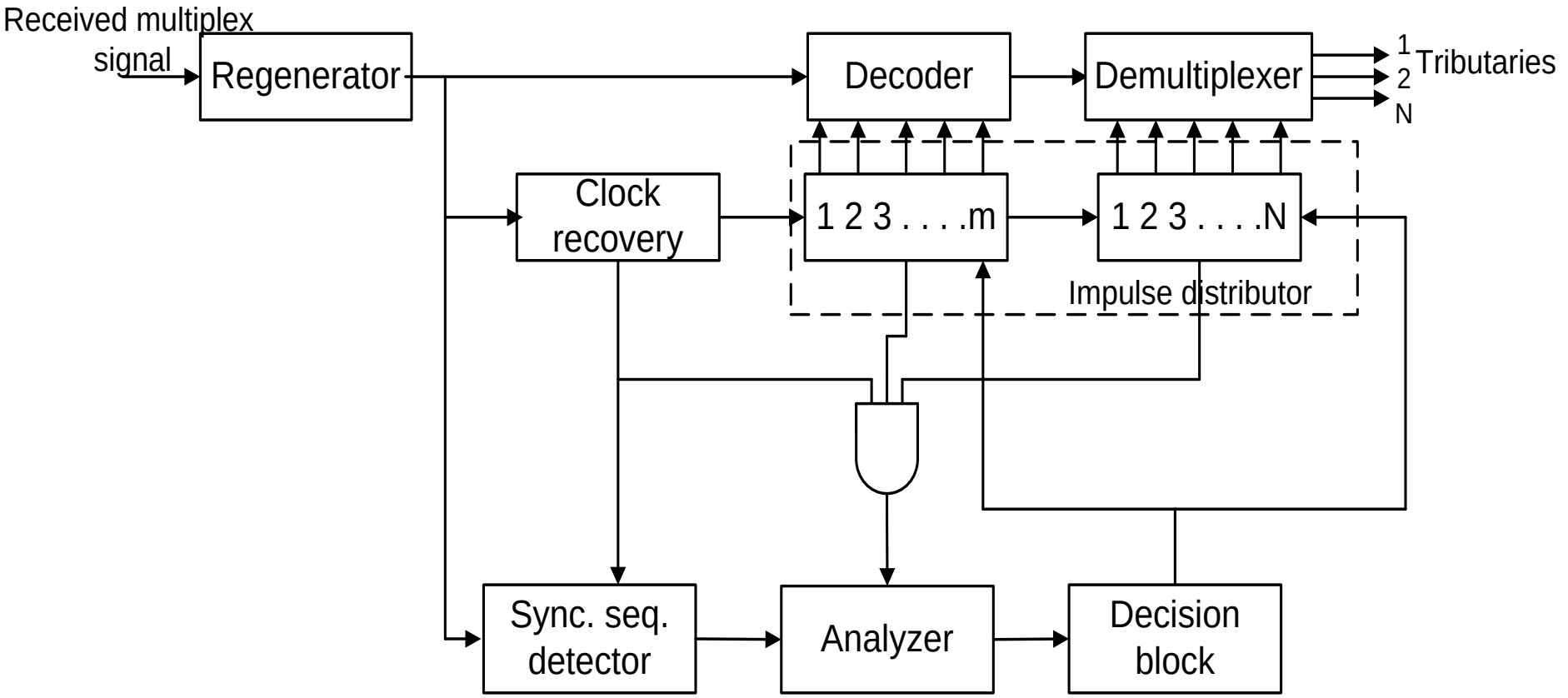
- Cyclic synchronization algorithm based on delay of clock impulses;



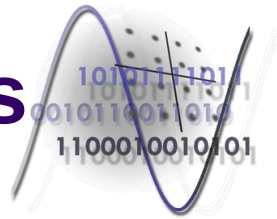
- There are two types of cycles:
  - extended cycles specific to normal functioning in search state;
    - cycles with a T_c+T_b duration;
    - by these cycles it is decreased the time difference between the received and the local synchronization group with one clock period at every moment, when the local synchronization group is applied to the analyzer;
  - supplementary cycles due to the apparition of false synchronization groups in the received signal, groups detected by the synchronization group detector;
    - these cycles slow down the synchronization search process.

Cyclic synchronization methods

- Cyclic synchronization by sliding;
  - Block schematic of the cyclic synchronization circuit based on the sliding method;



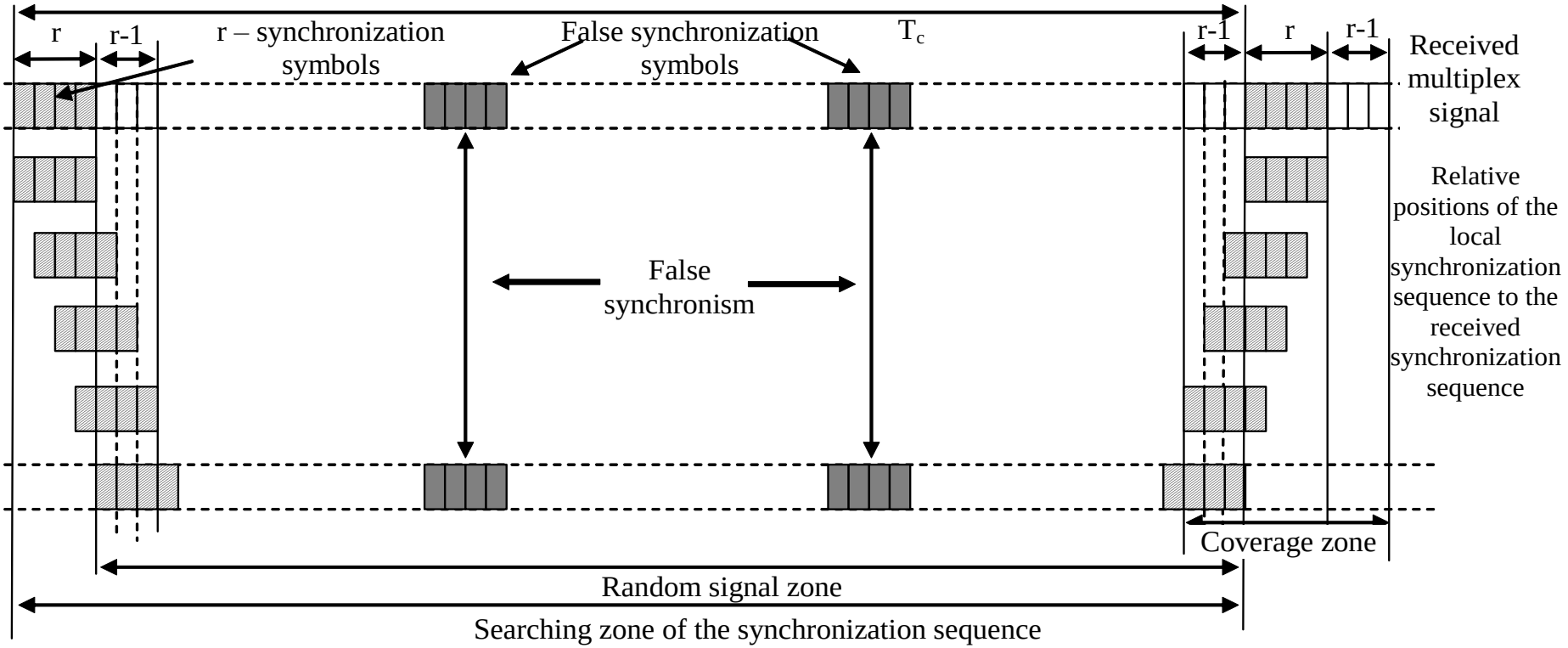
Cyclic synchronization methods



- Main characteristics:
  - ensures a substantial increase of the synchronization speed;
  - it is not generated a local synchronization sequence;
    - the detection moment of the received synchronization group is compared with the state of the decoder and demultiplexer impulse distributor;
    - the probability of false synchronizations is higher relatively to the method based on delay of the clock impulses.
- Functioning:
  - in the synchronism state:
    - the impulse from the AND gate, obtained by the coincidence between the clock impulse, impulse **m** of decoder impulse distributor and the impulse **N** of demultiplexer impulse distributor is in phase with the impulse generated by the synchronization group detector;
  - the loss of the synchronization:
    - means the absence of the coincidence between impulses at the output of the AND circuit and the synchronization group detector;
  - in synchronism search state:
    - it is generated a restart command of the impulse distributors at each detection of the synchronization group: the impulse distributors are forced in synchronism position.

Cyclic synchronization methods

- Cyclic synchronization algorithm based on sliding method;



- in synchronism state false detections of the synchronization group could appear only due to bit errors in the received signal;
  - around the synchronization group of length r, appears a region of r-1 symbols, where it is verified both the information signal and the synchronization group;
    - this is the region more exposed to false detection of the synchronization group;