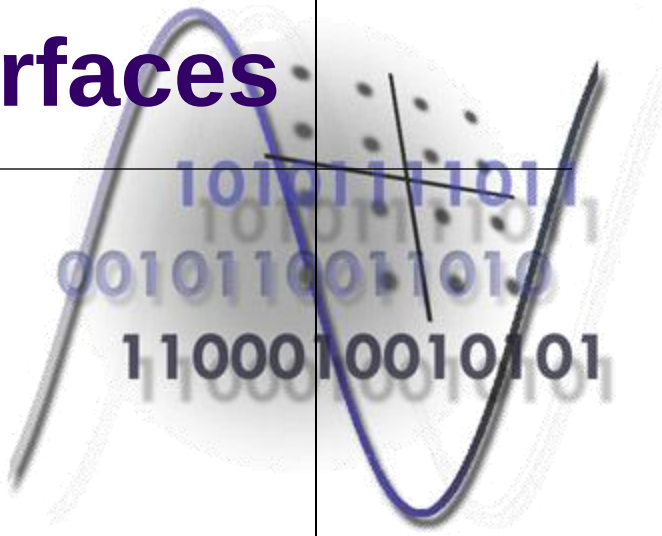
Course 4
Frame synchronization. PCM multiplexer interfaces



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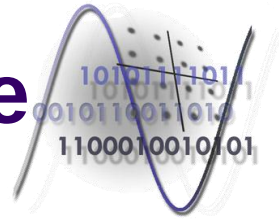
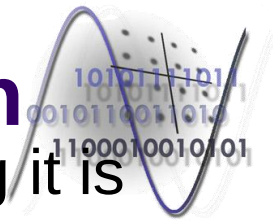
Content of the course



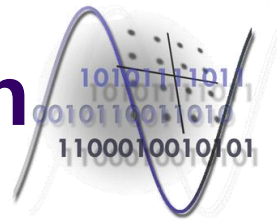
- Frame synchronization;
  - Synchronization sequence insertion methods;
  - Cyclic synchronization equipment;
  - Cyclic synchronization methods;
  - Frame synchronization algorithms for the primary multiplex E1.
- PCM multiplexer interfaces
  - Line interface of PCM multiplexers;
  - Terminal – PCM multiplexer interface.

Frame synchronization



- In transmission systems with time division multiplexing it is necessary;
  - Identification at reception of the multiplexing order of the involved tributaries;
  - Identification of the first bit of the frame;
- In multiplexed digital signal it is inserted a special code group named synchronization group;
  - Relatively to this sequence is defined the order of the multiplexed tributaries;
- The *cyclic* or *group synchronization* process;
  - It achieves the alignment between the transmission and reception side of a digital transmission system;
  - It is maintained and restored the alignment, in case of losing this;
    - in some situations could be necessary the use of two levels of synchronization, namely: frame and word synchronization (characteristic for the primary multiplex).

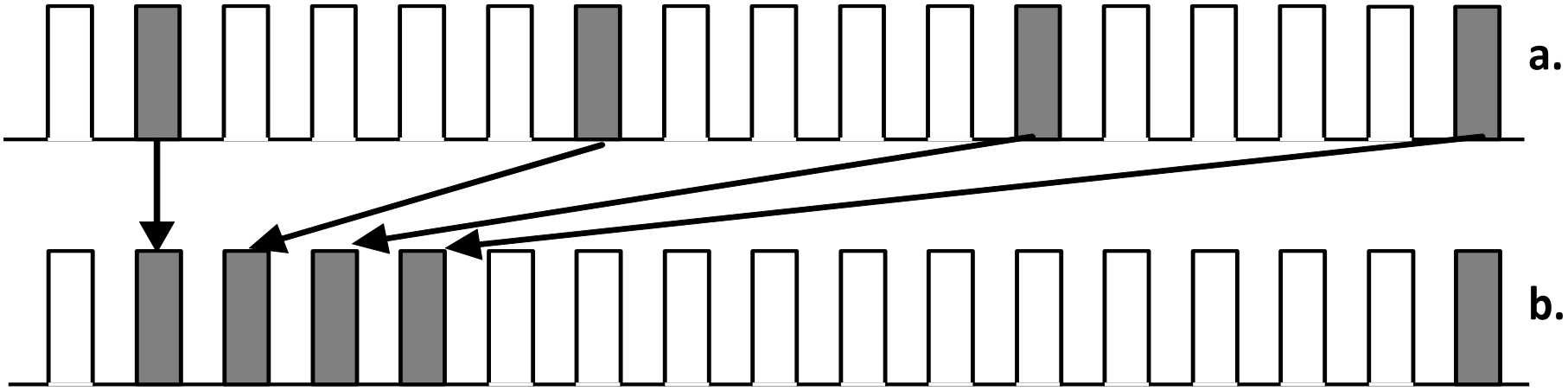
Frame synchronization



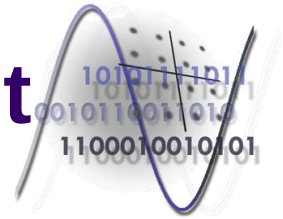
- Conditions imposed to the synchronization sequence:
  - To reduce as much as possible the simulations (of this sequence) by the transmitted data;
  - The recognition (detection) probability of these sequences must be high in the presence of bit errors;
- Methods for insertion of the synchronization sequence:
  - Distributed allocation;
    - is proper for channels with high level of bit errors (especially packet errors);
      - the synchronization is reestablished faster in the presence of packet errors;
    - the complexity of the method is higher;
      - for low error probability the synchronization time is larger.
  - Grouped allocation;
    - is more sensitive to bit errors – especially to packet errors;
    - the complexity of the method is lower;
      - the synchronization time is lower for low error probability.

Frame synchronization

- The choice of a given method depends on:
  - the technological complexity;
  - error performances;
  - the synchronization time.
- Synchronization group insertion methods:
  - a) distributed insertion ; b) grouped insertion.



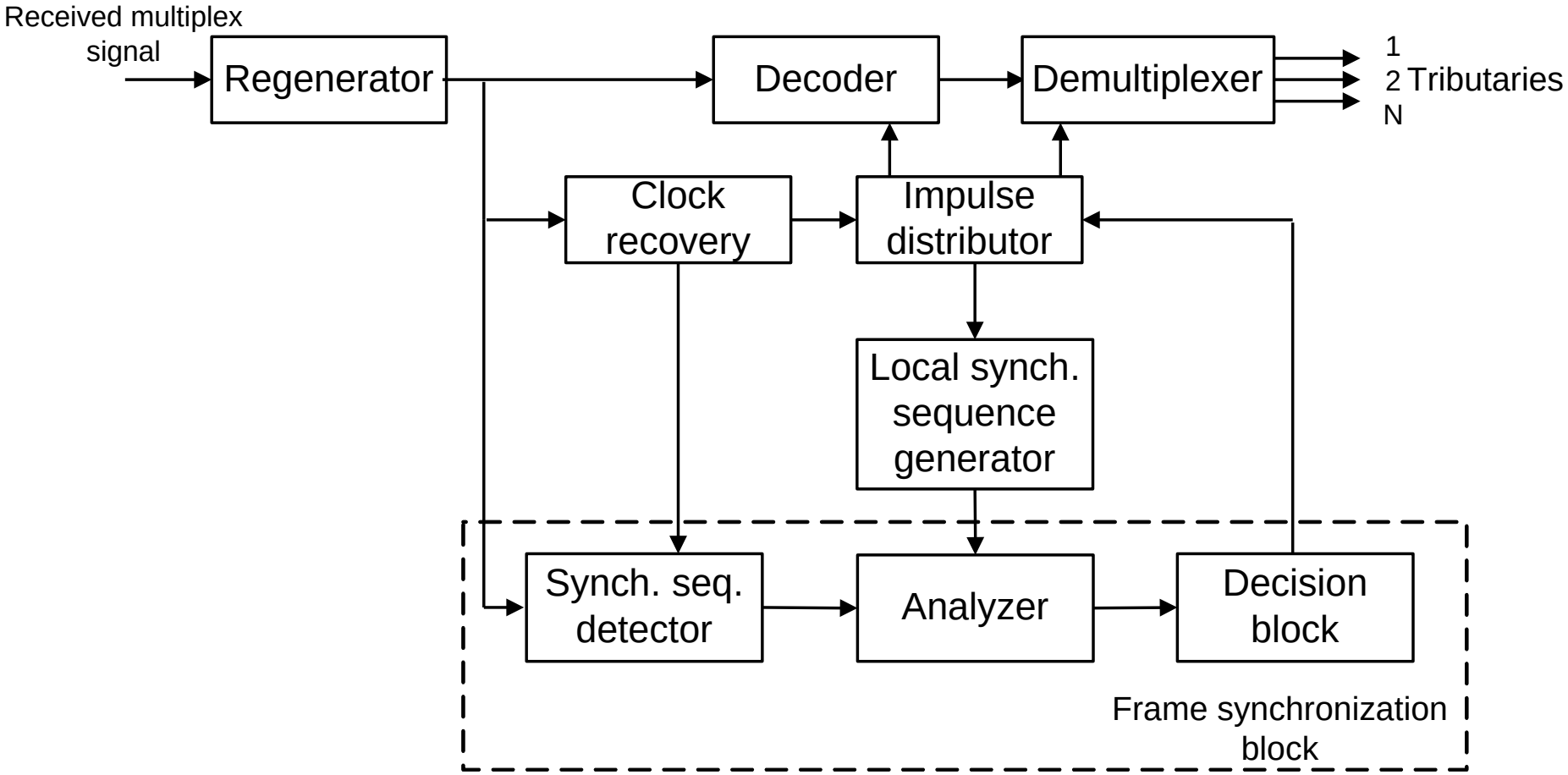
The synchronization equipment



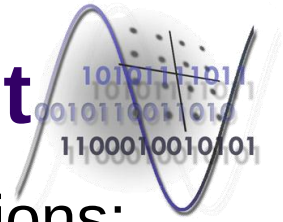
- The synchronization devices must fulfill the following requirements:
  - synchronization time at the connection establishment and after the loss of synchronization as small as possible;
  - minimum synchronization information in a frame in the condition of an acceptable synchronization search time;
  - the detection probability of the synchronization signal must be high in the situation of bit errors;
    - the time between two losses of the synchronization must be as large as possible;
  - the synchronization equipment must be as simple and reliable as possible;
- The synchronization device has the following functions:
  - establishment of the synchronization at the beginning of the transmission;
  - control of the synchronism state during the transmission;
  - identification of the states when the synchronization is missing;
  - reestablishment of the synchronization after the loss of this.

The synchronization equipment

- Block schematic of a cyclic synchronization circuit;
  - Positioning of the synchronization device inside the receiver;



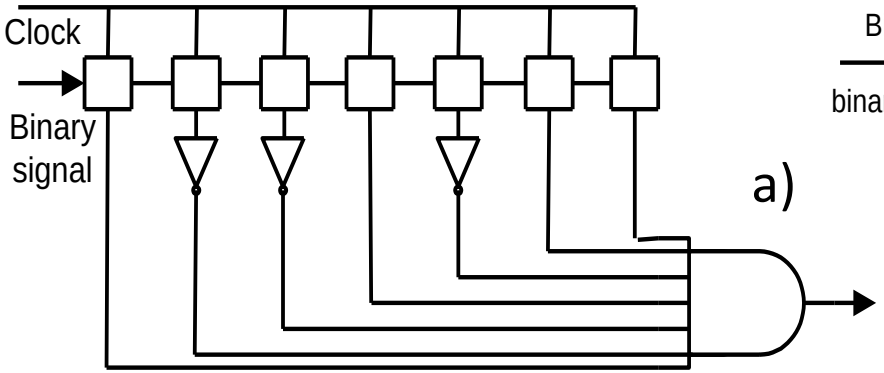
The synchronization equipment

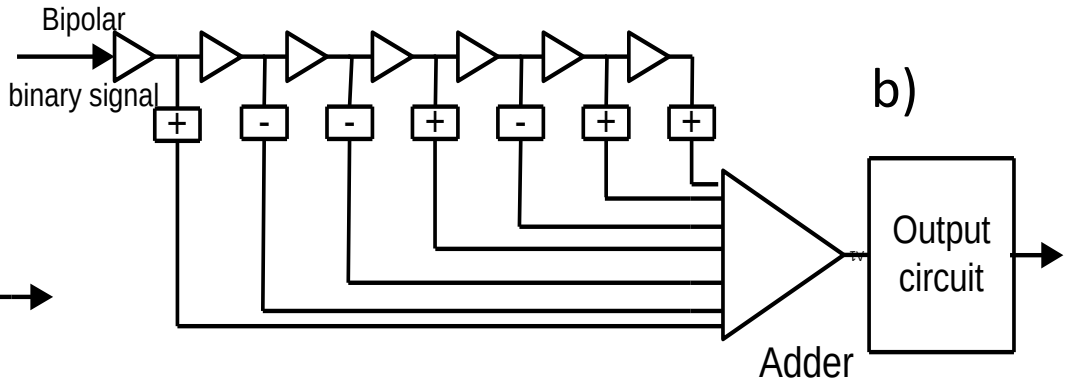


- Three blocks can be identified with the following functions:
  - **The detector** of the synchronization group:
    - evaluates the received digital signal, separating the code groups (groups of information bits) having similar structure with the synchronization group;
    - the synchronization group is separated based on the maximum correlation between the received signal and the synchronization group stored in the detector;
    - there are two possibilities for evaluation of the received signal:
      - serial evaluation – bit by bit processing;
        - it is simple to implement;
      - parallel evaluation - storage of a transmission cycle and processing after that;
    - the detector can extract code groups which are not the synchronization group;
      - simulations (of the synchronization group) produced by the transmitted bits, having a probabilistic characteristic;
      - the decrease of the number of false synchronizations is achieved by other blocks of the synchronization device;
        - has to be established an appropriate detection/decision threshold.

The synchronization equipment

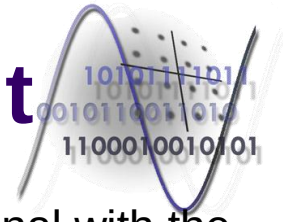
- Block schematics of the synchronization group detector circuit;





  - a) simple implementation;
    - does not allow the detection of the synchronization group in the presence of bit errors;
  - b) more complex implementation;
    - allows the detection of the synchronization group in the presence of bit errors;

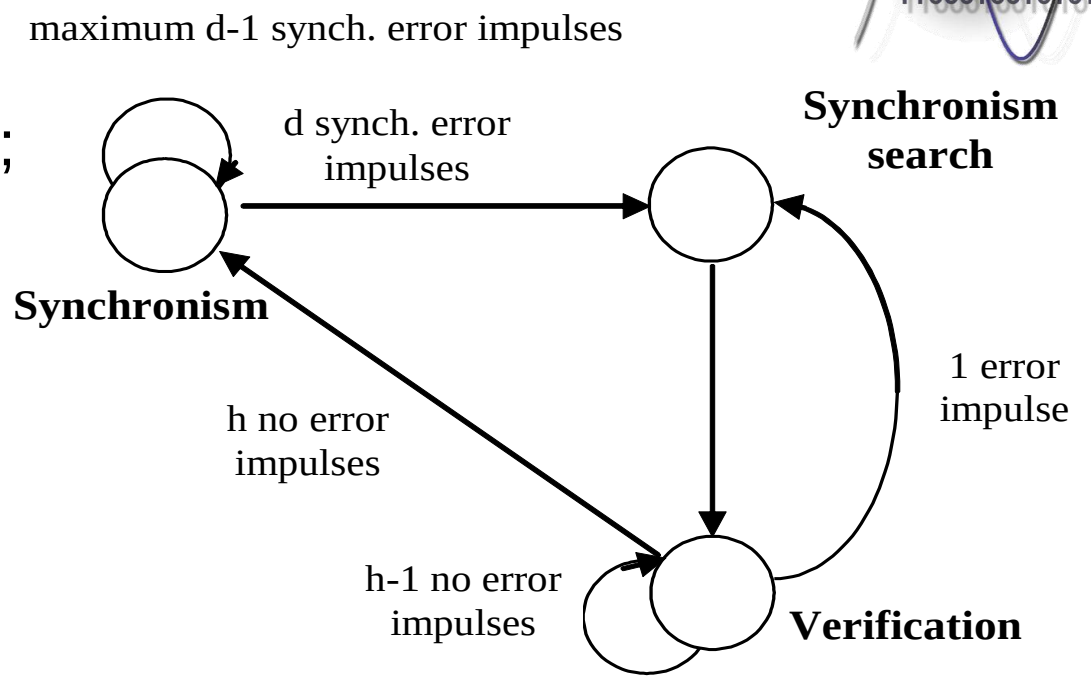
The synchronization equipment



- **The analyzer;**
  - it compares the synchronization group extracted from the received signal with the locally generated synchronization group;
  - takes decisions on the correspondence between the two signals according to the following criterions:
    - the repetition period, necessary to verify if the synchronization group is a real one or it is a simulation by the information signal;
    - the apparition time of the synchronization group - it is verified if the local synchronization group appears simultaneously whit the extracted synchronization group;
  - the analyzer output signal:
    - error or no synchronization error – reflects the two enunciated criterions.
- **The decision circuit;**
  - takes decisions on the synchronism state based on the analyzer output according to a criteria named *synchronization strategy*;
  - using the command signal generated the system pass through the states of synchronism search, synchronism verification and synchronism;
  - works based on a synchronization strategy which targets:
    - decrease of the synchronization loss probability due to false detections and errors;
    - detection of the synchronism state, as exactly as possible, after loss of synchronization.

The synchronization equipment

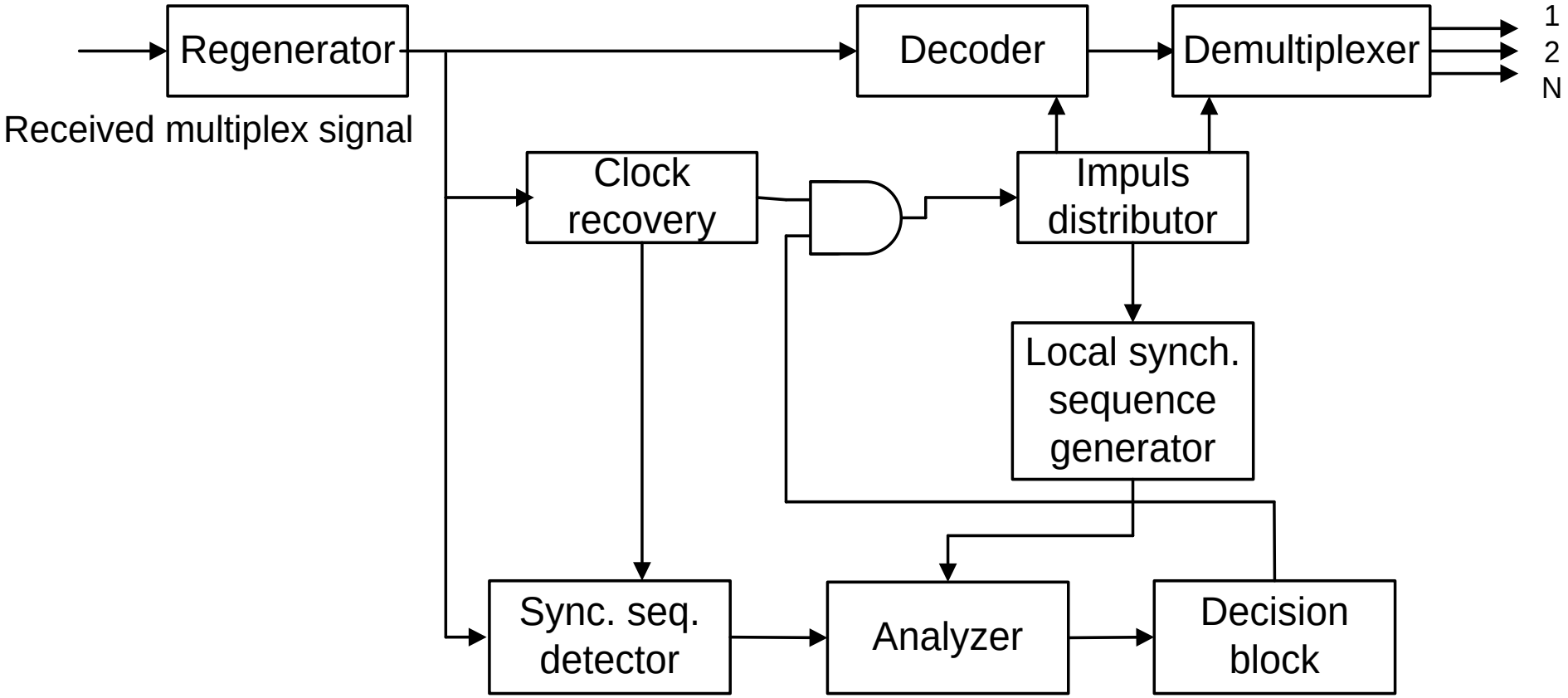
- General strategy of frame synchronization;



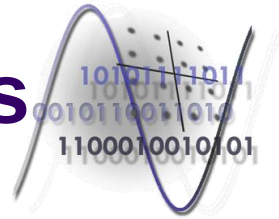
- if the circuit is in the synchronism state it is necessary to appear *d* consecutive false detections of the synchronization group in order to pass in the synchronism search state;
- in order to go back in the synchronism state there are necessary *h* correct detections of the synchronization group;
- any false detection of the synchronization group determines the transition from the synchronism verification state in the synchronism search state.

Cyclic synchronization methods

- Cyclic synchronization by delay of the clock impulses;
  - Block schematic of the cyclic synchronization circuit based on the impulse delay method;



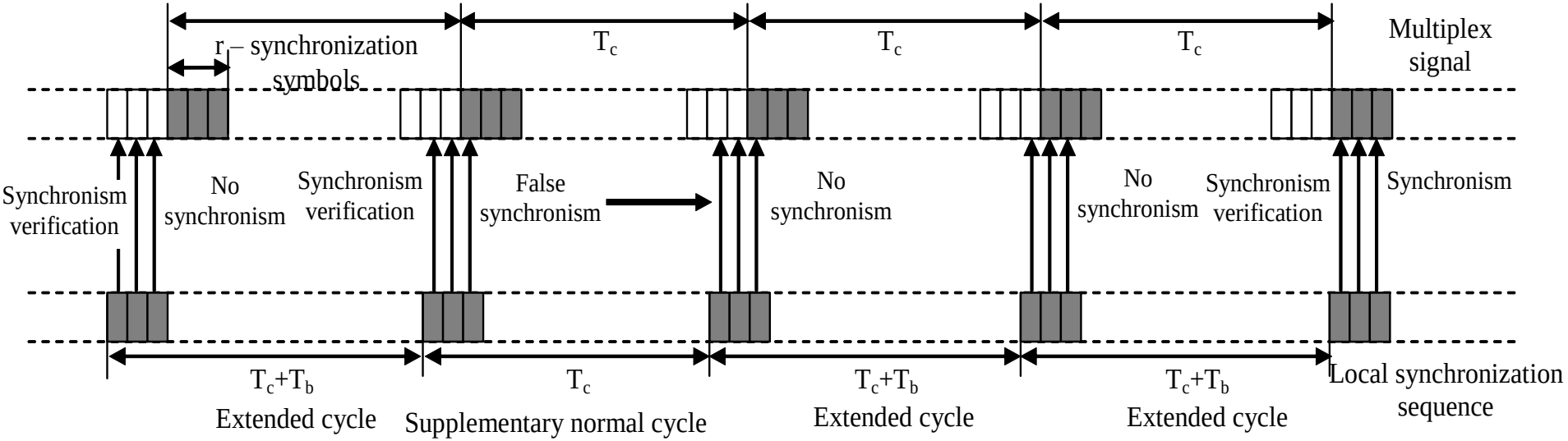
Cyclic synchronization methods



- Functioning:
  - in the synchronism state:
    - the signal obtained at the output of the synchronization group detector appears in the same moment and with the same periodicity as the local synchronization group;
    - the decision circuit allows the passing of the clock to the impulse distributor.
  - in the synchronism search state;
    - the analyzer input signals do not satisfy the periodicity and apparition time conditions;
    - an interdiction signal is generated by the decision circuit (in the apparition moment of the locally generated synchronization group) which blocks the gate circuit (and the clock access to the impulse distributor) a clock period ;
    - the cycle of the local impulse distributor is extended with one bit period;
    - the searching process keeps going until the synchronism state is decided by the analyzer;
  - very low probability of false synchronization but very high synchronization time;

Cyclic synchronization methods

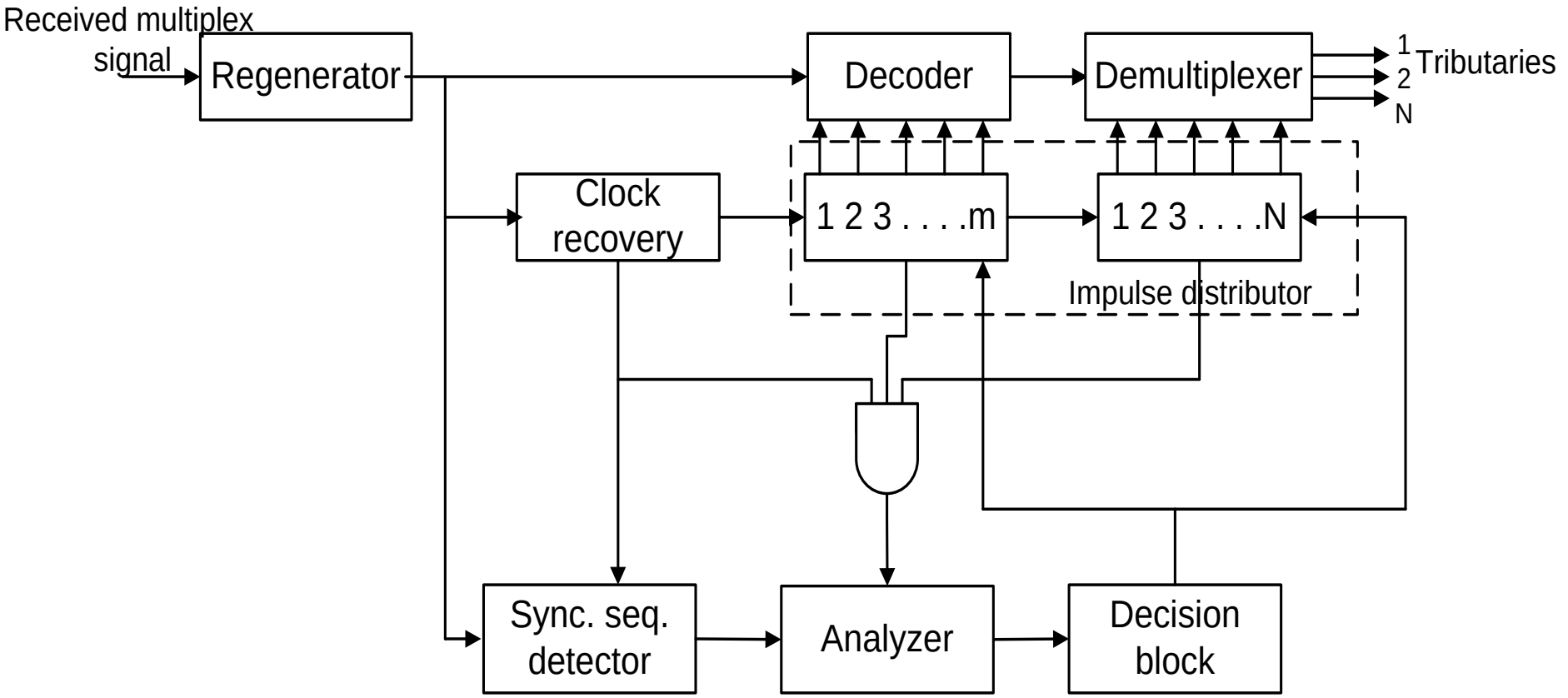
- Cyclic synchronization algorithm based on delay of clock impulses;



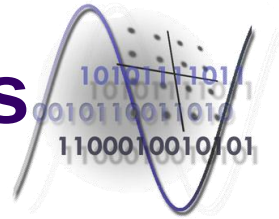
- There are two types of cycles:
  - extended cycles specific to normal functioning in search state;
    - cycles with a T_c+T_b duration;
    - by these cycles it is decreased the time difference between the received and the local synchronization group with one clock period at every moment, when the local synchronization group is applied to the analyzer;
  - supplementary cycles due to the apparition of false synchronization groups in the received signal, groups detected by the synchronization group detector;
    - these cycles slow down the synchronization search process.

Cyclic synchronization methods

- Cyclic synchronization by sliding;
  - Block schematic of the cyclic synchronization circuit based on the sliding method;



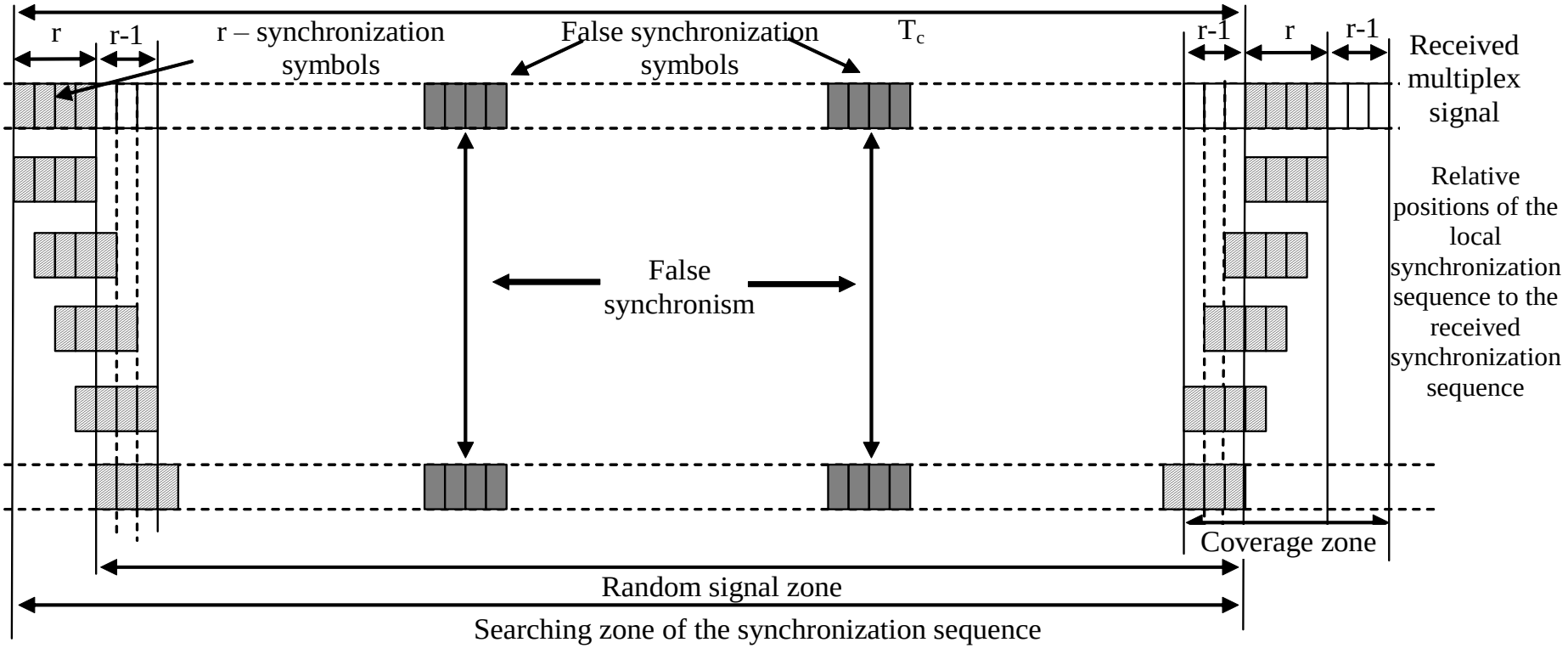
Cyclic synchronization methods



- Main characteristics:
  - ensures a substantial increase of the synchronization speed;
  - it is not generated a local synchronization sequence;
    - the detection moment of the received synchronization group is compared with the state of the decoder and demultiplexer impulse distributor;
    - the probability of false synchronizations is higher relatively to the method based on delay of the clock impulses.
- Functioning:
  - in the synchronism state:
    - the impulse from the AND gate, obtained by the coincidence between the clock impulse, impulse **m** of decoder impulse distributor and the impulse **N** of demultiplexer impulse distributor is in phase with the impulse generated by the synchronization group detector;
  - the loss of the synchronization:
    - means the absence of the coincidence between impulses at the output of the AND circuit and the synchronization group detector;
  - in synchronism search state:
    - it is generated a restart command of the impulse distributors at each detection of the synchronization group: the impulse distributors are forced in synchronism position.

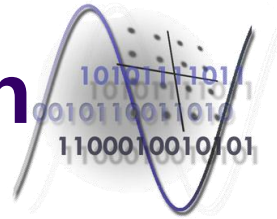
Cyclic synchronization methods

- Cyclic synchronization algorithm based on sliding method;



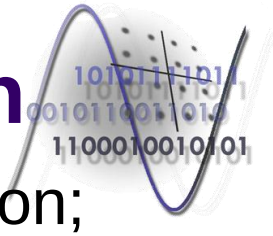
- in synchronism state false detections of the synchronization group could appear only due to bit errors in the received signal;
  - around the synchronization group of length r, appears a region of r-1 symbols, where it is verified both the information signal and the synchronization group;
    - this is the region more exposed to false detection of the synchronization group;

The E1 PCM frame. Synchronization



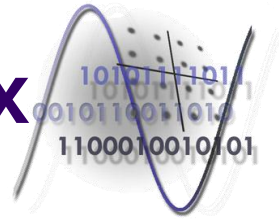
- Aspects related to frame synchronization;
  - Loss of frame synchronization detection:
    - three consecutive frames with FAS errors or,
    - three consecutive bit errors in position two in frames without FAS or,
    - bit error probability higher then 10^{-3};
      - the FAS signal is monitored for this error detection;
    - in CRC-4 working mode 1000 CRC comparison are performed in a second;
      - if the threshold of 914 bad comparisons (91.4%) is exceeded it is declared loss of the frame synchronization;
      - it ensures a better frame synchronization, being avoided the problem of frame alignment sequence (FAS) simulation.

The E1 PCM frame. Synchronization



- Aspects related to frame and multiframe synchronization;
  - Loss of multiframe synchronization detection in the CAS case:
    - two consecutive MFAS signals with errors or,
    - two multiframes with all zero bits in slot 16;
  - Frame and multiframe synchronization detection:
    - **Normal frame synchronization:**
      - FAS received correctly, bit two in NFAS is “1”, next FAS received correctly;
    - **Multiframe synchronization with CAS:**
      - MFAS received correctly and slot 16 of the previous frame is not zero;
    - **Multiframe synchronization with CRC:**
      - bit in position one of NFAS frames generates the sequence: 0 0 1 0 1 1;
        - it is realized an initial frame and multiframe synchronization;
      - at least 2 CRC MFAS must be correctly received in a 8ms time interval (4 CRC-MF), between these MFAS detections being a time interval of 2ms or multiples of this value;
        - it is realized a check and validation of the synchronization based on the CRC control sequence.

Line interface of the primary multiplex

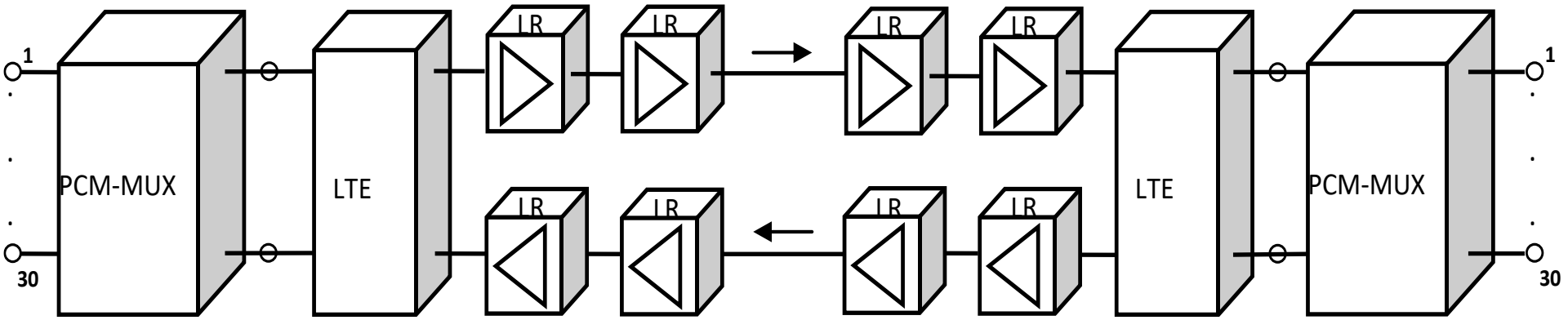


- Transmission of the E1 frame;
  - 4 wire full duplex transmission;
    - AMI (*Alternate Mark Inversion*) coding;
      - the “0” bit is coded with a 0V level and the “1” bits are alternatively coded with ± A impulses;
        - this code has no DC component (it is avoided the saturation of the separation transformer’s core);
        - has relatively narrow bandwidth;
        - simple decoding;
        - reduced synchronization capability;
      - it is replaced with a HDB3 (*High-Density-Bipolar-3 Zeros*) coding;
        - this code replaces groups of 4 zeros with violations of AMI coding rule – it is ensured also a reduced level of the DC component.

Line interface of the primary multiplex

The last impulse on line	Number of impulses from the last replace	
	Odd	Even
negative	0 0 0 -	+ 0 0 +
positive	0 0 0 +	- 0 0 -

- The HDB3 coding rule;

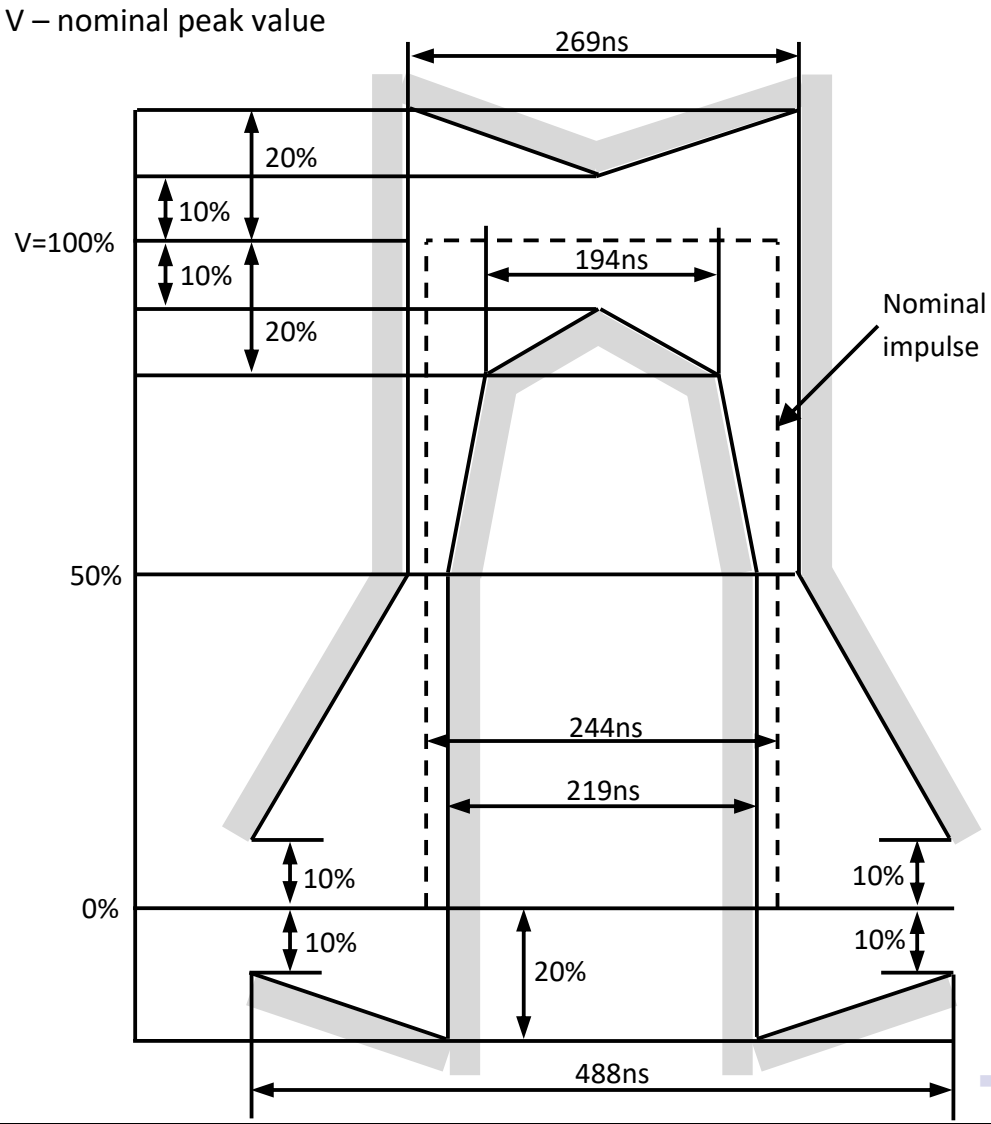


LTE – “Line Terminating Equipment”

LR – “Line Regenerator”

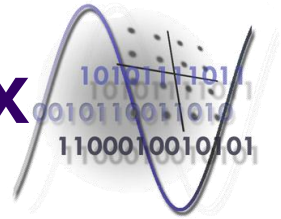
- E1 transmission system;

Line interface of the primary multiplex



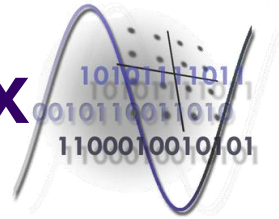
- Coded impulse mask;

Line interface of the primary multiplex



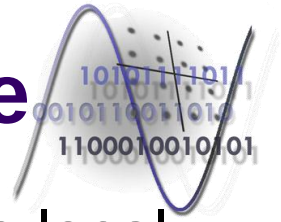
- (E1) line interface parameters:
  - Nominal bit rate: 2048kbps;
  - Precision of the nominal bit rate: at least ± 50ppm;
  - Line code: HDB3;
  - Frame structure;
  - Transmission medium / Number of pairs in each direction;
    - Coaxial; Twisted pairs; 1 cable / 1 pair for each transmission direction;
  - Load impedance: 75Ω (coaxial), 120Ω (twisted pair);
  - Peak amplitude: 2.37V – 3V;
  - Power level and power spectral mask;
  - Impulse nominal duration: 244ns;
  - Ration of positive and negative amplitudes: 0.95 – 1.05;
  - Ratio of positive/negative pulse duration: 0.95 – 1.05;
  - Maximum peak to peak jitter;
  - DC power: has to be as low as possible;

Line interface of the primary multiplex



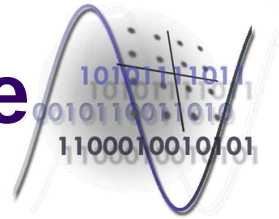
- T1 interface specific characteristics:
  - Transmission of T1 frames is similar with the transmission of E1 frames;
    - 4 wire full duplex with regenerators after each 1.5km cable length;
  - B8ZS *(Bipolar with 8 Zero Substitution)* line coding;
    - AMI type cod which replaces the groups of 8 consecutive zero bits with a coded sequence having the structure: 0 0 0 V B 0 V B;
      - 3 “0” symbols, a violation of the AMI coding rule, followed by a binary symbol encoded normally, a “0” symbol, after that a new violation of the AMI coding rule and finally a binary symbol encoded normally.

Terminal – multiplexer interface



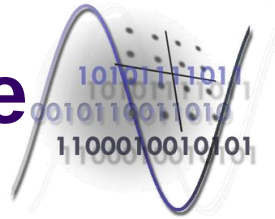
- There are defined two types of interfaces between the local equipment (terminal - multiplexer);
  - These correspond to two transmission strategy of data transmission and synchronization;
  - Codirectional interfaces;
    - correspond to the case when each equipment transmits the data together with his own synchronization signal;
      - all equipment must have the same clock synchronized from an external source;
  - Contradirectional interfaces;
    - the multiplexer transmit the synchronization information for both transmission directions;
      - it is not necessary an external synchronization source;

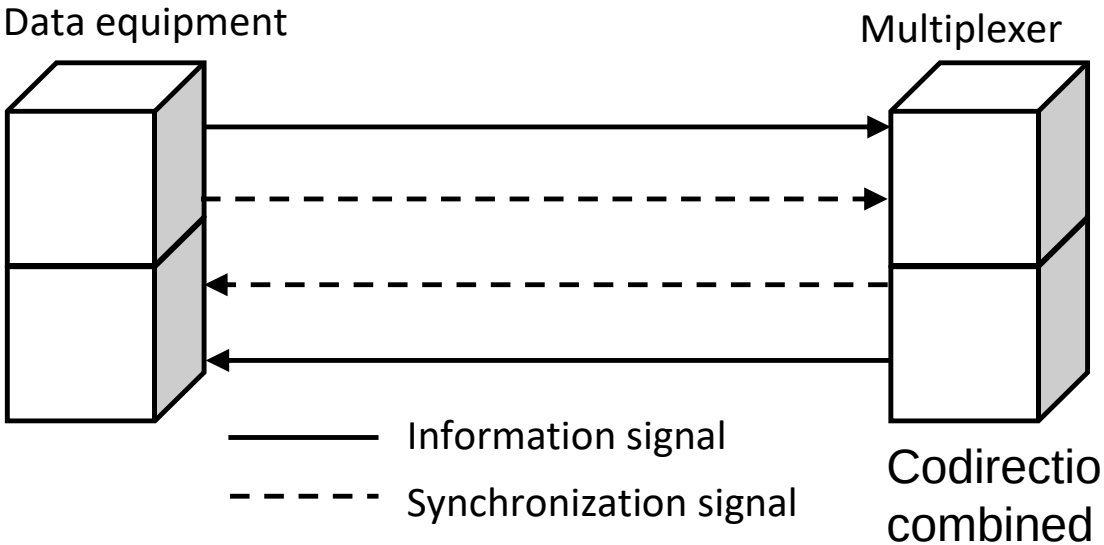
Terminal – multiplexer interface



- Codirectional interfaces;
  - A complex signal, combining both the information and the synchronization signals (bit clock and byte clock) is transmitted between the connected equipment;
  - A single channel composed of a pair of wire is used in each directions;
    - separation transformers are usually used.
  - Precision of the clock signal: at least ±100ppm;
  - The clock generator of each equipment (multiplexer or terminal equipment) is synchronized with an external reference clock;

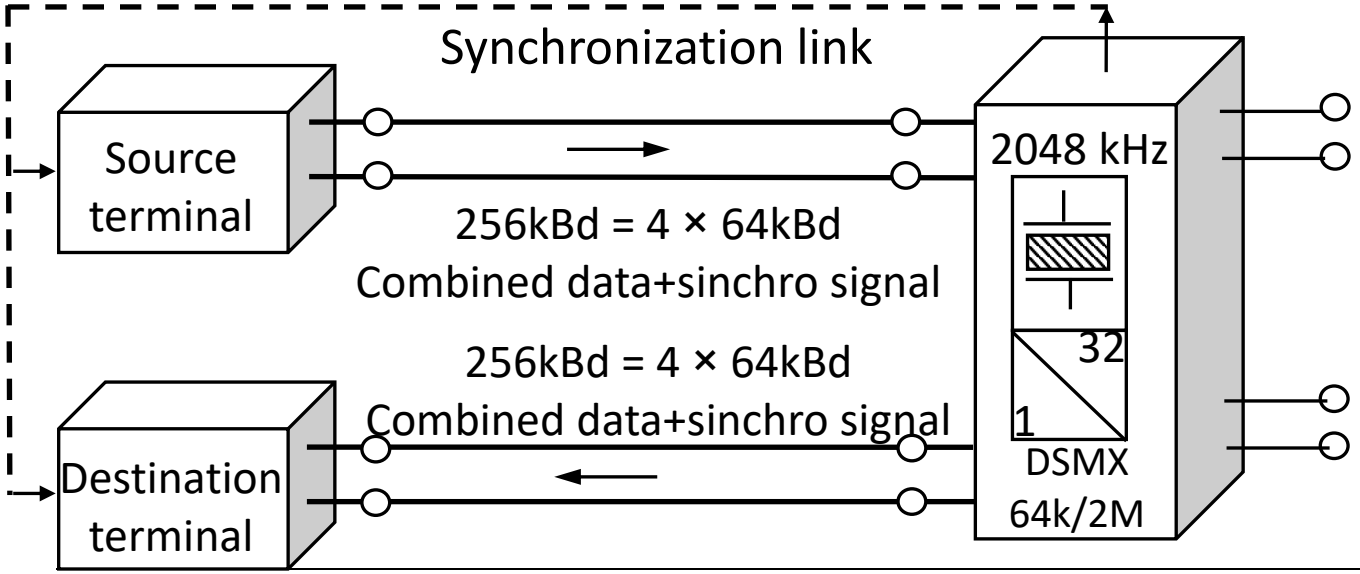
Terminal – multiplexer interface



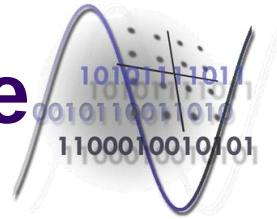


Codirectional interface – principle;
channels used;

Codirectional interface – technical details;
combined data and synchronization channels



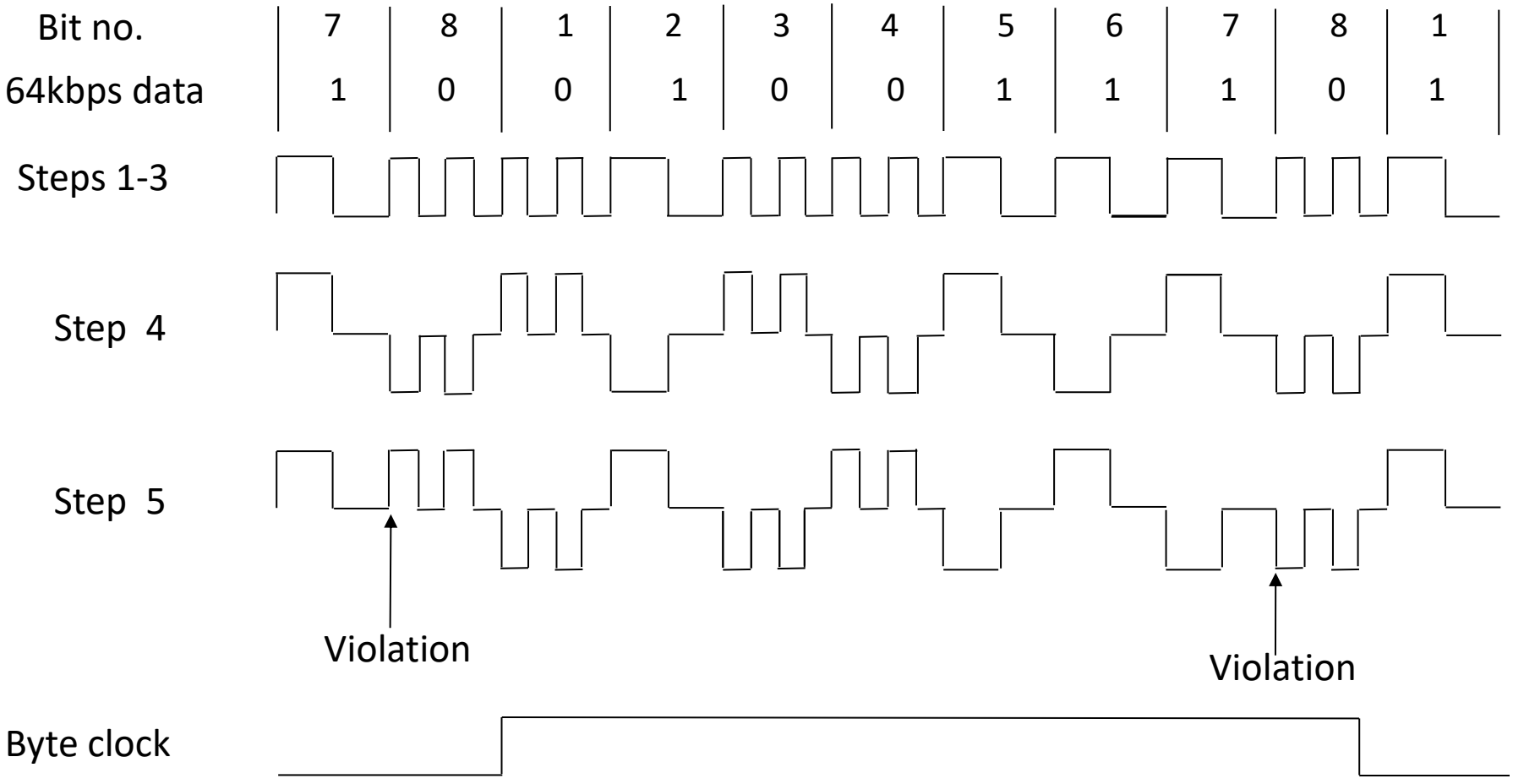
Terminal – multiplexer interface



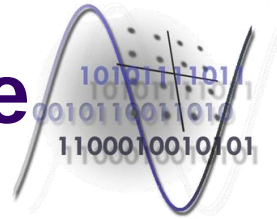
- Codirectional interface – the coding rule;
  - step 1: the period corresponding to the 64kbps rate is split in 4 unit intervals;
  - step 2: a binary “1” (64kbps rate) is coded as a block of 4 binary symbols (each having a period 4 times smaller): “1 1 0 0”; “0” represents 0V;
  - step 3: a binary “0” (64kbps rate) is coded as a block of 4 binary symbols (each having a period 4 times smaller): “1 0 1 0”;
  - step 4: the coded data signal is converted into a 3 level signal by alternating the polarity of consecutive blocks of 4 symbols;
  - step 5: the alternation of the polarity of the blocks is violated every 8^{th} block, meaning the position corresponding to bit 8 in a byte;
    - in this way can be realized the byte level synchronization between the two equipment.

Terminal – multiplexer interface

- Codirectional interface – coding rule;

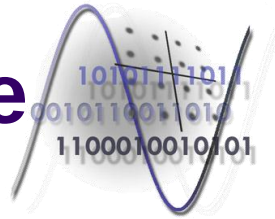


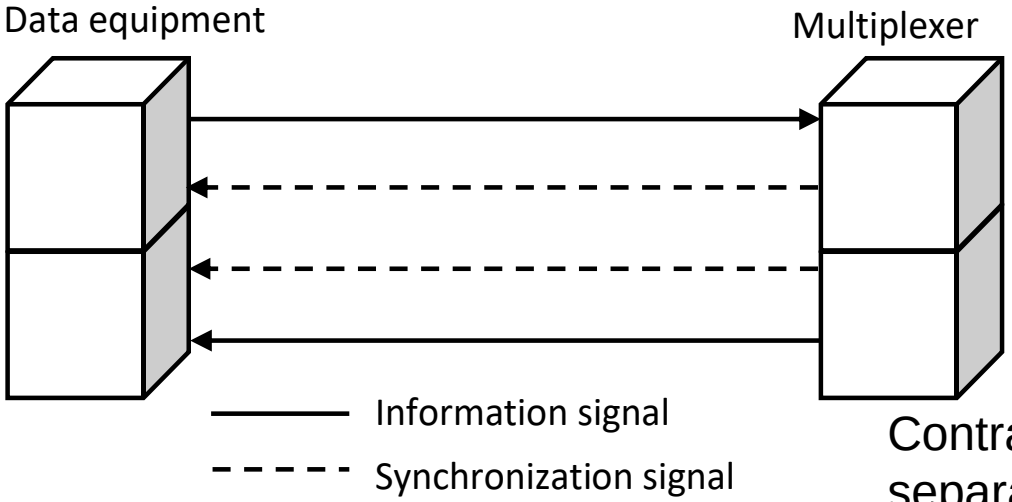
Terminal – multiplexer interface



- Contradirectional interfaces;
  - Both the data signal and the synchronization signal is transmitted between equipment;
  - The synchronization signal is transmitted from multiplexer to terminal equipment;
  - There are necessary two channels, each on a pair of wire, in both directions: data and synchronization
    - bit clock and byte clock;
  - Precision of the clock signal: at least ±100 ppm;
  - It is not necessary an external reference clock;

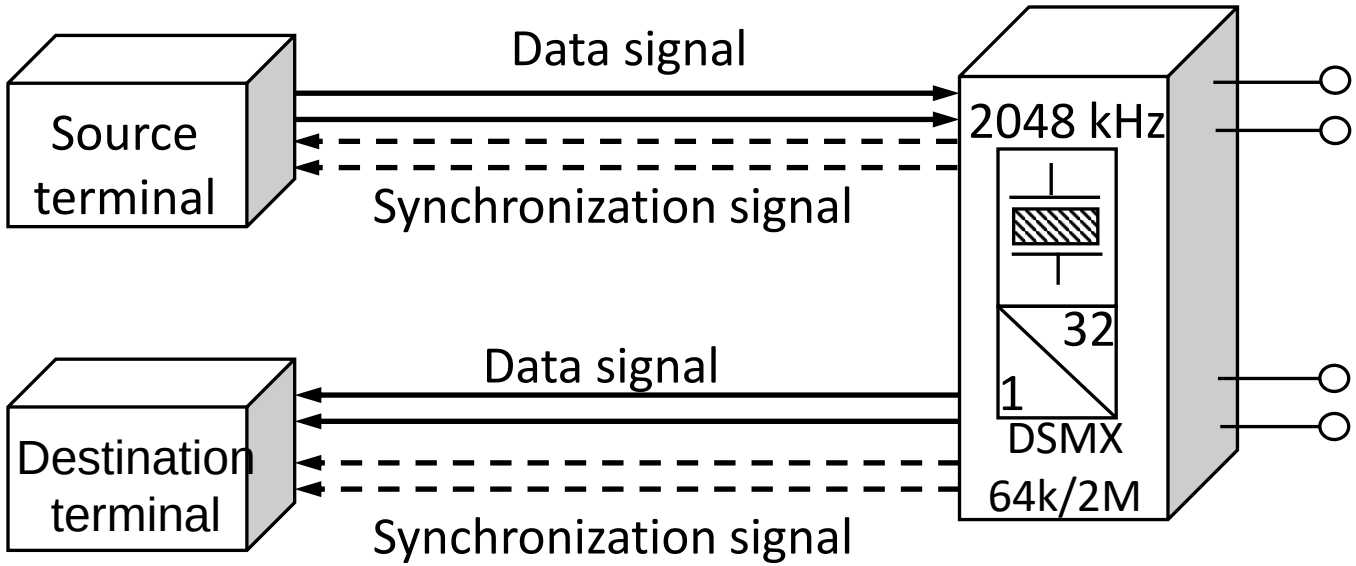
Terminal – multiplexer interface





Contradirectional interface – principle; channels used.

Contradirectional interface – technical details; separate data and synchronization channels.



Terminal – multiplexer interface

- Contradirectional interface – coding rule;
  - the clock signal transferred between equipment is transformed into a three level signal by alternating the polarity of consecutive nonzero impulses;
  - at the end of each byte (bit on position 8) is inserted a violation in the polarity alternation of the impulses;
    - it is realized a byte level synchronization between equipment.