Design with Microprocessors

Year III Computer Science

Lecturer: Tiberiu Marita
Overview

Objectives
• Know, understand and use concepts like: microprocessor, bus, memory system, i/o system and data transfer methods, interfaces.
• Analyze and design a system with a microprocessor

Prerequisites
• Logic Design, Digital System Design, Computer Architecture, Assembly Language Programming, Computer Programming (C language)

Discipline structure
• 2C + 1L + 1P / week

Lecture structure
• Part 1 – ATMEL (ATmega2560, ATmega328P ) and applications
• Part 2 – MP systems design issues (examples with x86 family)

LP topic
• Practical work with the Arduino boards (ATmega2560 (MEGA2560), ATmega328P(UNO)) and several peripheral modules (www.arduino.cc)
Evaluation

**Evaluation:** exam mark (E) + lab/project mark (LP)

```plaintext
if (LP >= 5) AND (E >= 4.5)
    Final_mark = 0.5 *LP + 0.5 *(E + Bonus)
else
    Final_mark = 4 OR Absent
```

**Bonus**

```plaintext
if no_of_attendances_at_the_lecture >= 5
    Bonus = (no_of_attendances - 4)* 0.1
```
Lecture References

Lecture documents

http://users.utcluj.ro/~tmarita/PMP/PMPCurs.htm

Textbook ATMega


Textbooks (8086 family µP)


• S. Nedevschi, L. Todoran, „Microprocesoare”, editura UTC-N, 1995 ⇒ UTCN Library

Additional documents

Data sheets from Atmel, Intel etc. (http://www.atmel.com/ )
Further study (for homework, lab & project)


Other books: [http://www.robofun.ro/carti](http://www.robofun.ro/carti)
Lecture 1:
Introduction to MP based systems.
Introduction to AVR MCUs
What is a Microprocessor?

A microprocessor / microcontroller incorporates most or all of the functions of a central processing unit (CPU) on a single integrated circuit (IC).

A Central Processing Unit (CPU) is a logic machine that can execute computer programs.

The fundamental operation of most CPUs, regardless of the physical form they take, is to execute a sequence of instructions called a program stored in some kind of computer memory. There are four steps that nearly all Von Neumann CPUs use in their operation: fetch, decode, execute, and writeback.

Die of an Intel 80486DX2 microprocessor (actual size: 12×6.75 mm) in its packaging.

Intel 80486DX2 microprocessor in a ceramic PGA package.
History


8 bit microprocessors: 8008 (1972), the world's first 8-bit microprocessor. These processors are the precursors to the very successful Intel 8080 (1974), Zilog Z80 (1976), and derivative Intel 8-bit processors. The competing Motorola 6800 was released August 1974. Its architecture was cloned and improved in the MOS Technology 6502 in 1975, rivaling the Z80 in popularity during the 1980s

16 bit (Intel 8086, 8088, 80186, 80286, 8086 SX, TMS 9900)


64 bit (most of nowadays microprocessors)

Types:

RISC: MIPS (R2000, R3000, R4000), Motorola 88000, ATmega (Atmel)

CISC: VAX, PDP-11, Motorola 68000, Intel x86 (each instruction can execute several low-level operations, such as a load from memory, an arithmetic operation, and a memory store, all in a single instruction)
2 level pipeline with EU si BIU, decoupled through a FIFO (4/6 bytes)
What is a Microprocessor based system?

Key components:
- CPU
- Memory
- Input/Output (I/O) ports

Additional devices:
- Interrupt controller
- DMA
- Dedicated I/O

Bus types:
- Address bus
- Data bus
- Control bus
A Typical PC Motherboard

- Processor (8088 up to 80486)
- Processor (8087 up to 80487)
- DMA controller (8237)
- Interrupt logic (8259)
- Expansion logic

- Disk Controller
- Video Card
- Expansion Slots

- System bus
- 640KB Dynamic RAM
- System ROM
- Timer logic (8253)
- Keyboard logic (8255)

- Speaker
- Keyboard
Additional devices can be included in the microcontroller chip:

- Re-programmable Flash memory and EEPROM
- Timer/Counters, PWM generators
- Serial Interfaces
- ADCs (Analog to Digital Converters) and DACs
Examples

Autonomous car/robot with lane-keeping and ACC functions (Digilent 2010 contest): http://www.youtube.com/watch?v=8797GgIC1WI

Other examples: every day usage (home appliances etc.)
BUSES

Address bus
- Unidirectional parallel signal lines connecting CPU and the memory
- Bus width; number of lines (wires), can be 16, 20, 24, 32, or 64 parallel signal lines.
- On these lines the CPU sends out the address of the memory location that is to be written to or read from.
- A CPU with \( n \) address lines can address \( 2^n \) memory locations. For example, a CPU with 16 address lines can address \( 2^{16} \) or 65,536 (64K) memory locations.

Data bus
- bus width: 4, 8, 16, 32 or 64 bits
- Bidirectional parallel signal lines (wires)
- Many devices can be connected to the data bus; but only one at a time can have its output enabled.
- Any device that is connected to the data bus must have three-state outputs, so it can be disabled if not being used.

Control bus
- consists of 4 to 10 parallel signal lines.
- CPU sends out signal on the control bus to enable the outputs of addressed memory or port devices
- Typical control bus signals: memory read, memory write, I/O read and I/O write.
Atmel 8-bit AVR MCU family

True RISC architecture
True single cycle execution
One MIPS per MHz
32 general purpose registers
Harvard architecture
1.8 to 5.5V operation
A variety of sleep modes - 6
Fast wake-up from sleep modes
Software controlled frequency
Single cycle and high code density
Large device range
Variety of pin counts
Full code compatibility
Pin/feature compatible families
One set of development tools

tinyAVR
1–8 kB program memory

megaAVR
4–256 kB program memory
Extended instruction set (multiply)

XMEGA
16–384 kB program memory
Extra: DMA, cryptographic support.

Application specific AVR
megaAVRs with particular interfaces:
LCD, USB, CAN etc.
AVR architecture

- Modified Harvard Architecture
  (http://en.wikipedia.org/wiki/Harvard_architecture)
AVR MCU

- RISC machine (Load-store type with 2 addresses)
- 2 level pipeline: IF & Execute
AVR micro-architecture

2 level pipeline: IF & Execute:
- Overlapping of the Instruction Fetch & Execute phases $\Rightarrow$ IPC $\sim$ 1 for most of the instructions
- 1MIPS/MHz (MIPS – Millions Instructions Per Second)

R = Read the operand
P = Process
W = Write the result to destination
Data SRAM (internal)

Figure 8-3.  On-chip Data SRAM Access Cycles

2 cycle access
ALU operations

 clk_{CPU}
 Total Execution Time
 Register Operands Fetch
 ALU Operation Execute
 Result Write Back

 T1 | T2 | T3 | T4
ATmega328P vs Atmega 2560

• High-performance, Low-power AVR® 8-bit Microcontroller
• Advanced RISC Architecture
  – 131 Powerful Instructions – Most Single Clock Cycle Exec.
  – 32 x 8 General Purpose Working Registers + Peripheral Control Registers
  – Fully Static Operation
  – Up to 16 MIPS Throughput at 16 MHz
  – On-chip 2-cycle Multiplier
• High Endurance Non-volatile Memory segments
  – 32KBytes of In-System Reprogrammable Flash
  – 1KBytes EEPROM
  – 2KBytes Internal SRAM
  – Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  – Data retention: 20 years at 85°C/100 years at 25°C(1)
• Peripheral Features
  – Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  – One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  – Real Time Counter with Separate Oscillator
  – Six PWM Channels
  – 8-channel, 10-bit ADC
  – Byte-oriented Two-wire Serial Interface
  – Dual Programmable Serial USARTs
  – Master/Slave SPI Serial Interface
  – Byte Oriented 2-wire Serial Interface
  – Programmable Watchdog Timer with On-chip Oscillator
  – On-chip Analog Comparator

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  – Fully Static Operation
  – Up to 16 MIPS Throughput at 16MHz
  – On-Chip 2-cycle Multiplier
• High Endurance Non-volatile Memory Segments
  – 256KBytes of In-System Self-Programmable Flash
  – 4Kbytes EEPROM
  – 8Kbytes Internal SRAM
  – Write/Erase Cycles:10,000 Flash/100,000 EEPROM
  – Data retention: 20 years at 85°C/ 100 years at 25°C
• Peripheral Features
  – Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
  – Four 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Mode
  – Real Time Counter with Separate Oscillator
  – Four 8-bit PWM Channels
  – Twelve PWM Channels with Programmable Resolution from 2 to 16 Bits
  – 8/16-channel, 10-bit ADC
  – Four Programmable Serial USART
  – Master/Slave SPI Serial Interface
  – Byte Oriented 2-wire Serial Interface
  – Programmable Watchdog Timer with Separate On-chip Oscillator
  – On-chip Analog Comparator

The Memory and I/O maps for the 8086/8088 microprocessor.

(a) Isolated I/O.

(b) Memory mapped I/O.
AVR address spaces

ATmega 328P / 2560

Flash: 0x0000 – 0x3FFF / 0x1FFF
- Program Counter (PC) - 14 / 17 bits
- Program memory is addressable on words (2 bytes): 16K x 16 bits (32KB) / 128Kx16 bits (256 KB)
- Program memory cannot be extended

Data memory: is addressable on bytes
Registers: 32 GPR, 64 I/O, 160/416 extended I/O
(0x0000 – 0x001F): General purpose registers (GPR):
(0x0020 – 0x005F): direct I/O access or as memory
(0x0060 – 0x00FF / 0x01FF): Extended I/O in SRAM,
access with ST/STS/STD si LD/LDS/LDD
(0x0100 – 0x08FF / 0x0200 – 0x21FF): internal SRAM

Atmega 328P (Data Memory)

| Address (HEX) |
|---|---|
| 0 - 1F |
| 20 - 5F |
| 60 - 1FF |
| 200 |
| 21FF |
| 2200 |

ATmega 2560 (Data Memory)

| Address (HEX) |
|---|---|
| 0x0000 - 0x001F |
| 0x0020 - 0x005F |
| 0x0060 - 0x00FF |
| 0x0100 |
| 0x08FF |
| FFFF |
• 32 x 8-bit GPR (R0 – R31);
• 1 cycle read/write

Groups of registers:
R(0:15), R(16:31), R(26:31) – various possible usage
X, Y, Z, (16 bits); indirect addressing of instruction and data memory

Requirements for the register block: 1 cycle operations
• 1x 8-bit r, 1x 8-bit w
• 2x 8-bit r, 1x 8-bit w
• 2x 8-bit r, 1x 16-bit w
• 1x16-bit r, 1x 16-bit w