Design with Microprocessors

Year III Computer Science
1-st Semester

Lecture 10: Introduction to the x86 μP

Lecture References for x86

Textbooks

Barry B. Brey, The Intel Microprocessors: 8086/8088, 80186,80286, 80386 and 80486. Architecture, Programming, and Interfacing, 4-th edition, Prentice Hall, 1994.

S. Nedevschi, L. Todoran, „Microprocesoare”, editura UTC-N, 1995
$\Rightarrow$ UTCN Library

Additional documents:

http://users.utcluj.ro/~tmarita/PMP/Lecture

Data sheets from Intel, AMD etc.

Intel x86 History

4 bit microprocessors: Intel's 4004 (1971),

8 bit microprocessors: 8008 (1972), the world's first 8-bit microprocessor. These processors are the precursors to the very successful Intel 8080

16 bit (Intel 8086, 80186, 80286, 80386 SX)

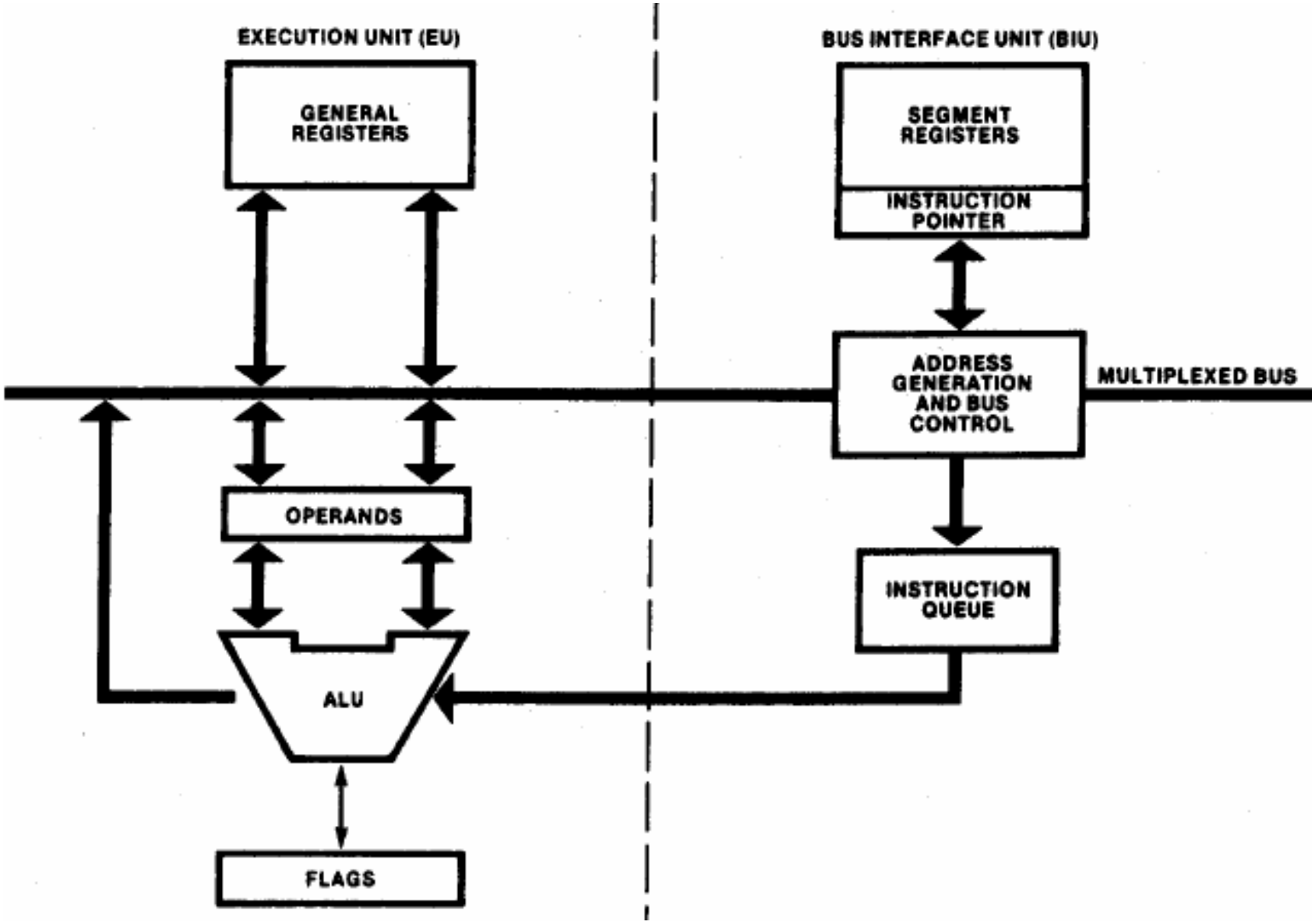
32 bit (Intel 80386DX, 80486DX, Pentium)

64 bit (most of nowadays microprocessors)

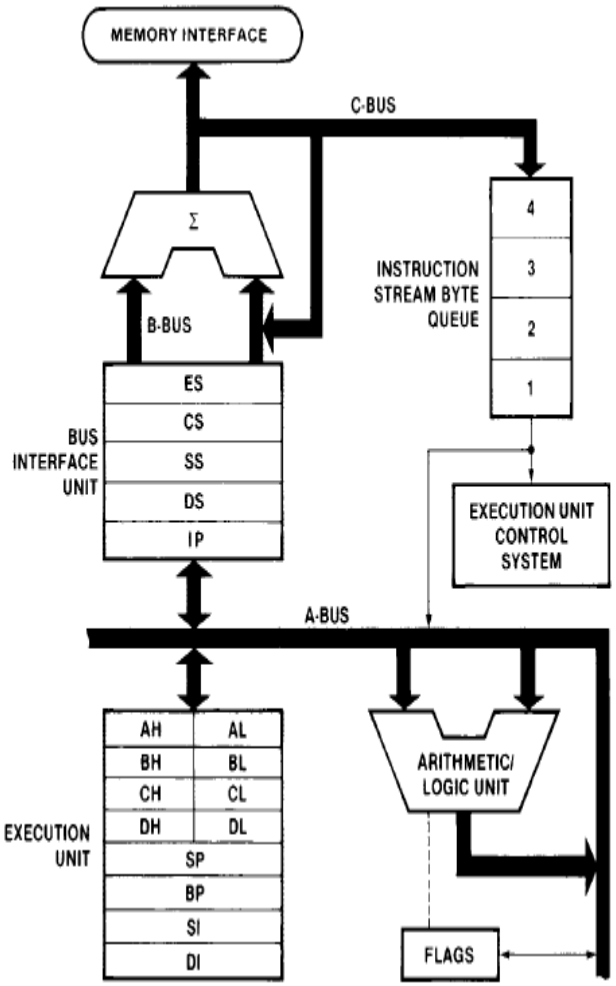
Architecture type:

CISC: - each instruction can execute several low-level operations, such as a memory load, an arithmetic operation, and a memory store, all in a single instruction

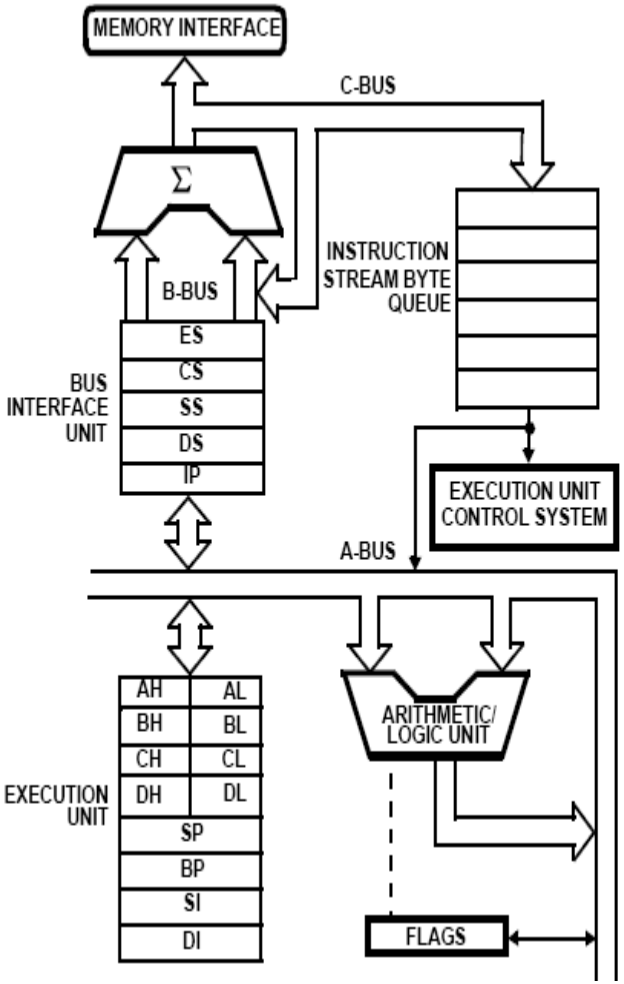
8086/8088 bloc diagram



8086/8088 bloc diagram



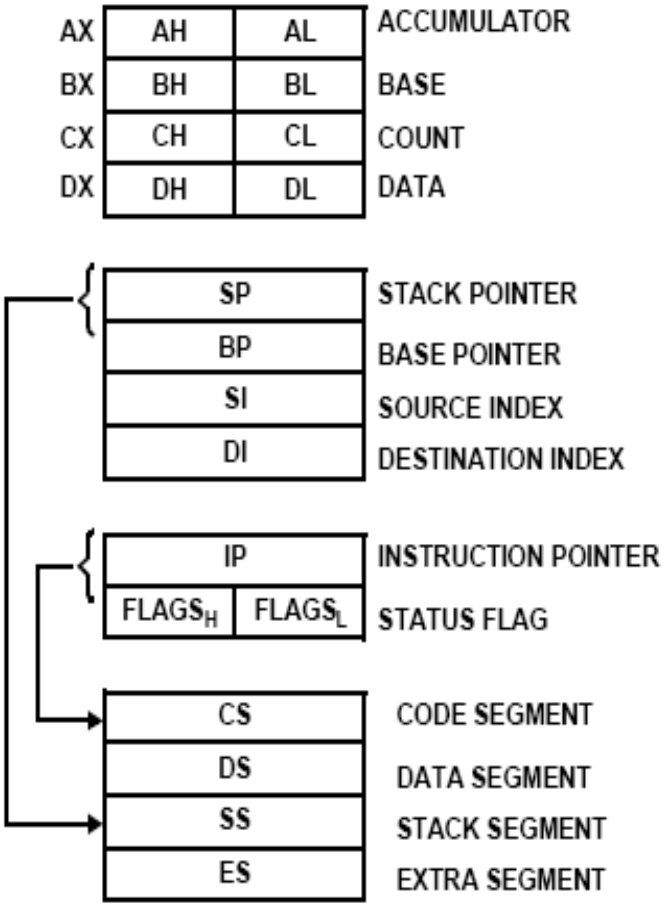
8088



8086

2 level pipeline with EU si BIU, decupled through a FIFO (4/6 bytes)

8086 registers



Multipurpose:

AX – accumulator

BX – base index (offset address in memory)

CX – count (REP, LOOP, shift, rotate …)

DX – data (MUL, DIV)

BP – pointer to a memory location

DI – destination address for string instructions

SI – source address for string instructions

Special purpose:

IP – address of the next instruction

SP – addresses of the topmost (free) element of the stack

FLAGS – status and control

Segment:

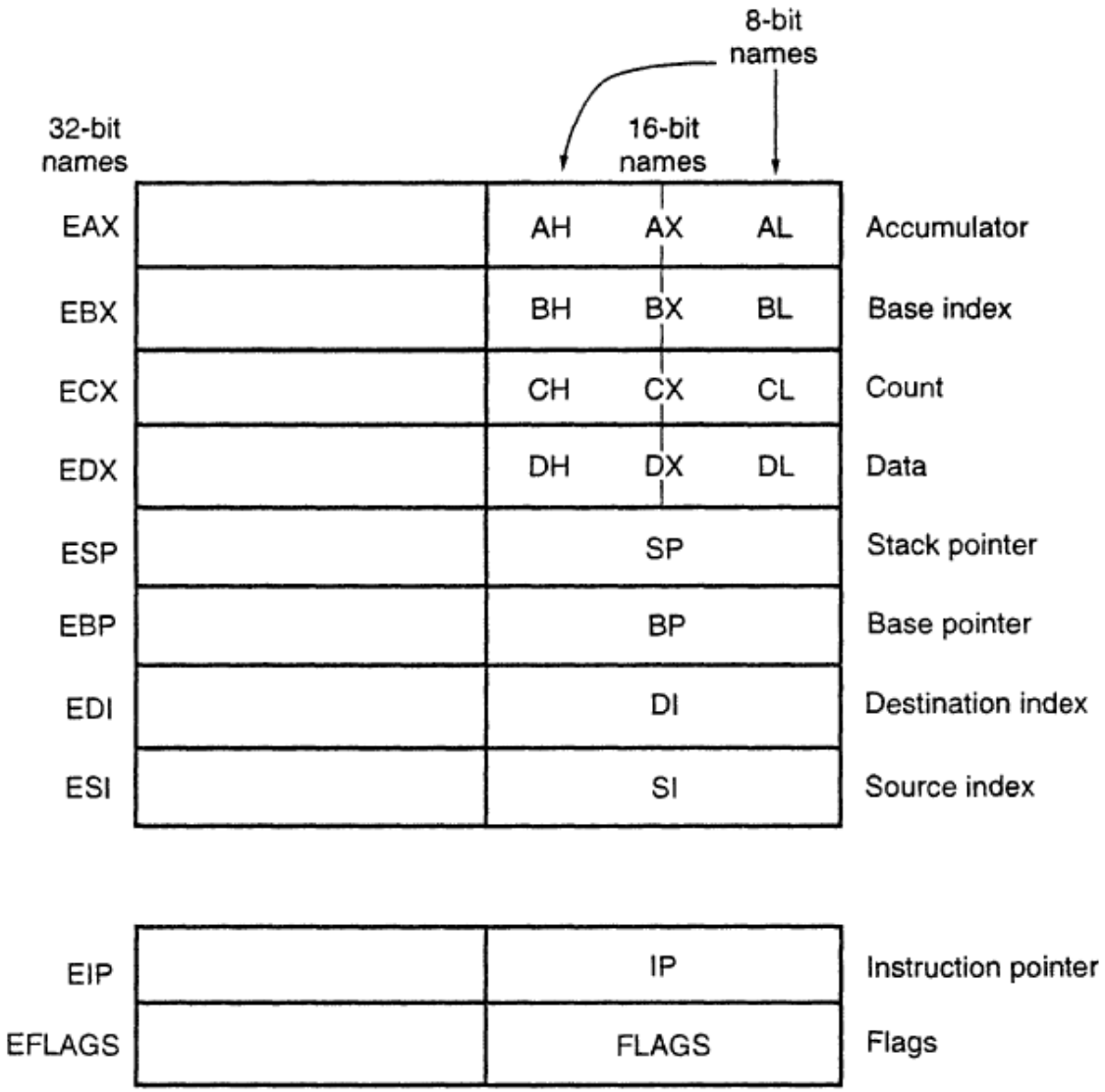
CS - starting address of a 64KB memory block that holds the code

DS - starting address of a 64KB memory block that holds the data

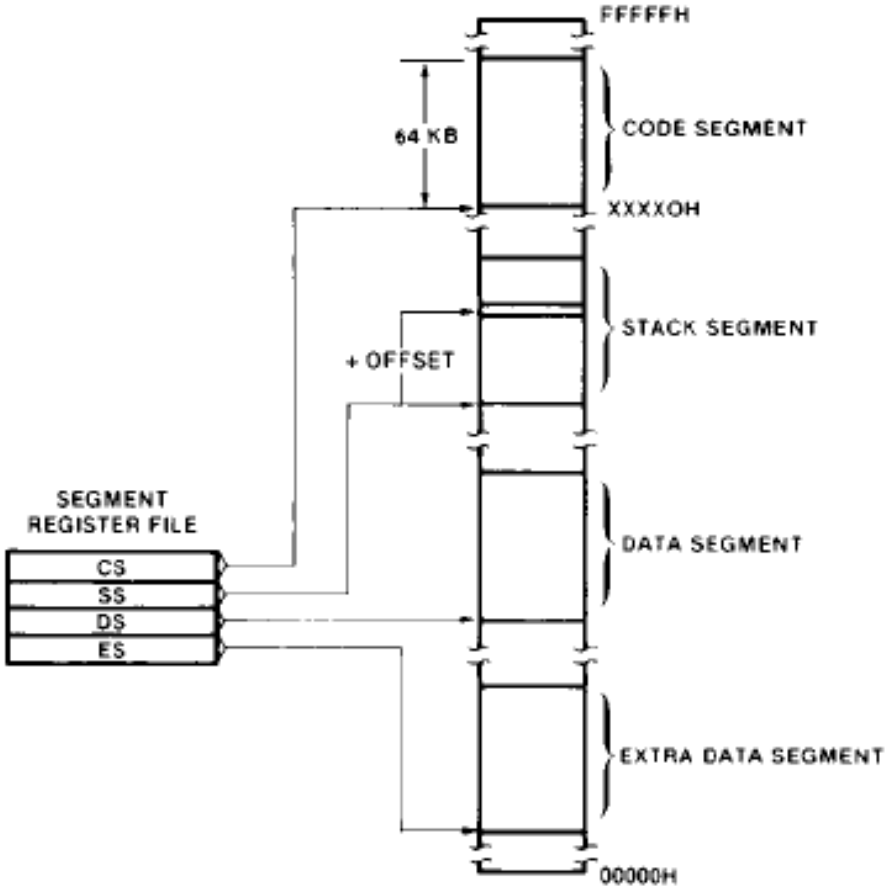
ES – additional data segment used by string instr. to hold destination data

SS - stack segment

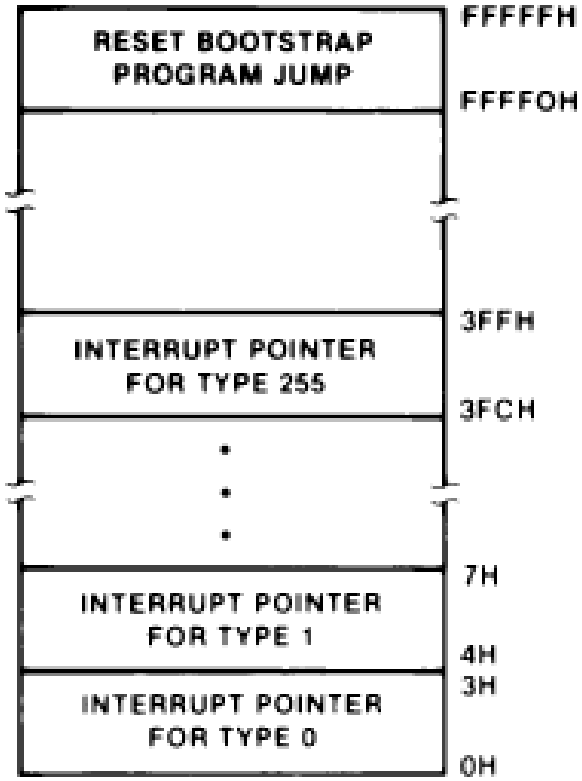
x86 registers



Real mode memory addressing

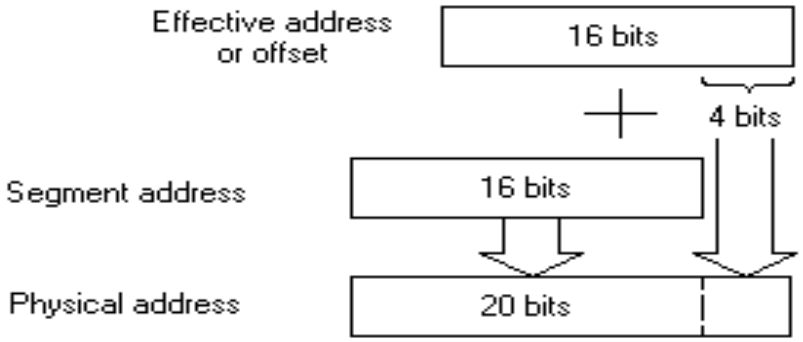


Segmented memory



Reserved memory locations:
- IVT – interrupt vectors table
- Reset address - FFFF0H:
  IP = 0000H, CS = FFFFH

Real mode memory addressing

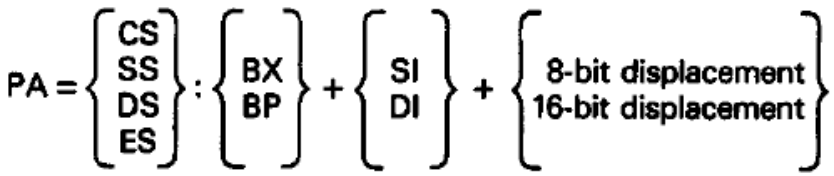


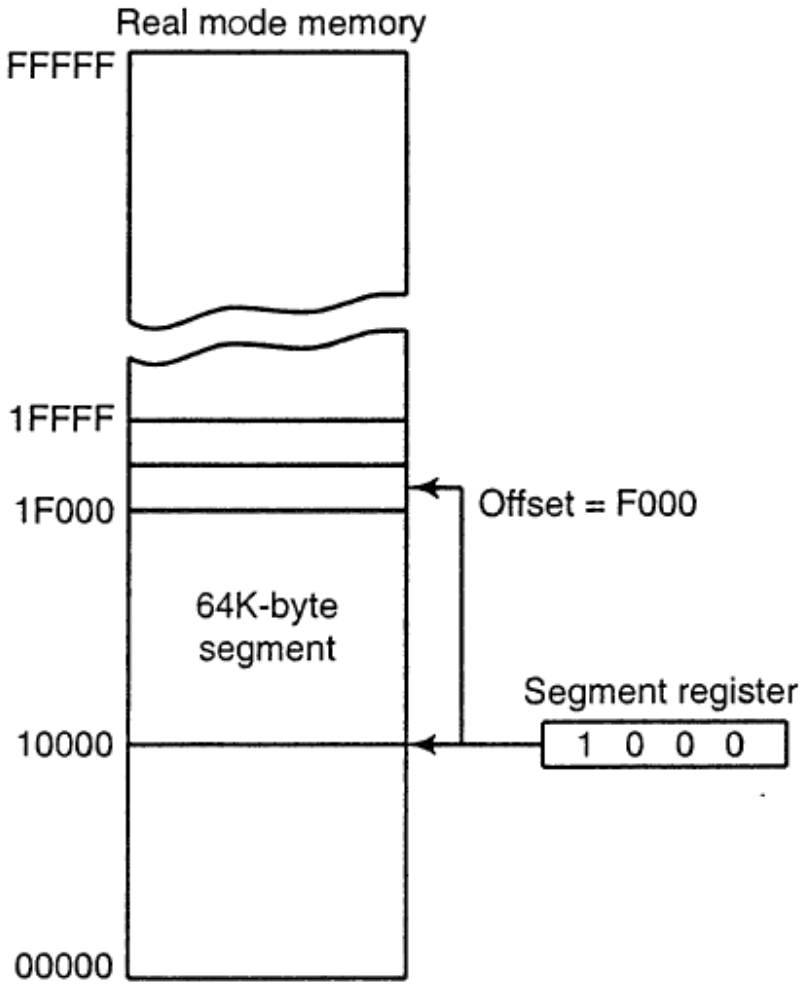
Physical address = 16*Segment + offset

Ex: Code= 16*CS +IP

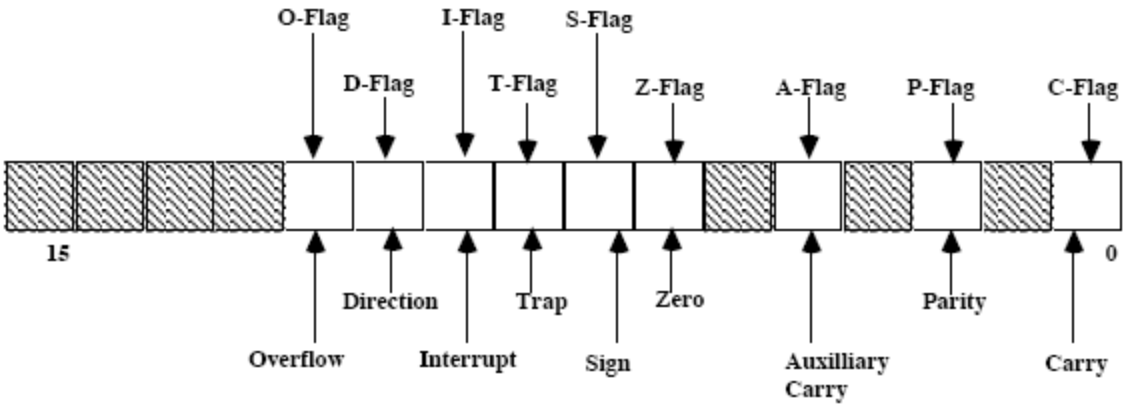
Segment	Offset	Special purpose
CS	IP	Instruction address
SS	SP or BP	Stack address
DS	BX, DI, SI, 8/16 bit numbers	Data address
ES	DI for string instructions	String destination address

16 bit segment and offset address combinations (8086 … 486, Pentium)





FLAGS



C (carry) – holds the carry bit after arithmetic or shift instructions

P (parity) – 0 for odd and 1 for even (count of number of ones) – obsolete

A (auxiliary carry) – holds the carry between bits 3 and 4 of the result (DAA/ DAS – BCD addition/subtraction)

Z (zero) – 1 if the result of an arithmetic/logic instruction is 0

S (sign) – sign of the result of an arithmetic/logic instruction (S=1 (MSB) – negative)

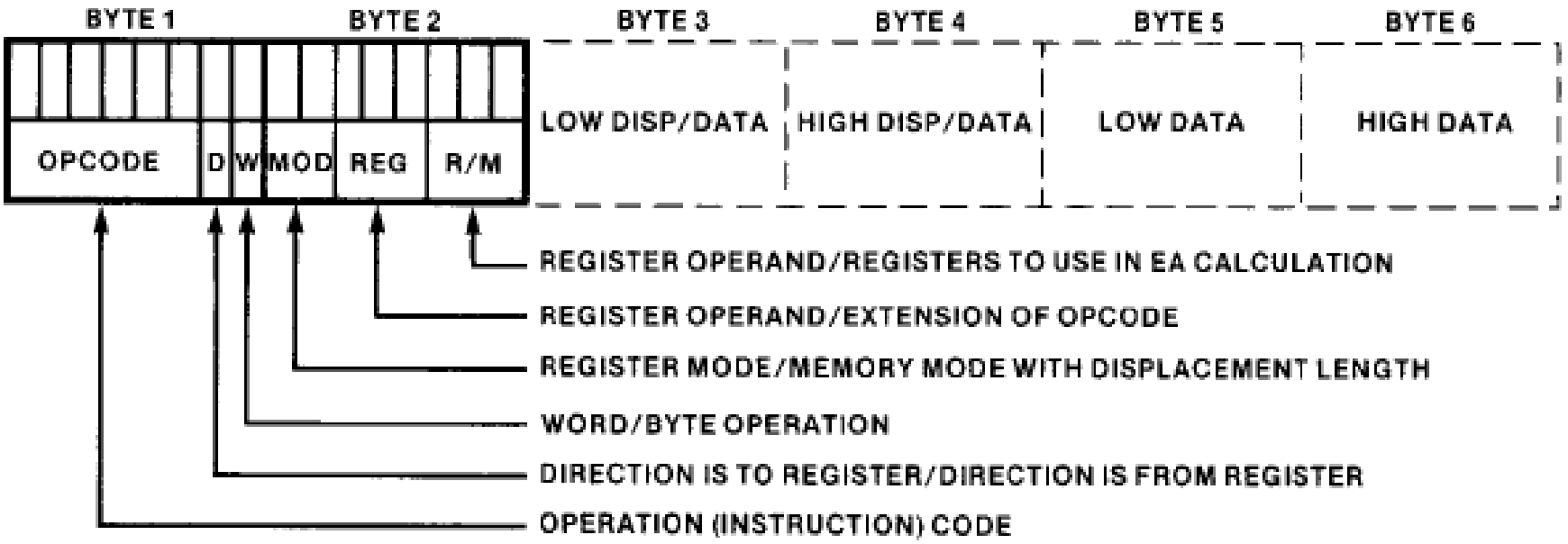
I (interrupt) – if 1 the interrupt system (INTR input) is enabled (STI/CLI)

D (direction) – increment (1) or decrement (0) the address (DI/SI) in string instr.

O (overflow) – overflow of the result capacity for signed addition or subtraction

T (trap) – T=1 ⇨ instruction flow is interrupted on conditions from debug/control reg. (debug)

8086 Instruction Format

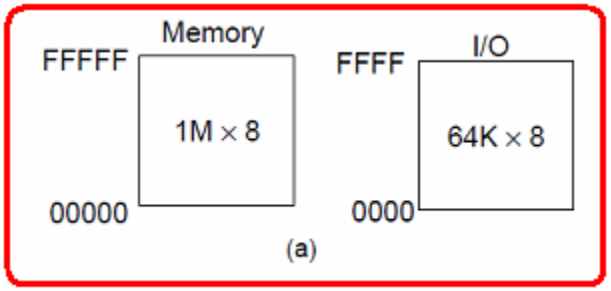


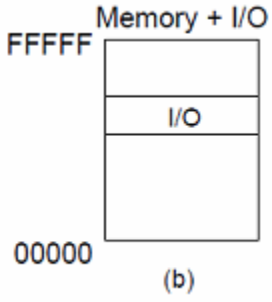
I/O address space

The Memory and I/O maps for the 8086/8088 microprocessor.

(a) Isolated I/O.

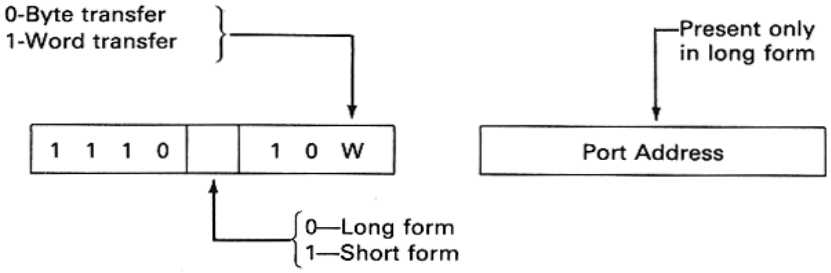
(b) Memory mapped I/O.





I/O instructions format

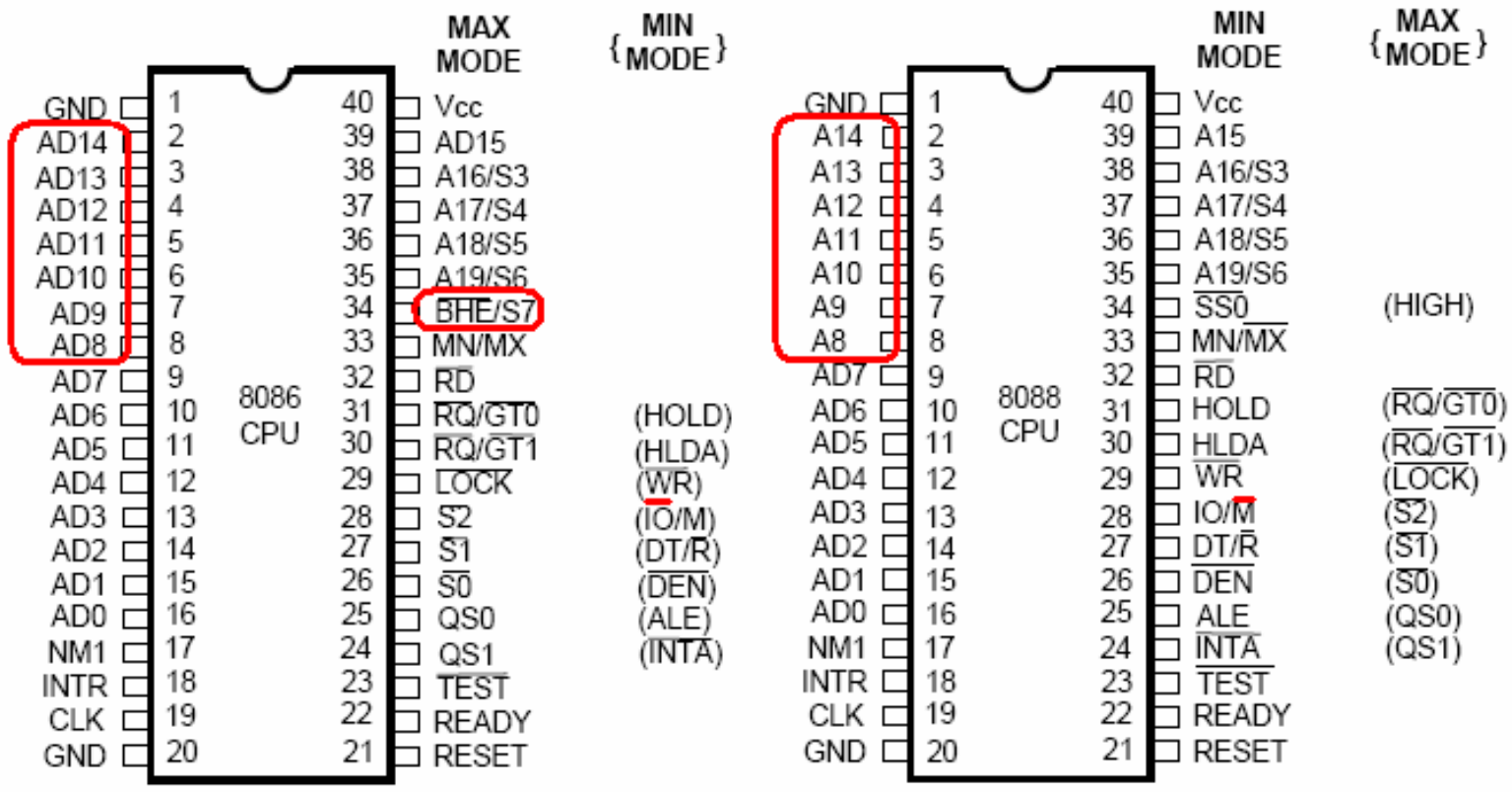
2 types: short (IN AL, DX) or long (OUT PORT,AL)



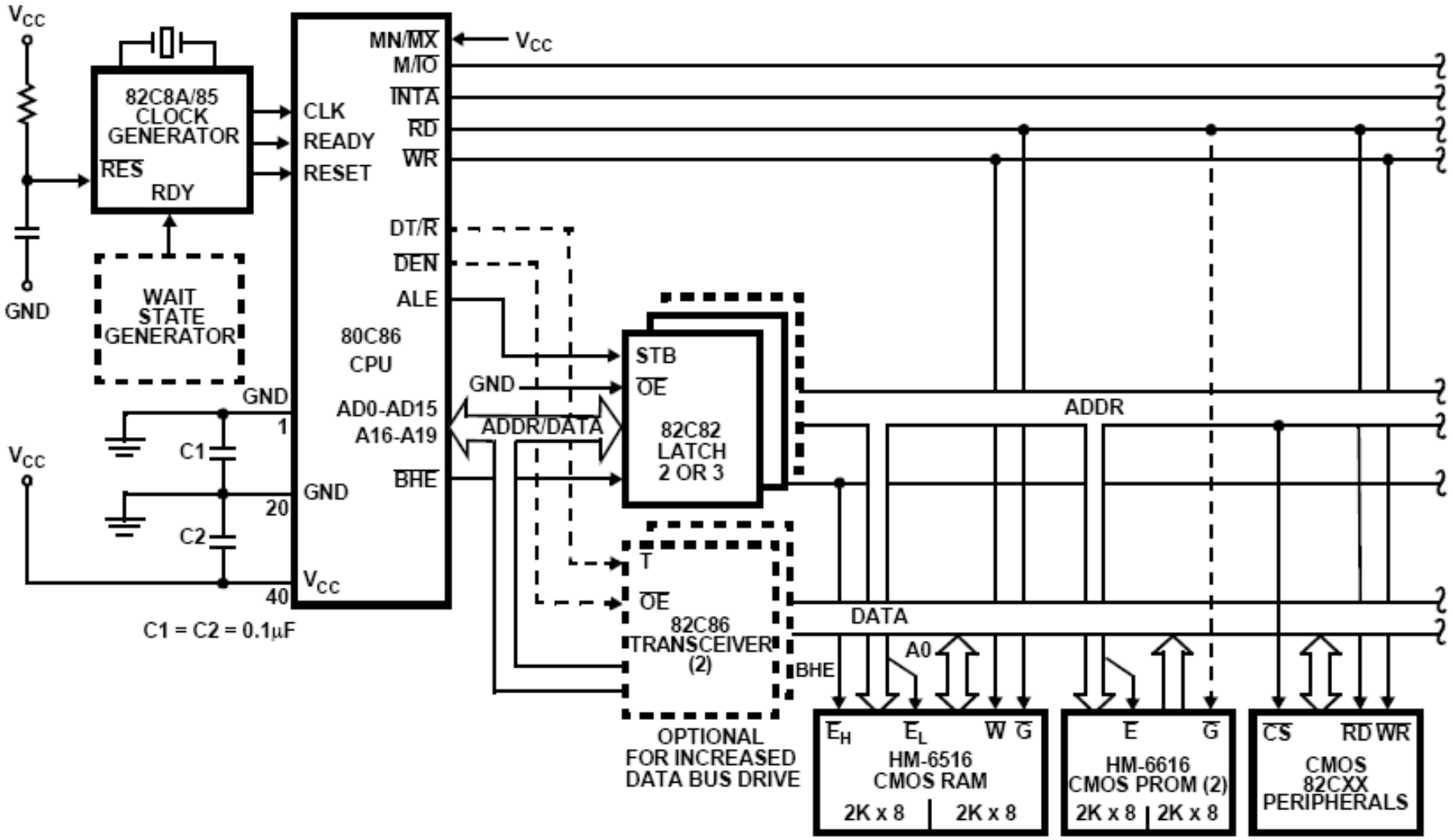

```
IN AL, PORT          (AL) <- (PORT)
IN AX, PORT          (AX) <- (PORT+1:PORT)
IN AL, DX            (AL) <- ((DX))
IN AX, DX            (AX) <- ((DX)+1:(DX))

OUT PORT, AL         (PORT) <- (AL)
OUT PORT, AX         (PORT+1:PORT) <- (AX)
OUT DX, AL           ((DX)) <- (AL)
OUT DX, AX           ((DX)+1:(DX)) <- (AX)
```

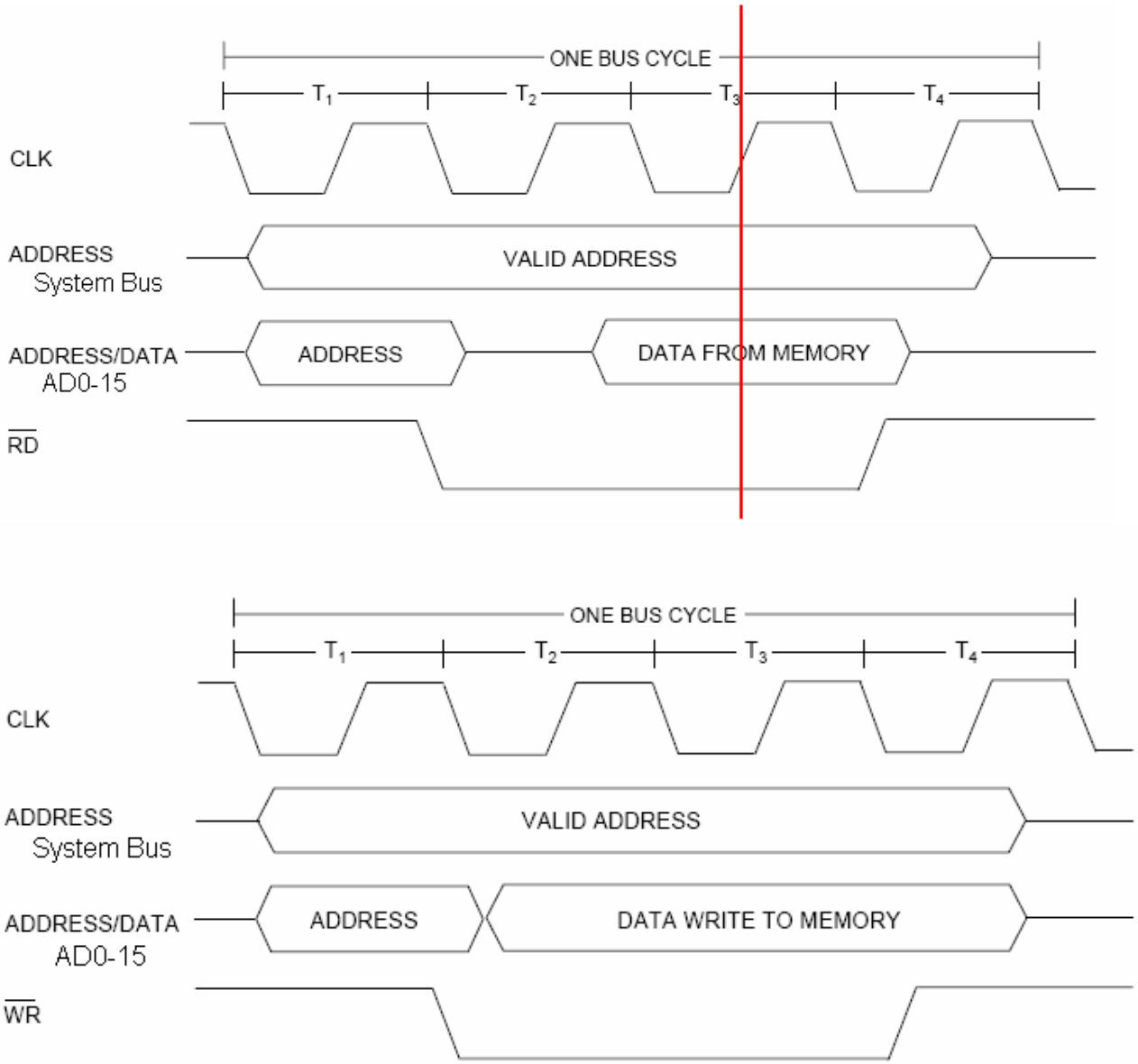
8088/8086 Family



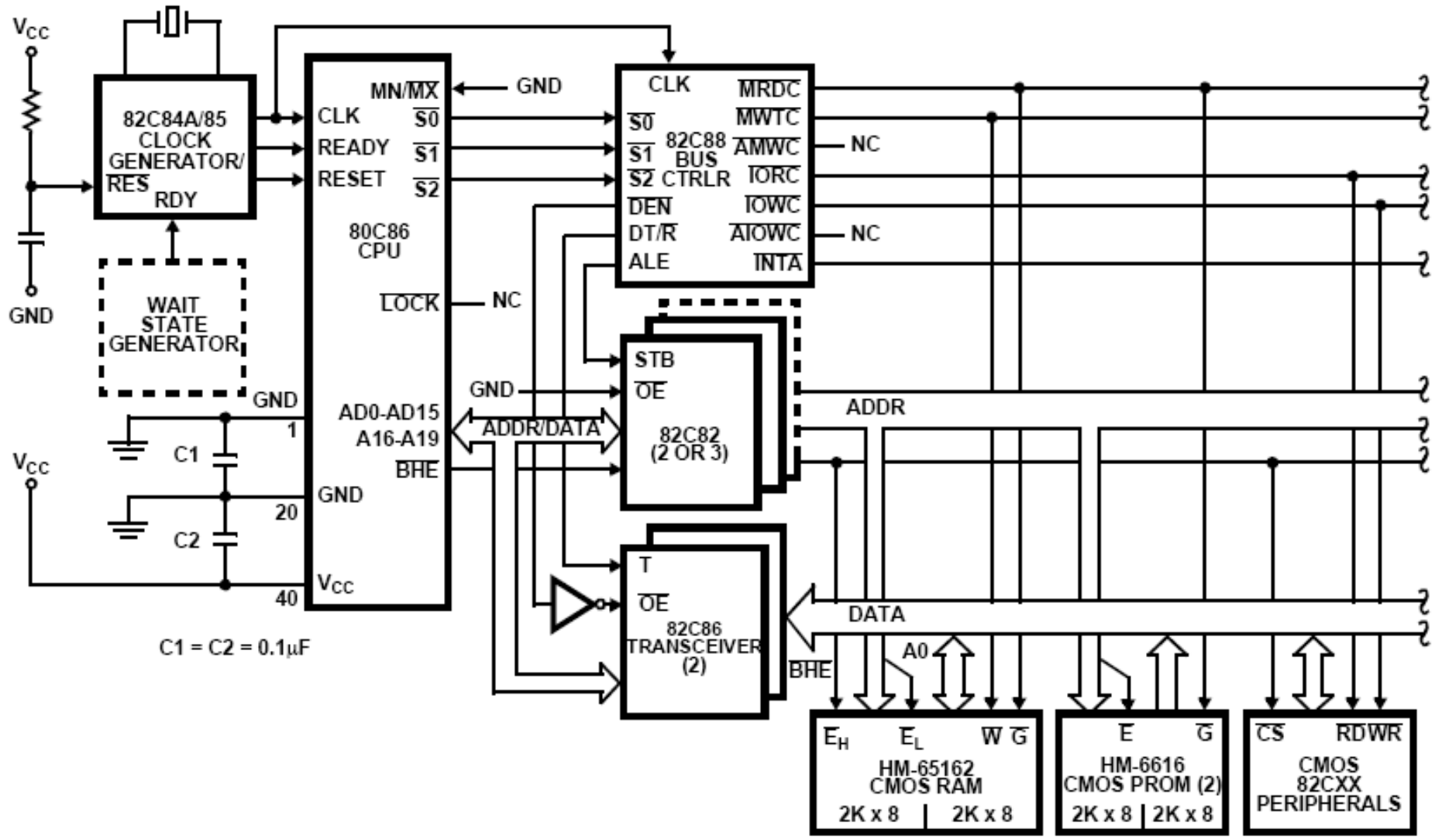
µP system with 8086 in minimum mode



Bus Timing (simplified)



µP system with 8086 in maximum mode

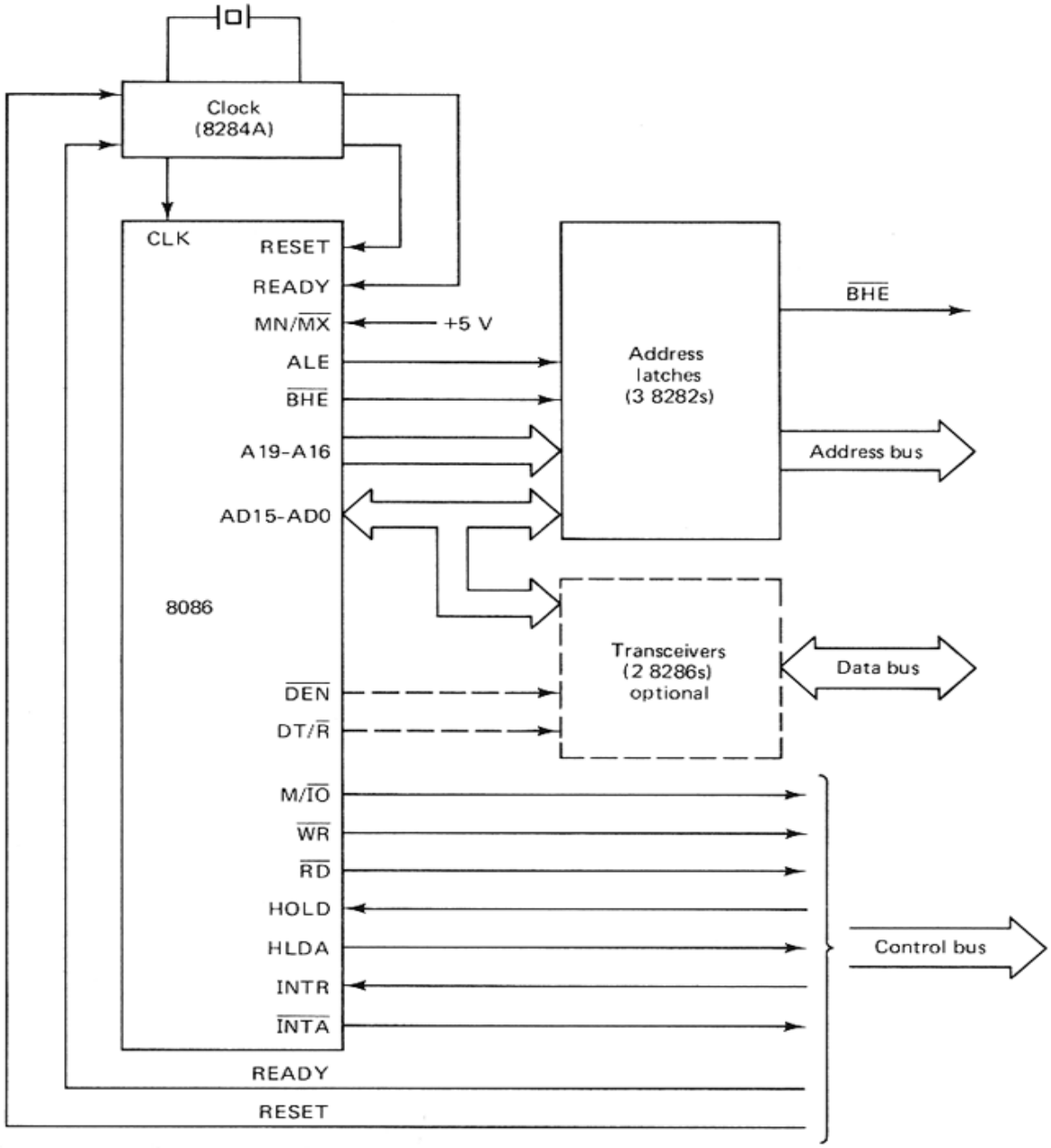


µP system with 8086 in maximum mode

82C88 (Bus controller) – commands generation based on the processor states ($\#S_2\#S_1\#S_0$)

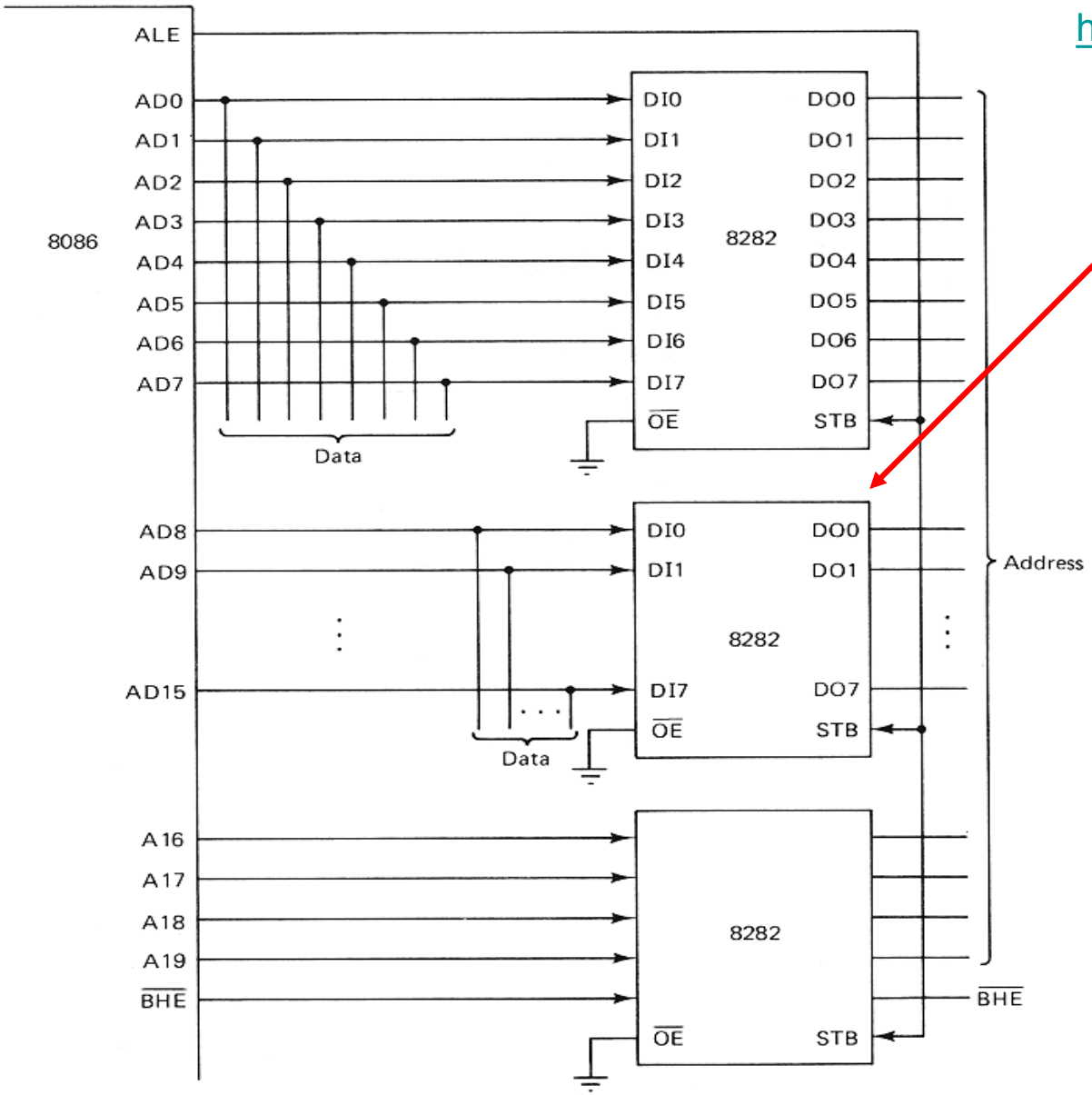
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	PROCESSOR STATE	82C88 COMMAND
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Connection of the 8086 in minimum mode to the system buses

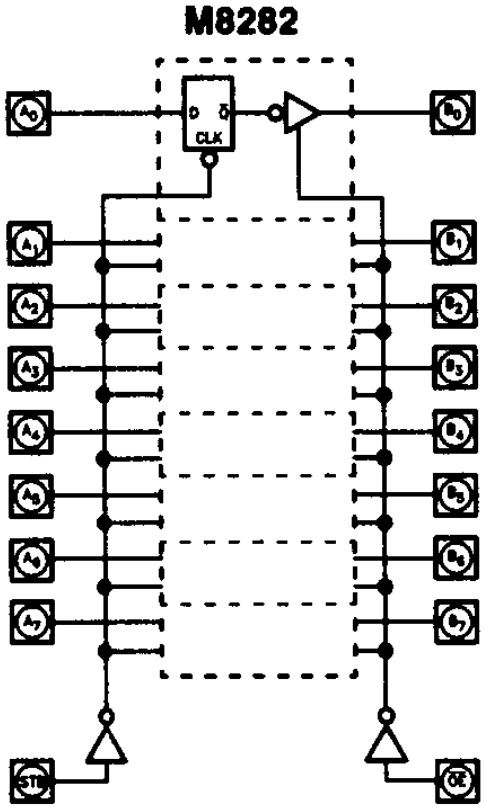


Note: In an 8088 system $\overline{BHE}$ is $\overline{SSO}$, M/$\overline{IO}$ is IO/$\overline{M}$, and only one 8286 is needed.

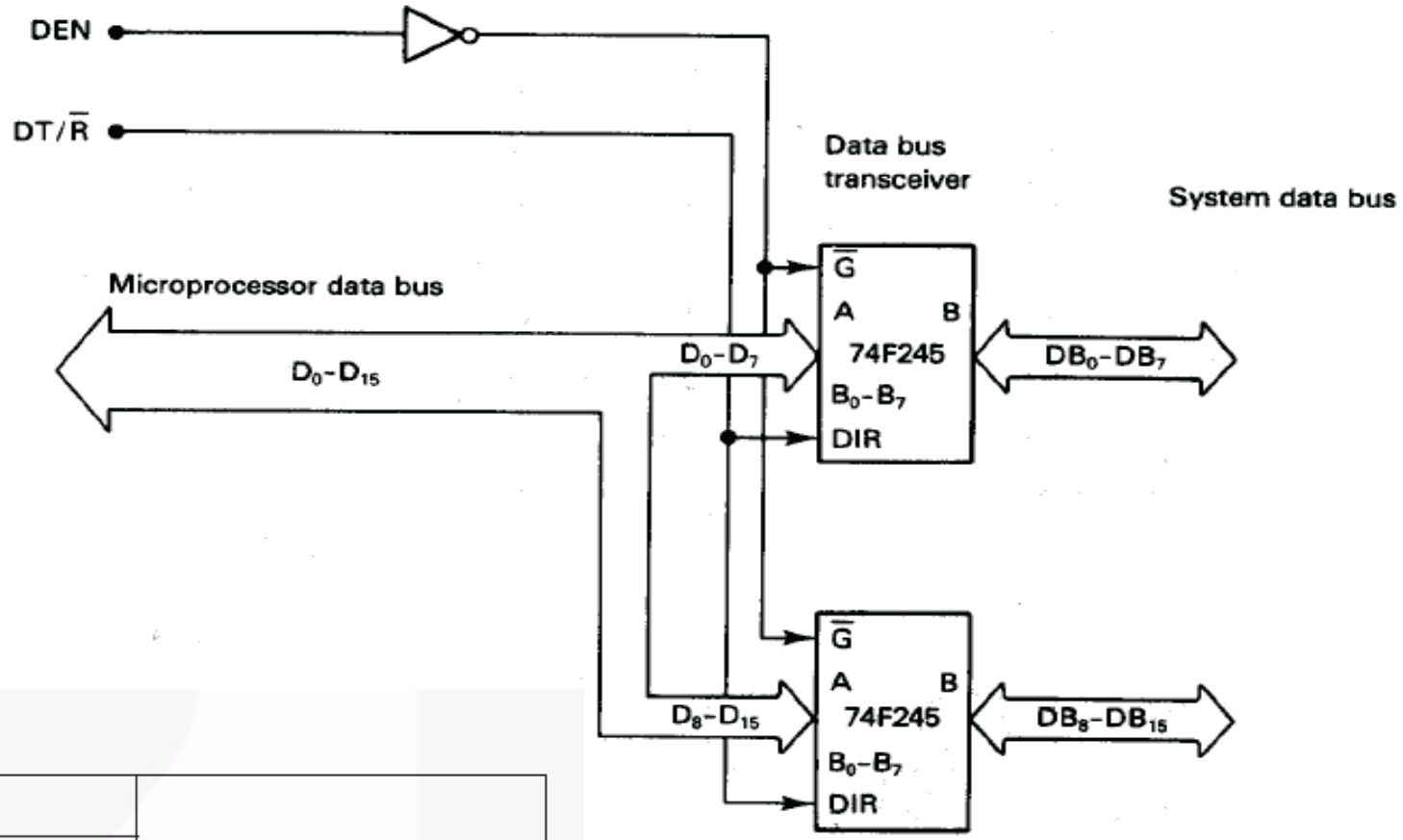
Address bus connection



http://www.datasheetarchive.com



Data bus connection



Truth Table

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Basic bus operations

Read or Write

μP (Register) $\Leftrightarrow$ Memory / I/O register (port)

MOV mem, reg

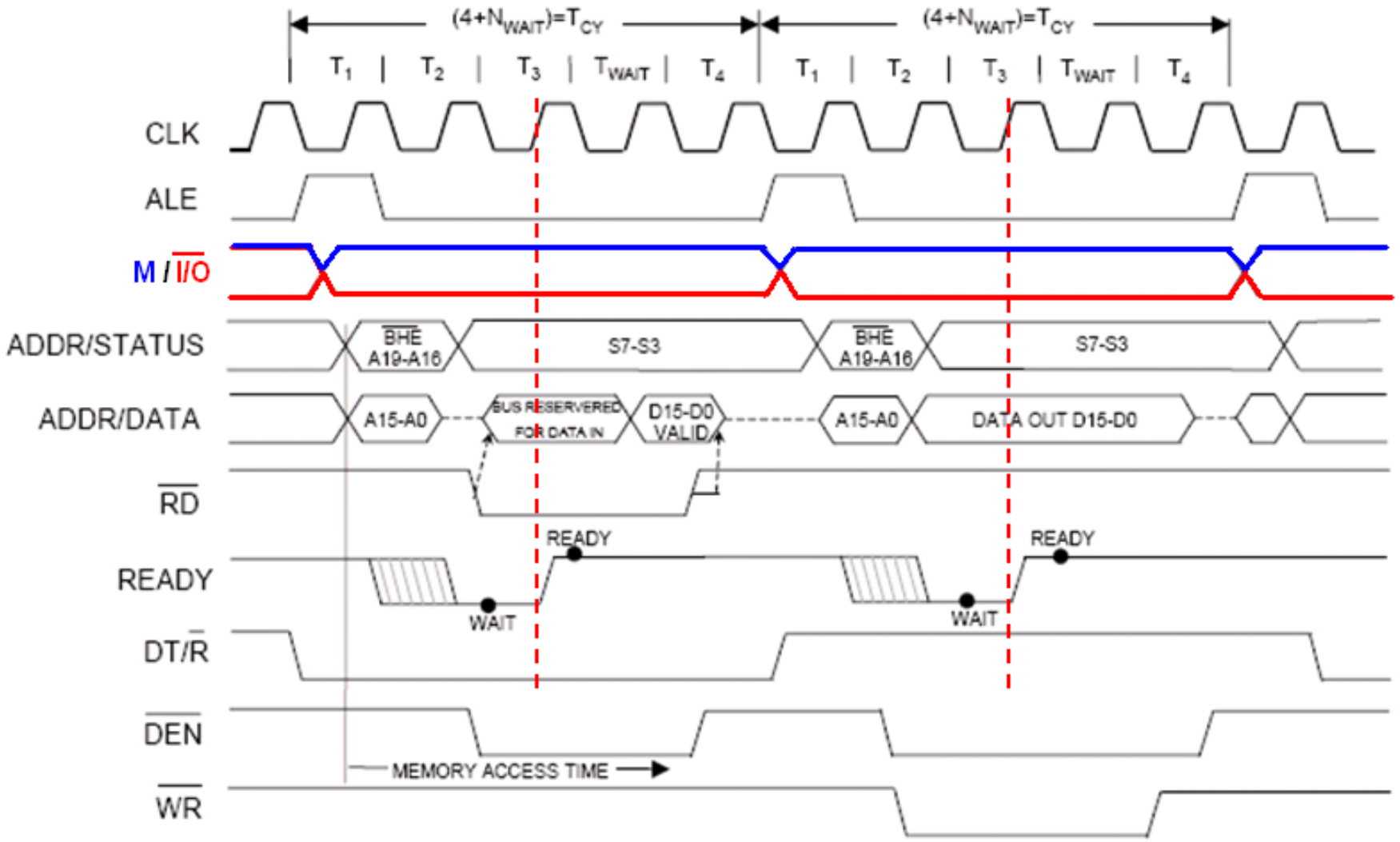
MOV reg, mem

MOV reg, reg

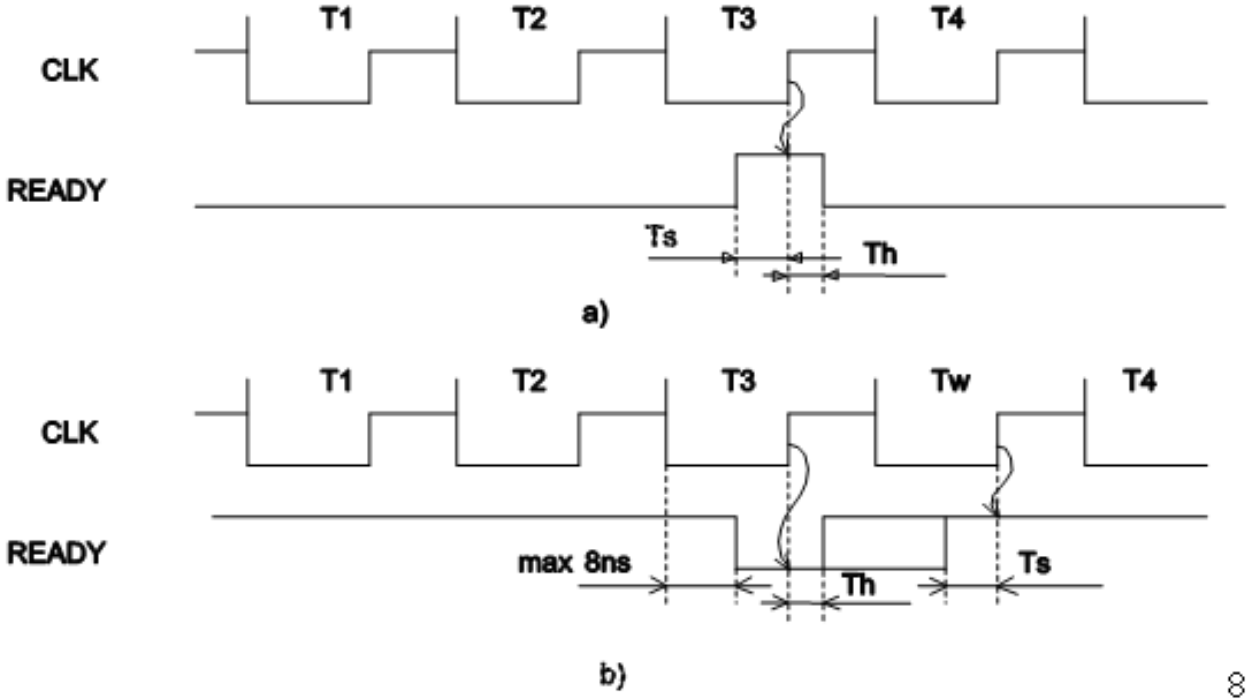
OUT port, regA

IN regA, port

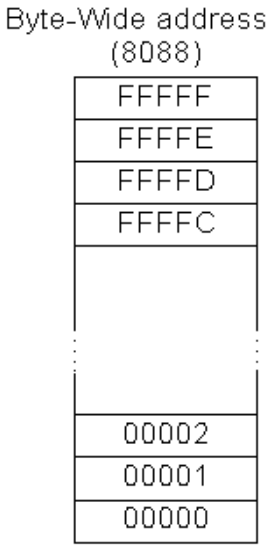
Bus Timing (detailed)

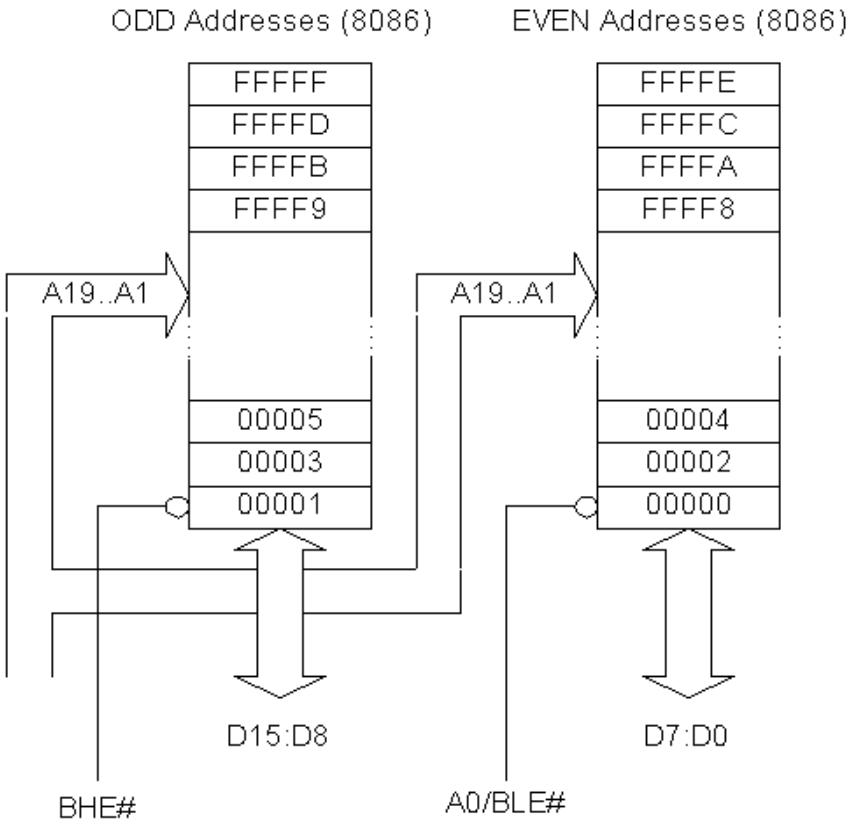


Wait States


T1
T2
T3
T4
CLK
READY
Ts
Th
a)
T1
T2
T3
Tw
T4
CLK
READY
max 8ns
Th
Ts
b)

Physical memory organization



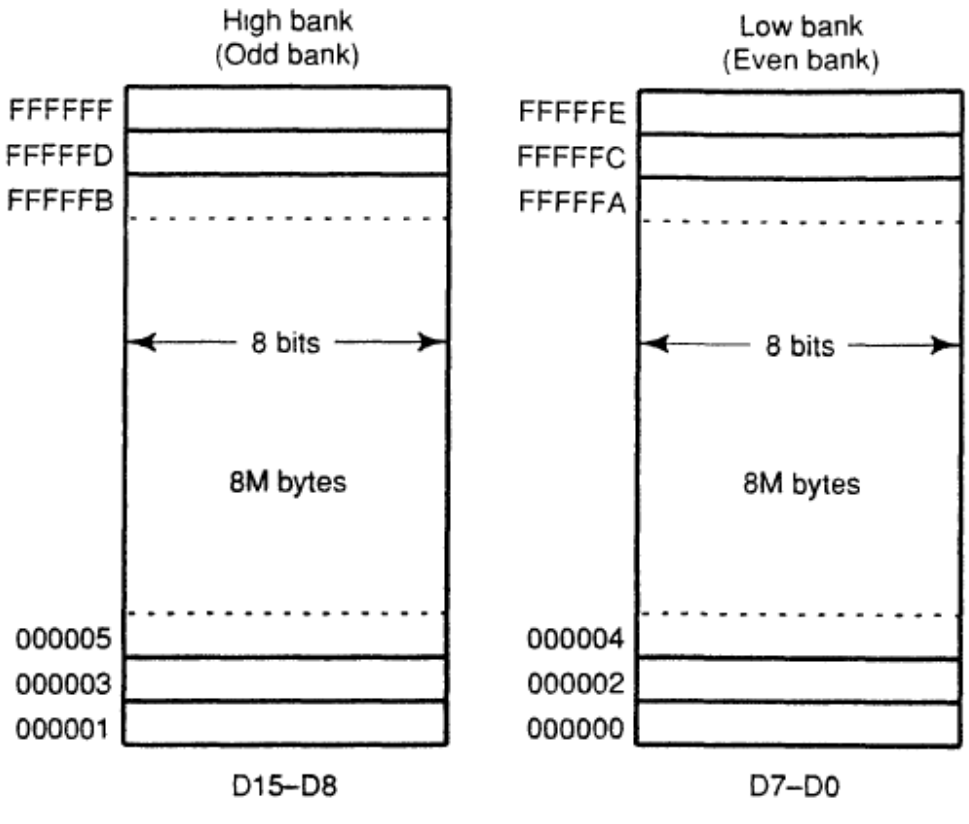


$\overline{BHE}$	A_0	Characteristics
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

Physical memory organization

Other 16 bit memory interfaces (286 … 386SX)

- With 24 bit address bus $\Rightarrow$ address space = 2^{24} = 16 MB (0 .. FF FF FF)



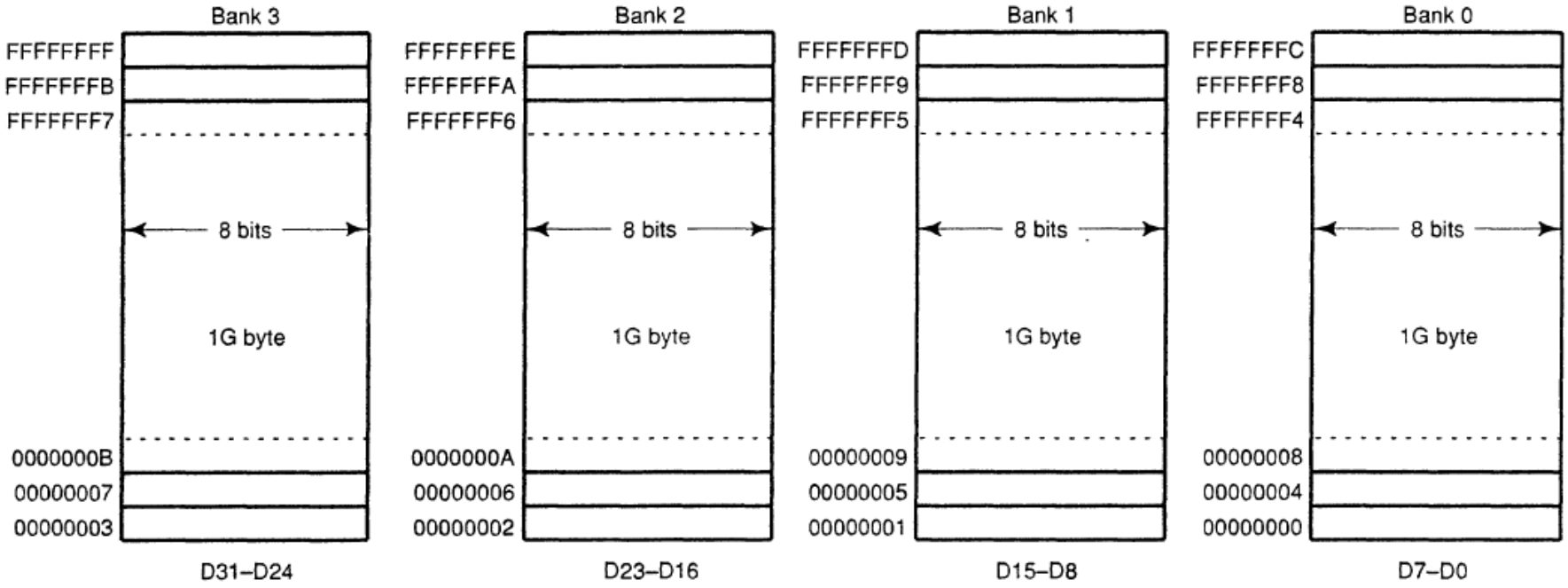
80286 microprocessor
80386SX microprocessor
80386SL microprocessor (memory is 32M bytes)
80386SLC microprocessor (memory is 32M bytes)

Physical memory organization

32 bit memory interface / data bus

- With 32 bit address bus $\Rightarrow$ address space = 2^{32} = 4 GB (0 .. FF FF FF FF)

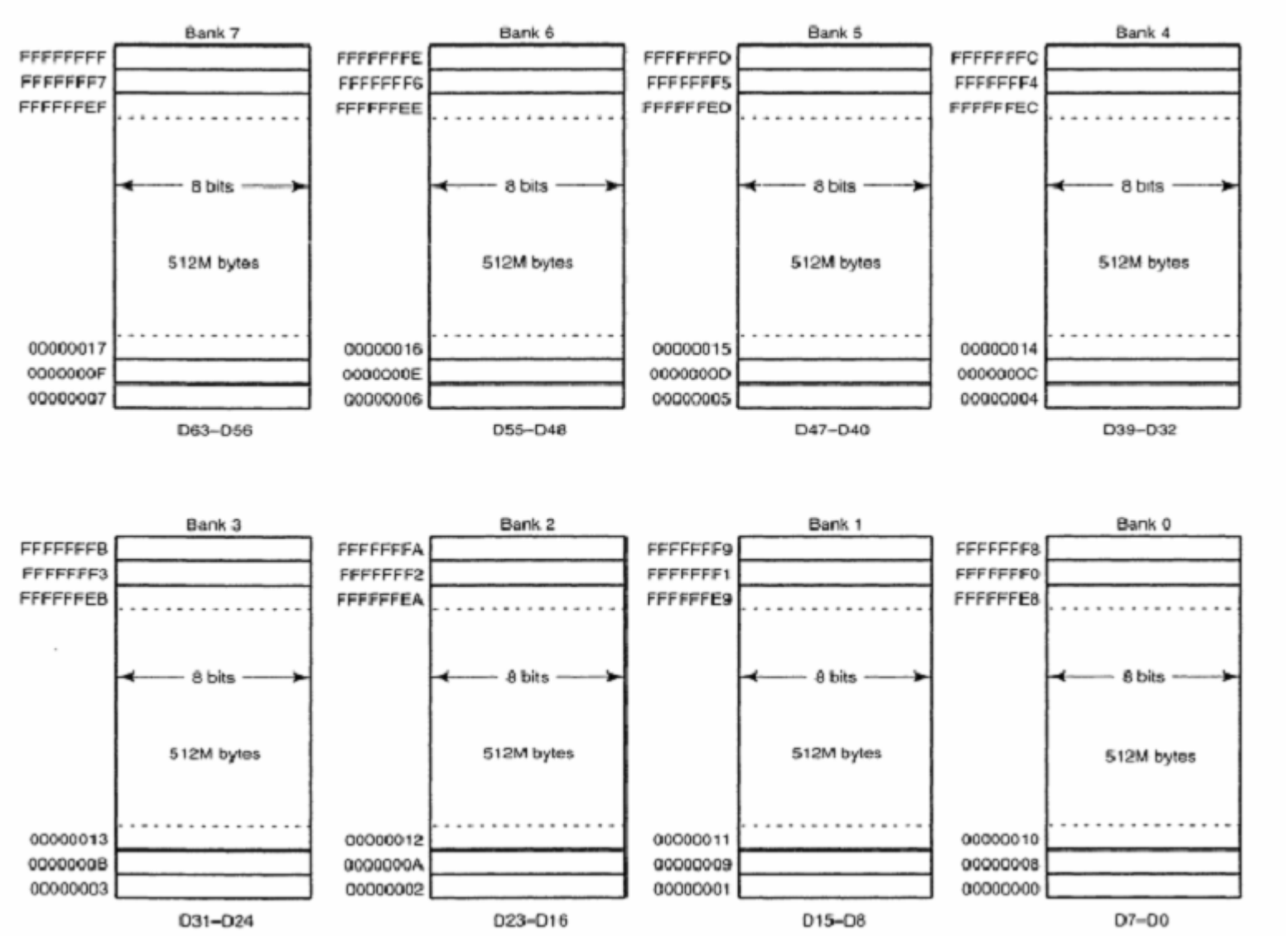
Bank selection signals: $\#BE_{0..3}$



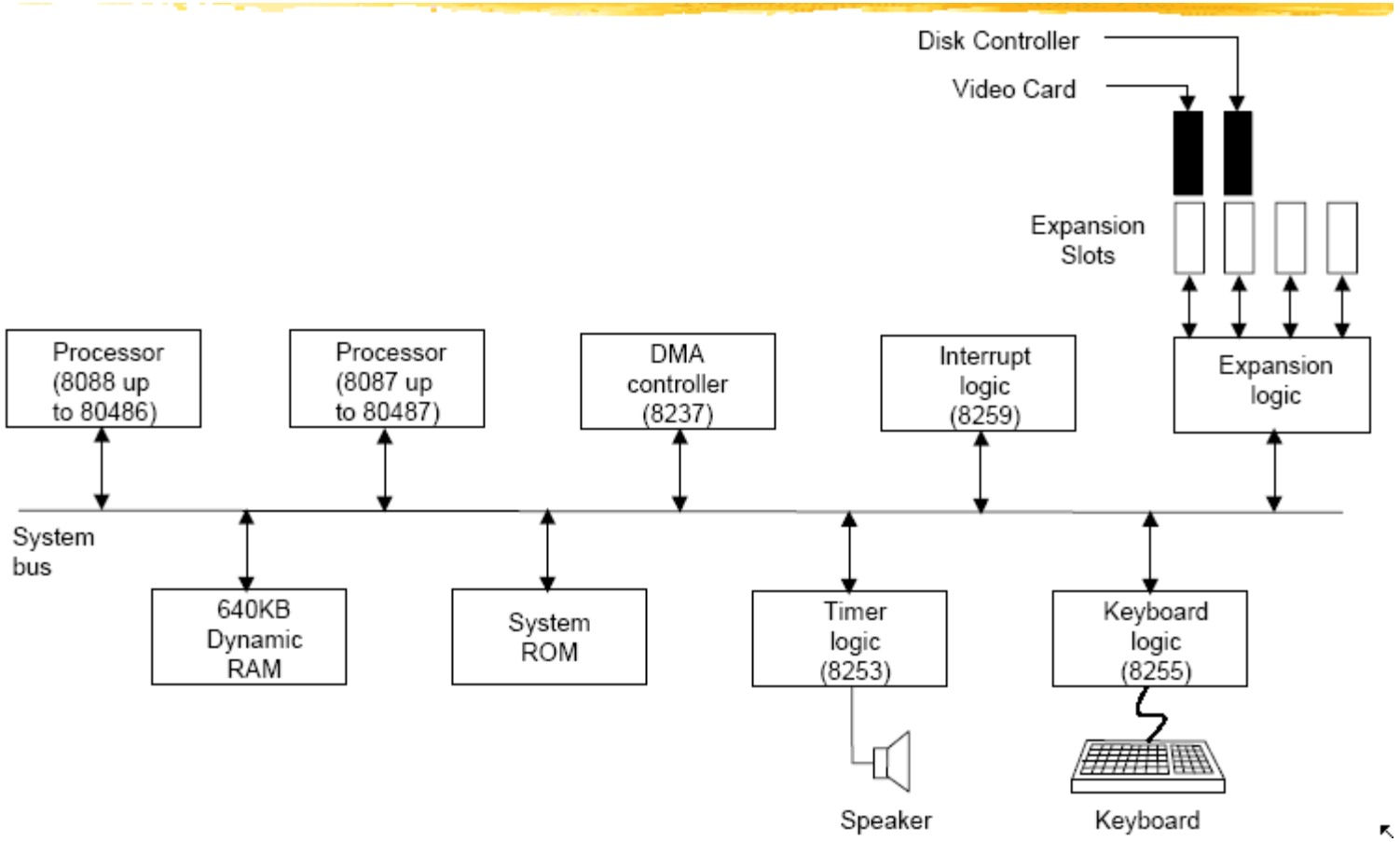
80386DX microprocessor
80486SX microprocessor
80486DX microprocessor

Physical memory organization

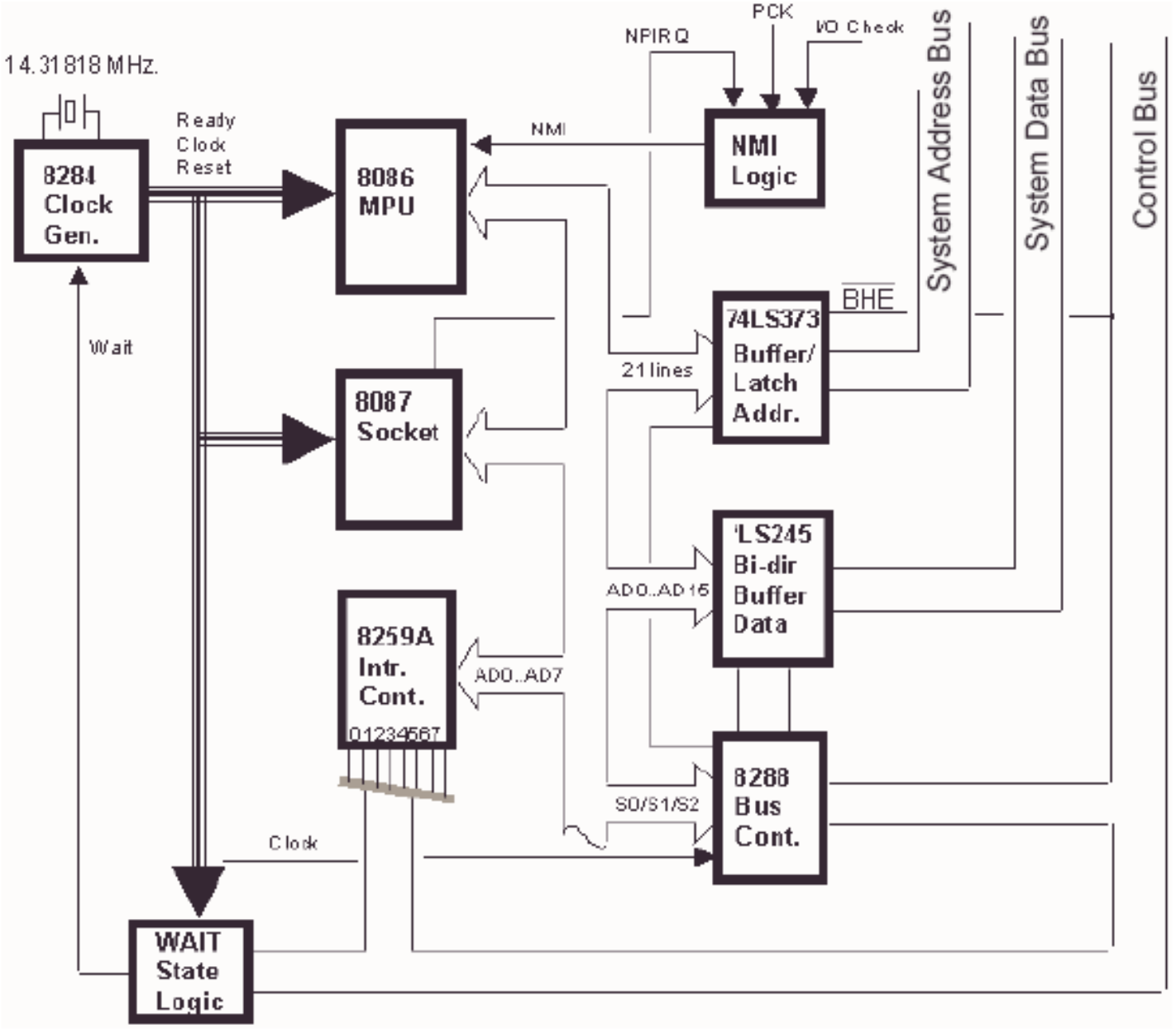
64 bit memory interface: bank selection signals: $\#BE_{0..7}$



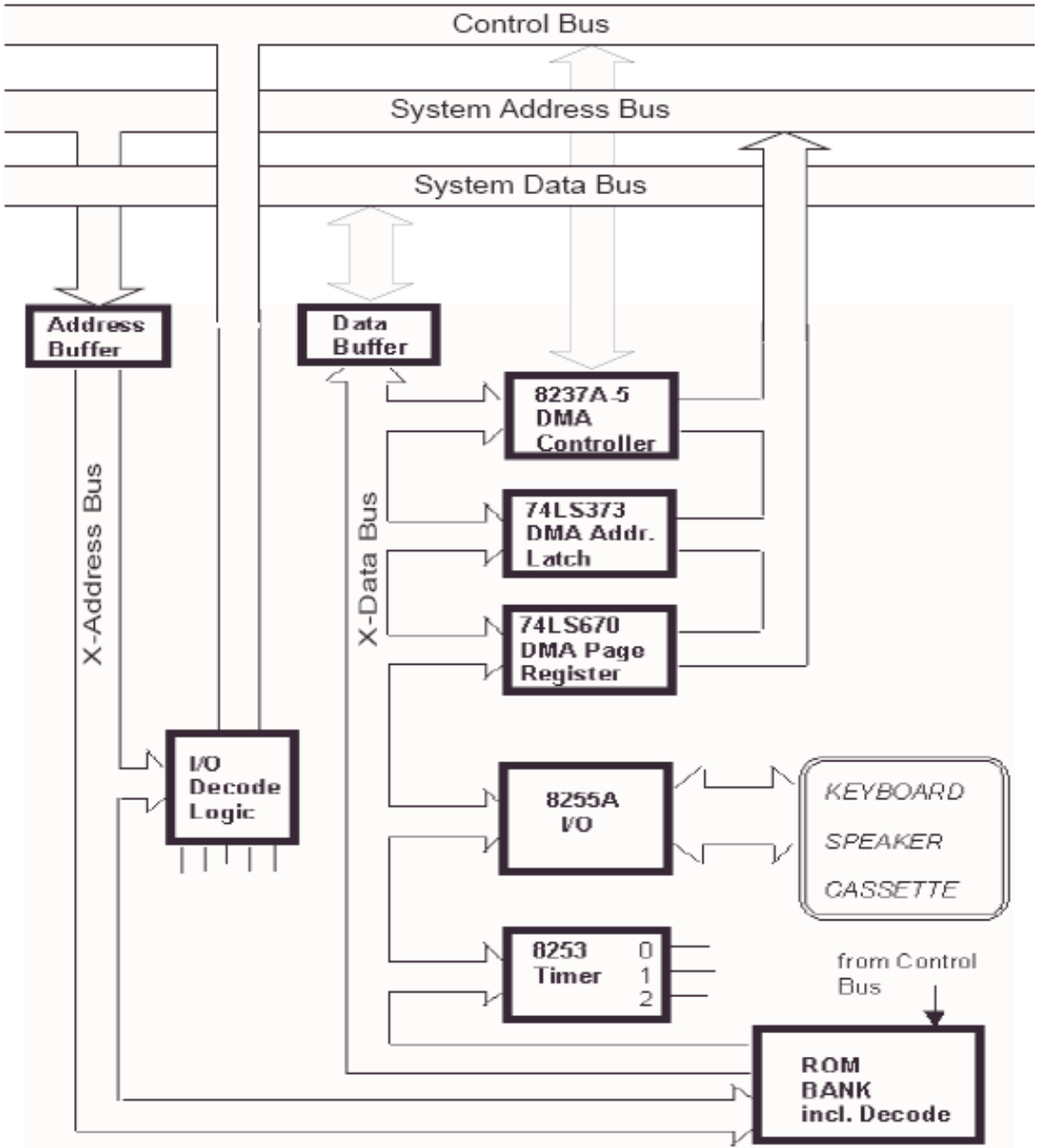
A Typical PC Motherboard



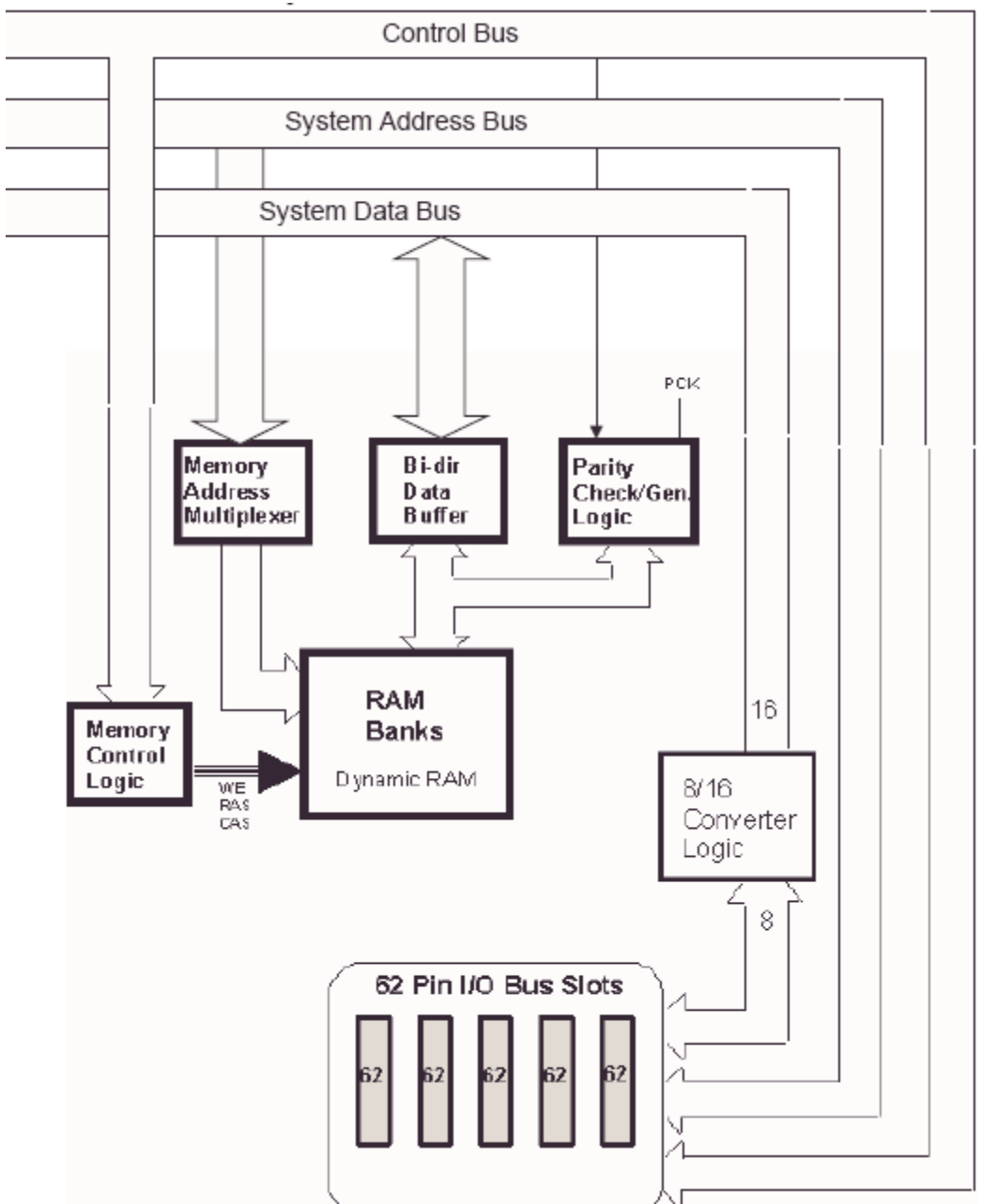
PC XT – Basic components. Bus generation



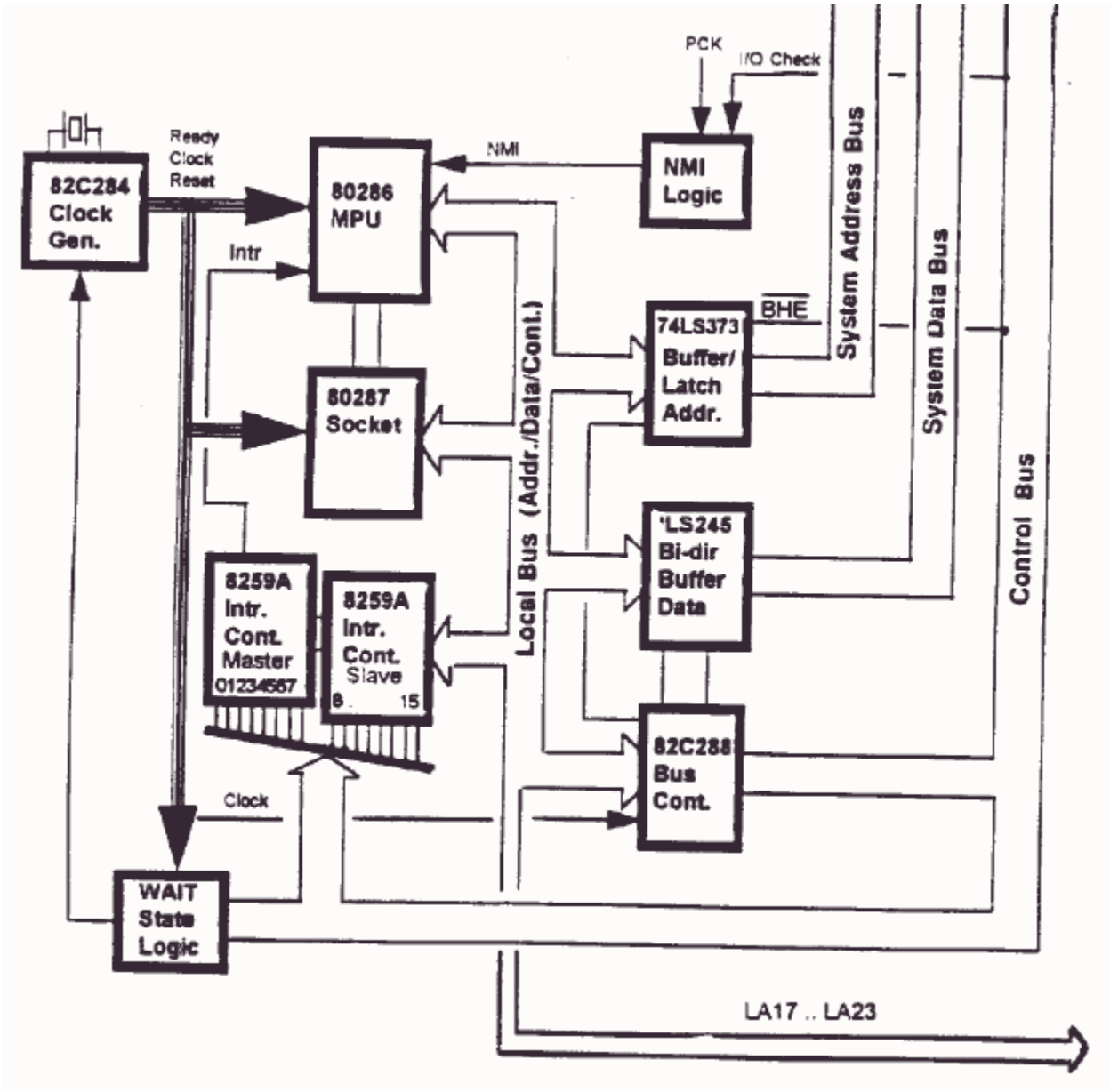
PC XT – DMA extensions, I/O, ROM



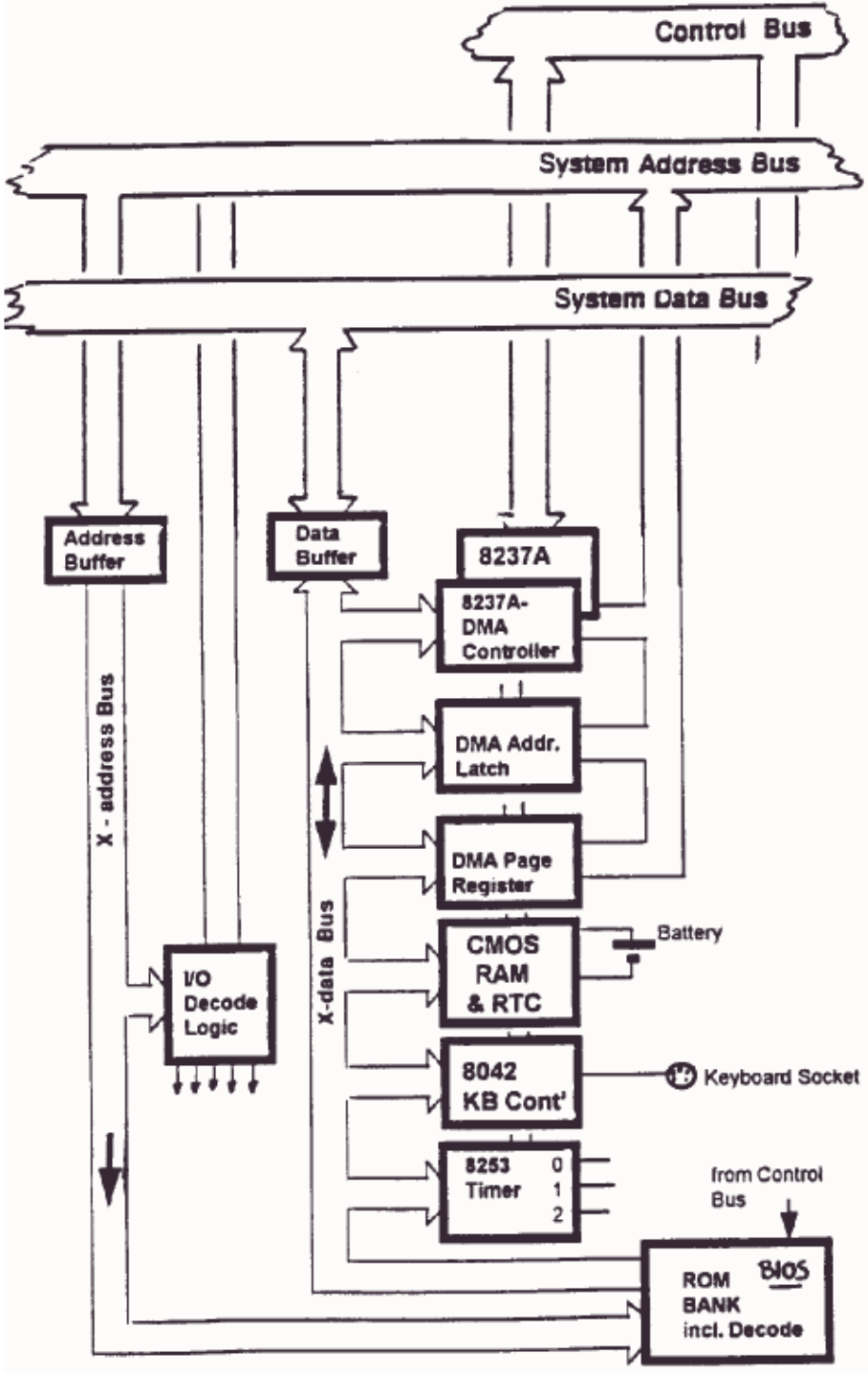
PC XT – RAM, I/O extensions



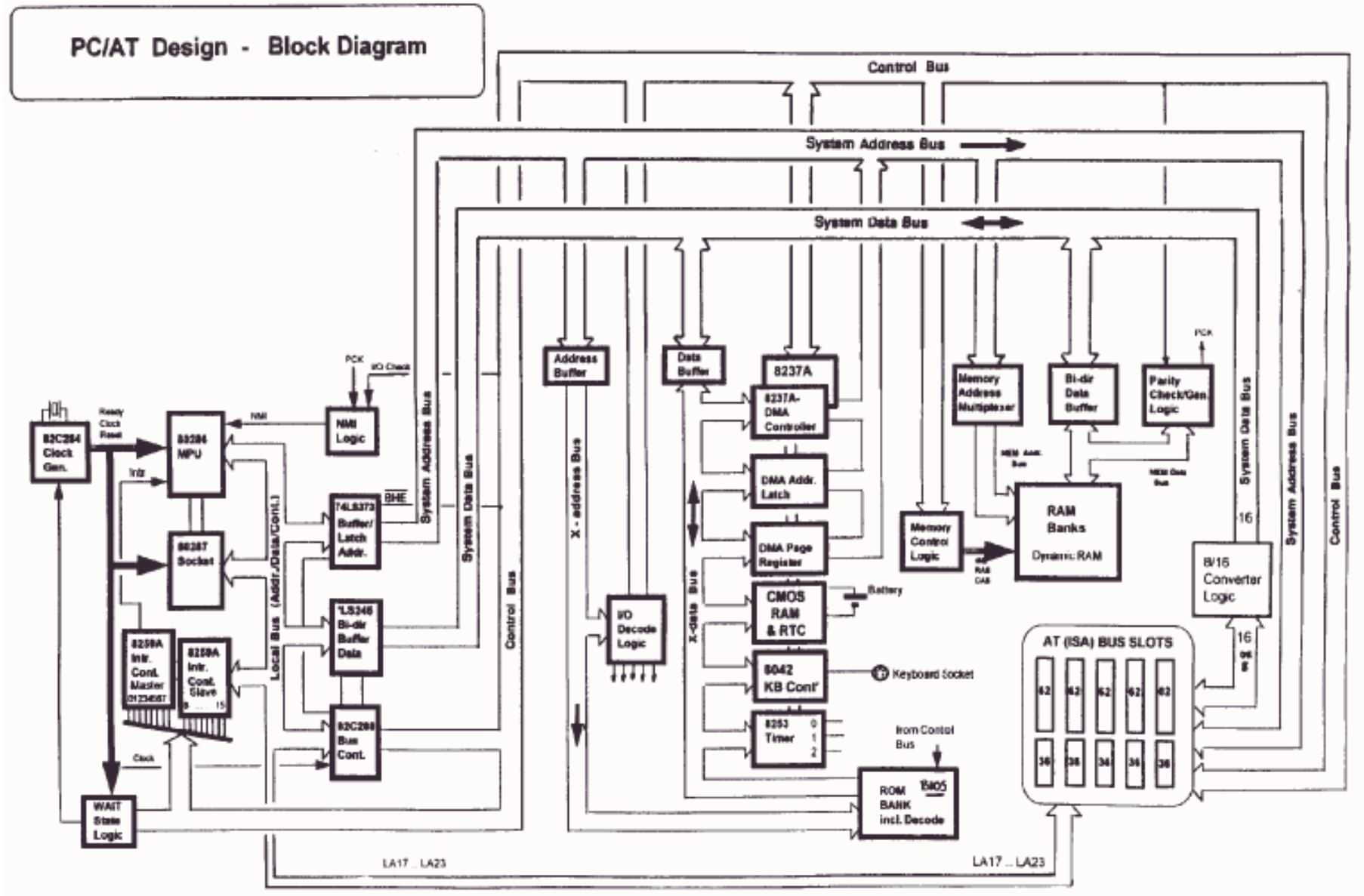
PC AT – Basic components. Bus generation



PC AT - Extensions



PC AT – Block diagram



80x186 family

80186/80188 -HIGH-INTEGRATION 16-BIT MICROPROCESSORS

- Enhanced 8086-2 CPU
- Clock Generator
- 2 Independent DMA Channels
- Programmable Interrupt Controller
- 3 Programmable 16-bit Timers
- Programmable Memory and Peripheral Chip-Select Logic
- Programmable Wait State Generator
- Local Bus Controller
- Completely Object Code Compatible with All Existing 8086, 8088 Software
- 10 New Instruction Types

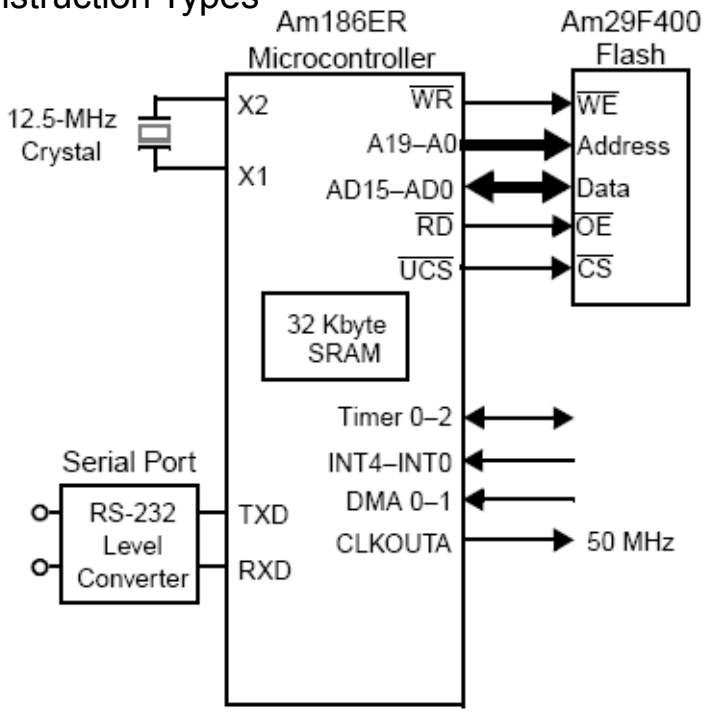


Figure 1. Am186™ER 50-MHz Example System Design

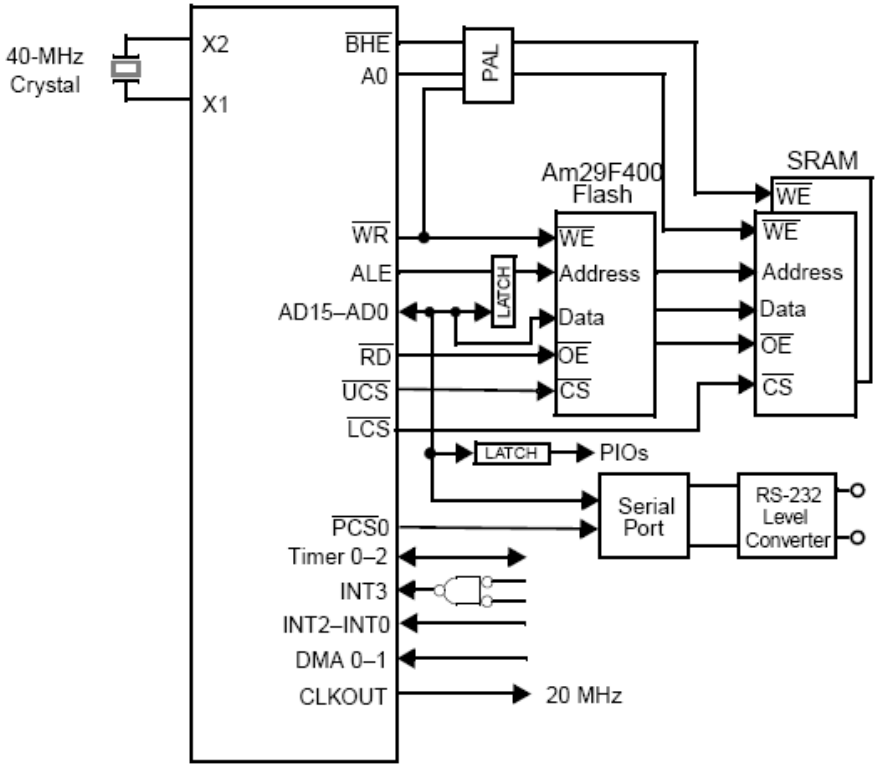


Figure 2. Typical 80C186 System Design

80186 – block diagram