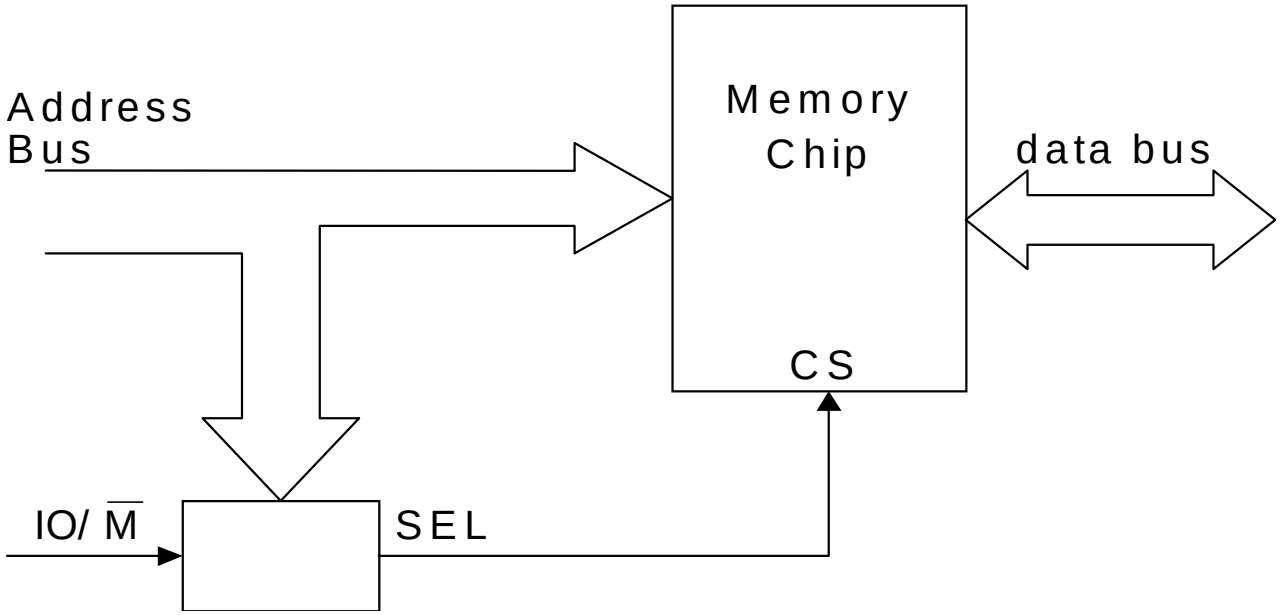
ELE 3230
Microprocessors and Computer Systems

Chapter 8
Memory Address Decoding

(Brey: Ch10-2; Hall: pp185-196)

Memory Address Decoding

- Typically, a system memory is formed by many different memory chips. There are more lines on the address bus than the number of address pins available on a given memory chip. Address decoding is used to monitor all address lines not connected directly to the memory chip's address pins to decide when a particular chip is being addressed.



Memory Address Decoding (Cont.)

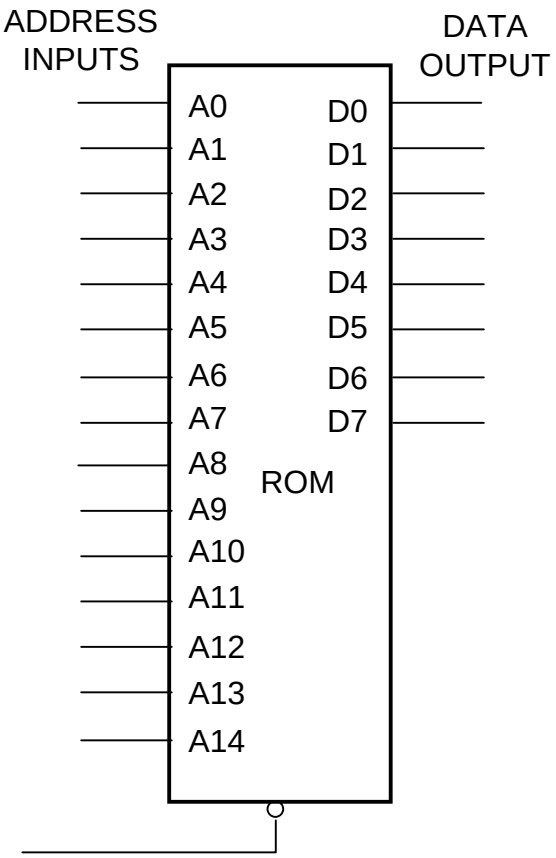
- The address decoder consists of logic gates and takes the address lines not used by the memory chip as input.

- Example: Suppose the memory chip has 11 address pins (the memory has 2^{11}=2K addresses) and the address bus has 20 address lines (2^{20}=1M address space). If we want to map the chip to a 2K block at the top of memory (FF800h to FFFFFh) then the decoder must generate a CS signal only when the address lines contains 1111 1111 1xxx xxxx xxxx.

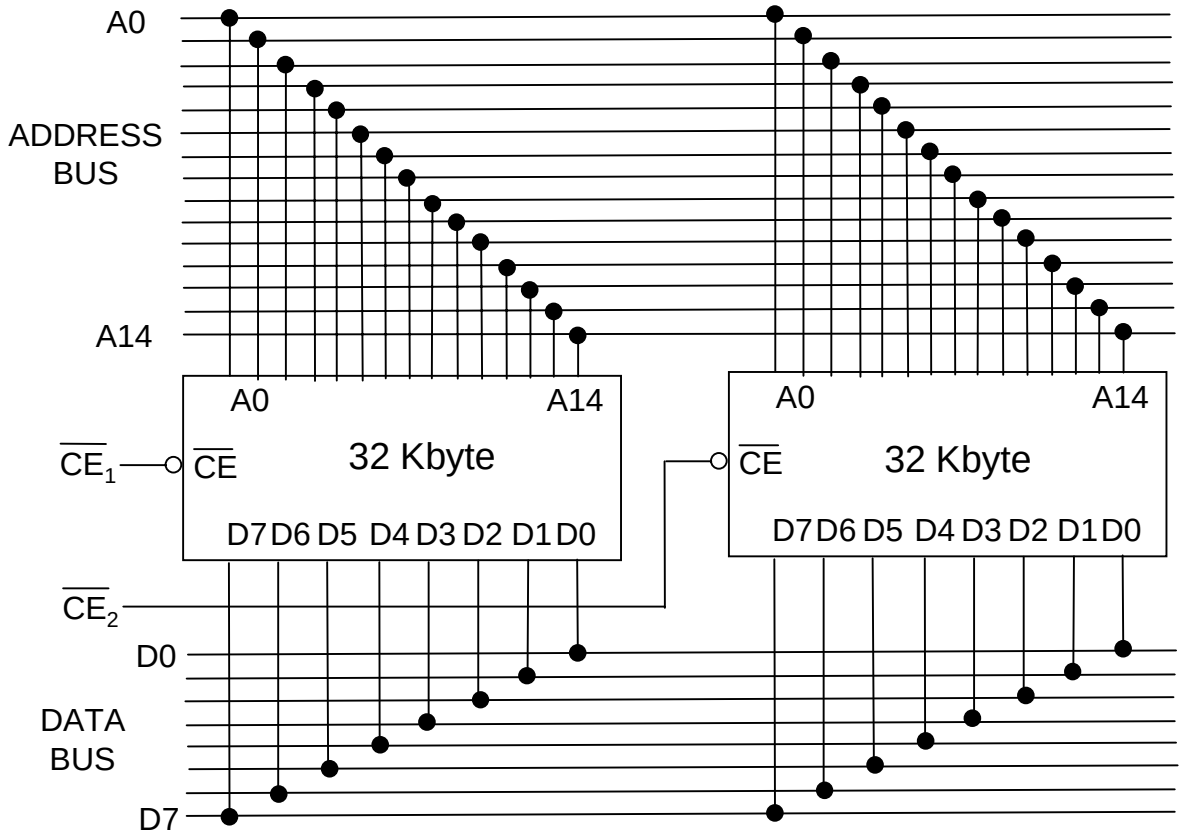
  x: don't care

- A 9-input AND gate connected to the 9 most significant address lines will perform the decoding function in this simple example.

ROMS

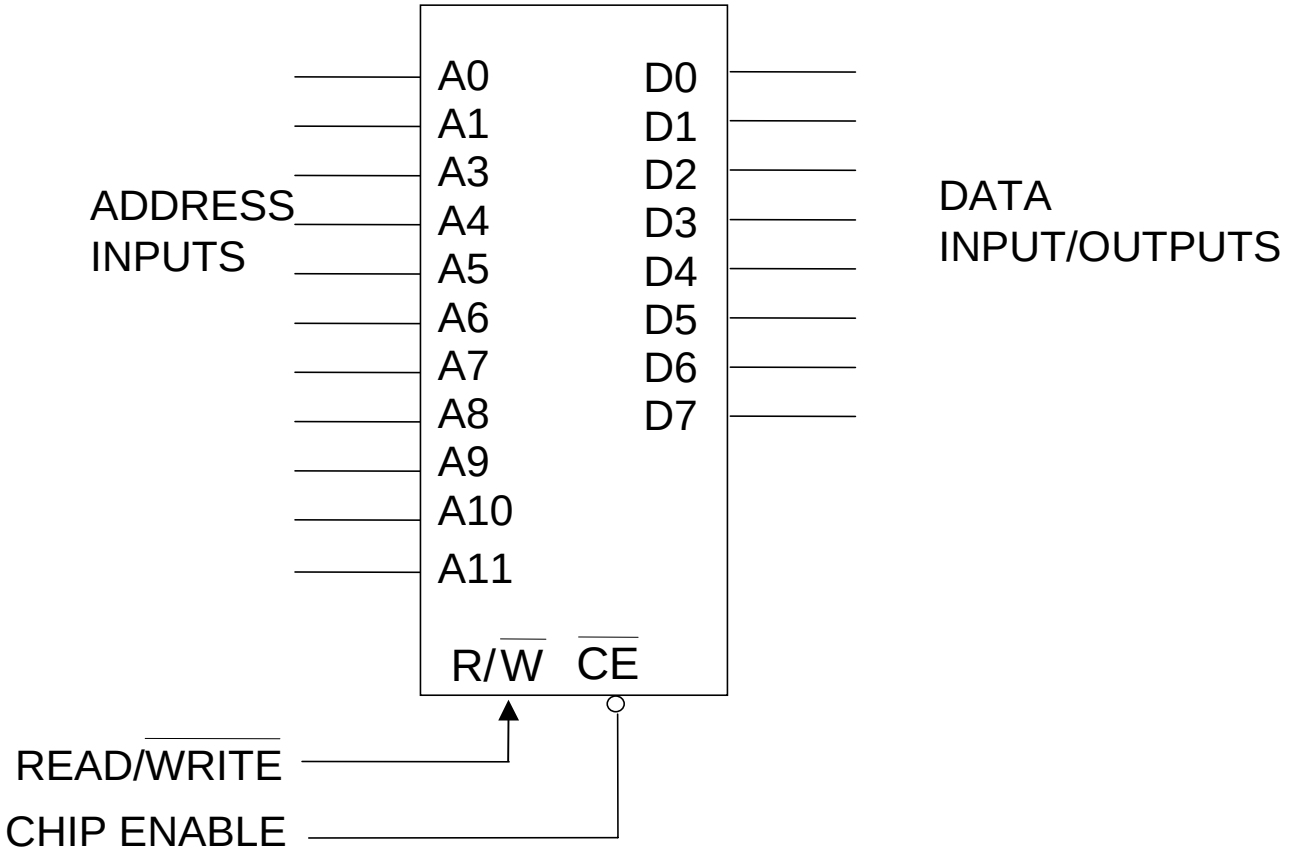


Schematic symbol



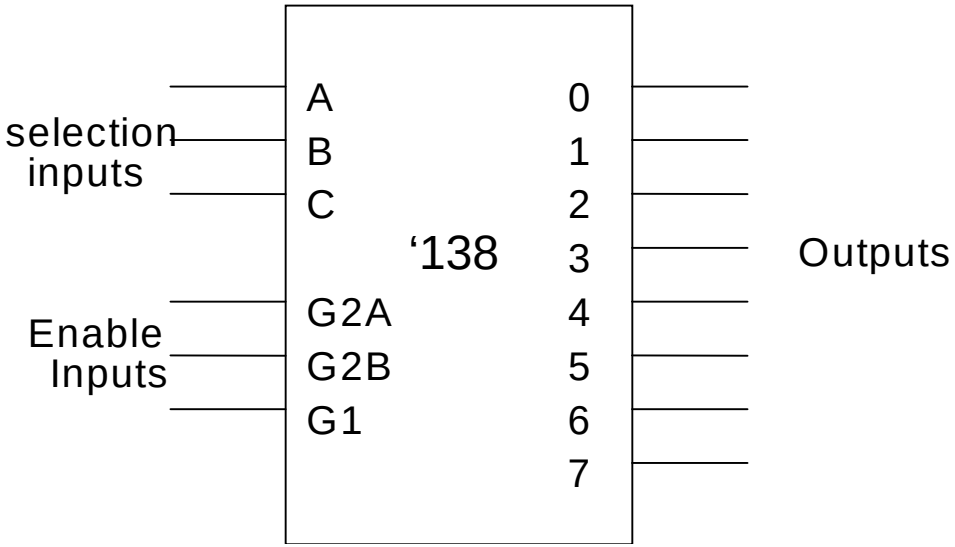
Connection in parallel

RAM Schematic Symbol



Memory Address Decoders

- In practice, combinational logic gates (e.g. the AND gate in the previous example) are rarely used for memory decoding since a different set of logic gates would be needed to generate the CS signal for each memory chip. Integrated circuit address decoders e.g. 74LS138 are normally used.



Memory Address Decoders (cont.)

- 74LS138 can be used to decode 3 address lines to enable up to 8 memory chips (each of its output may be used to enable a different chip).
- All 8 outputs are not asserted when any of the enable inputs (G1, G2A, and G2B) are not asserted.
- Only one output is asserted when all three enable inputs are asserted, and the output asserted depends on the A,B,C selection input (one output for each possible combination).
- Sometimes an external logic gate may be used in conjunction with the 74LS138 to perform decoding using more than 3 address lines.

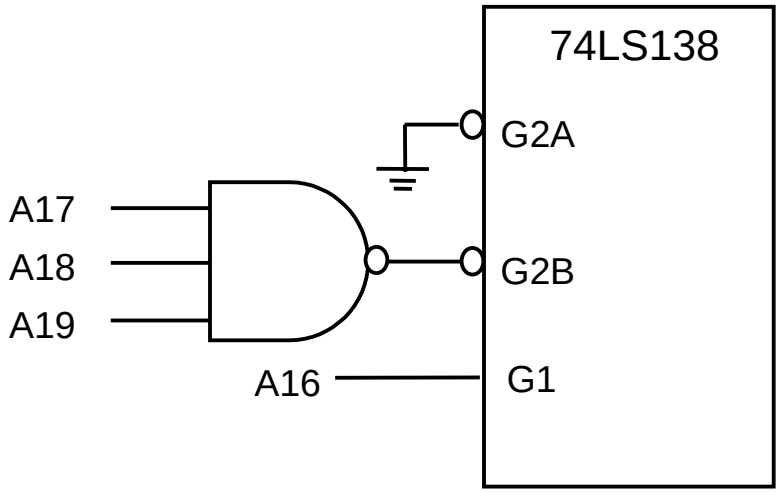
Using the 74LS138 Decoder

- Task: Design a circuit to map eight different 2764 EPROM chips (each EPROM is organized as 8K x 8 bits) to a 64K-byte block of memory with a physical address in the range F0000h to FFFFFh. (Note: each address holds 1 byte=8 bit of data)
- Solution: Each 2764 EPROM may be mapped directly to an 8K-byte block.

1st block:	F0000 - F1FFFh
2nd block:	F2000 - F3FFFh
3rd block:	F4000 - F5FFFh
4th block:	F6000 - F7FFFh
5th block:	F8000 - F9FFFh
6th block:	FA000 - FBFFFh
7th block:	FC000 - FDFFFh
8th block:	FE000 - FFFFFh

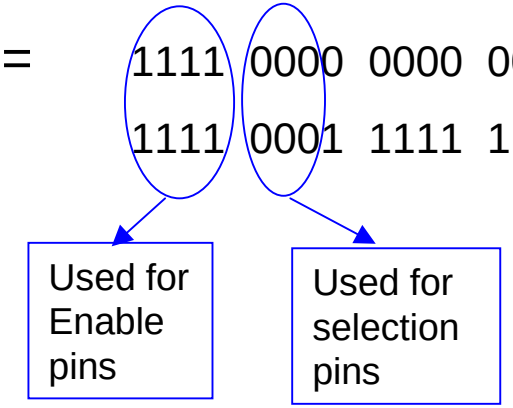
Using the 74LS138 Decoder (cont.)

- It is helpful to write these numbers in binary to see (1) which address lines are common to all chips and (2) which are common to all address in one chip, so they can be used to generate chip enable and chip selection.
- The most significant hexadecimal digit must be F (in this example) to address the 8 EPROMS. Hence address lines A16-A19 may be used to enable the ‘138 decoder (so that CE signals are only generated if A16-A19 are all asserted):



Address Decoding Example (Cont.)

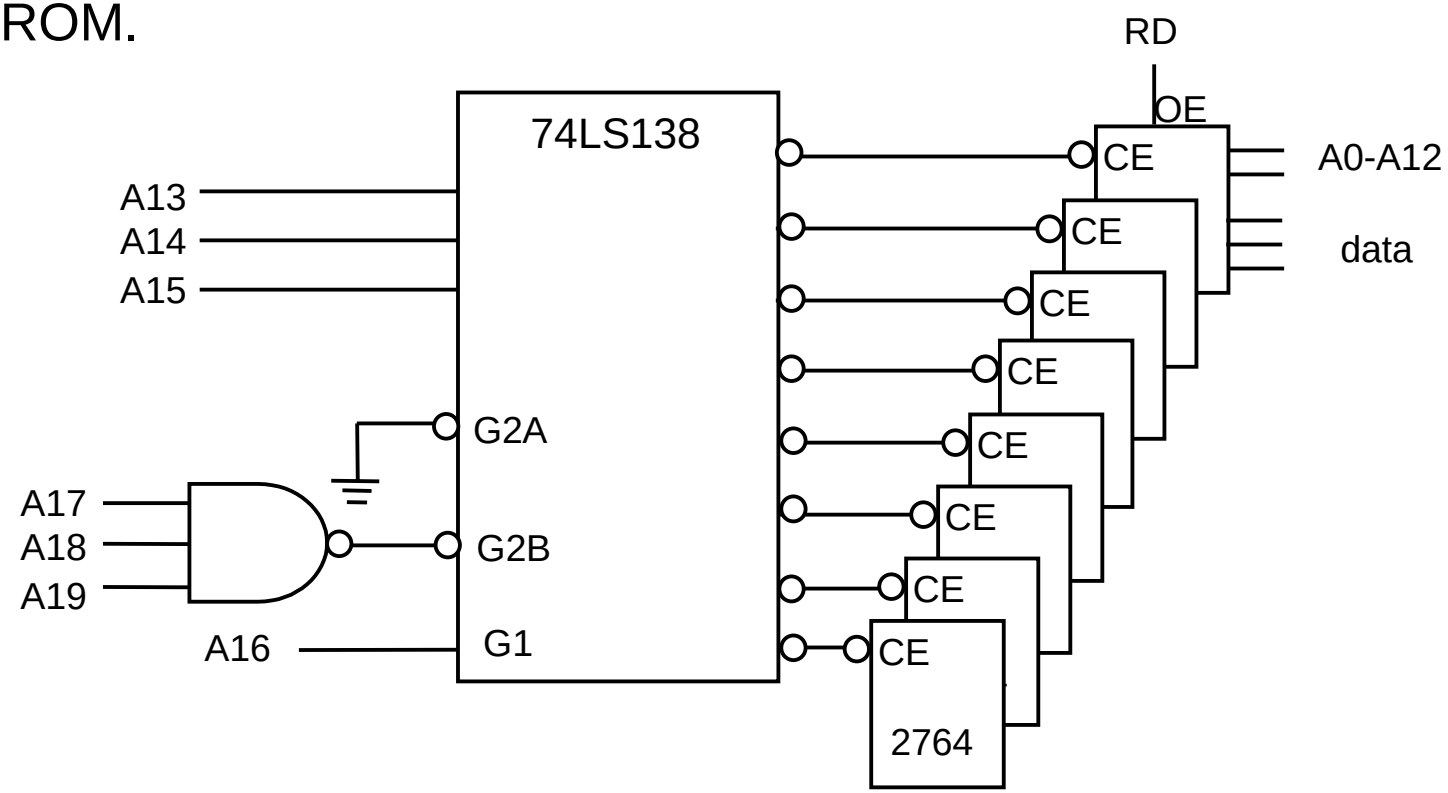
1st block:	F0000 - F1FFFh	=	1111 0000 0000 0000 0000 - 1111 0001 1111 1111 1111
2nd block:	F2000 - F3FFFh		
3rd block:	F4000 - F5FFFh		
4th block:	F6000 - F7FFFh		
5th block:	F8000 - F9FFFh		
6th block:	FA000 - FBFFFh		
7th block:	FC000 - FDFFFh		
8th block:	FE000 - FFFFFh		



- Notice pattern of bits: In each 8K block, the 2nd most significant set of 4 address lines have three lines (i.e. A13-A15) which have the same values for each block but different to other blocks. We can therefore use A13-A15 to generate the individual chip selection signals of the 8 EPROMs.

Address Decoding Example (cont.)

- The address pins of each EPROM must be connected to the 13 address least significant lines in order to address the 2^{13} (=8K) bytes in each EPROM.



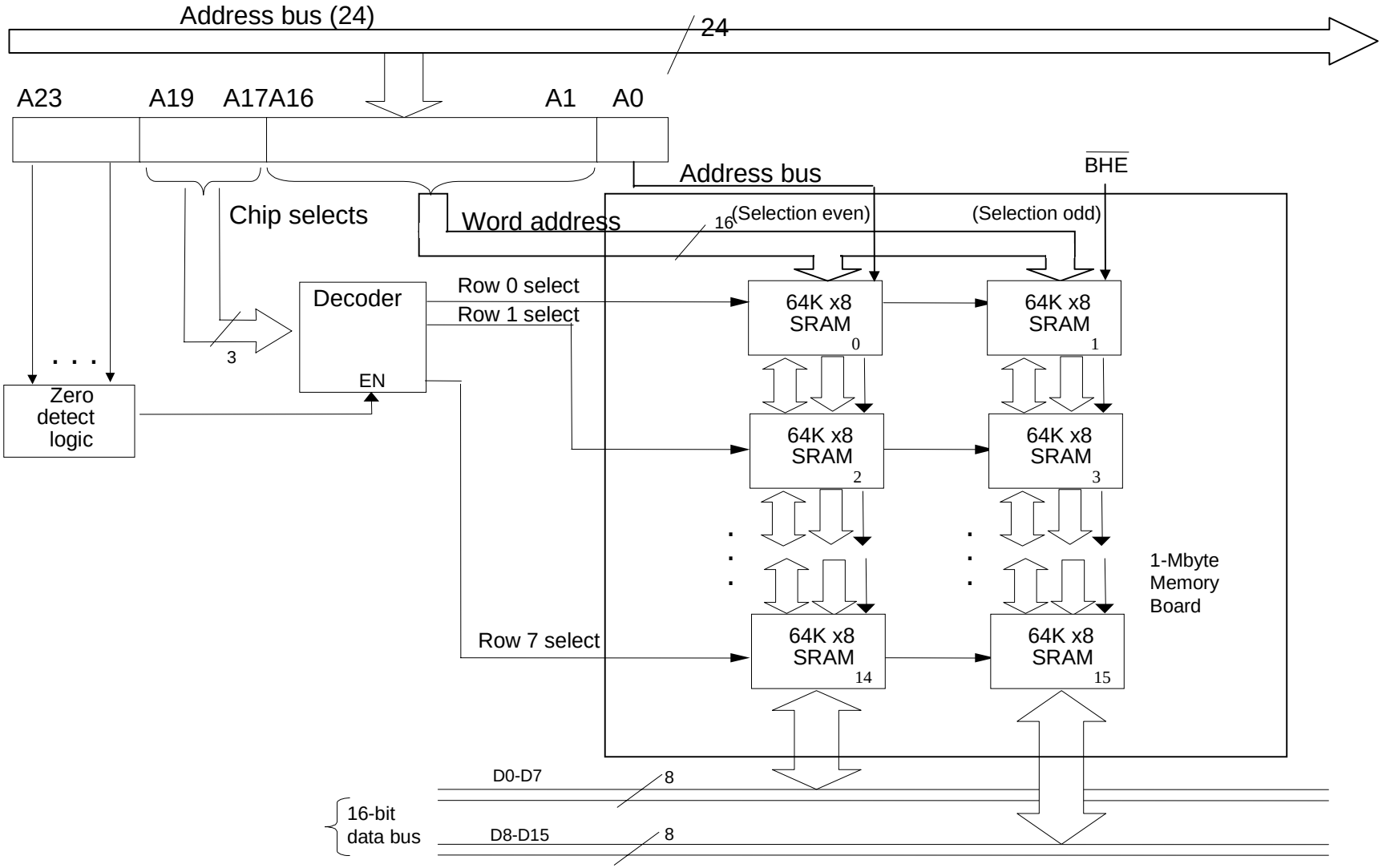
Q: What are the other possibilities to implement the input for the enable pins?

Example (2) of Address Decoding

- Task: Design the memory subsystem for a 16-bit microprocessor which has a 24-bit address. The system should use 64K x 8 bit SRAMS which have a single CS input and the total capacity should be 1MByte assigned to the lowest physical addresses. Show the connections to the address and data buses.

- Solution: Since the total memory is 1MByte, a total of 16 SRAM chips, each of 64kbyte capacity, will be needed. As the data bus is 16-bits wide, the 8-bit SRAMs must be arranged in pairs. One possible solution is:

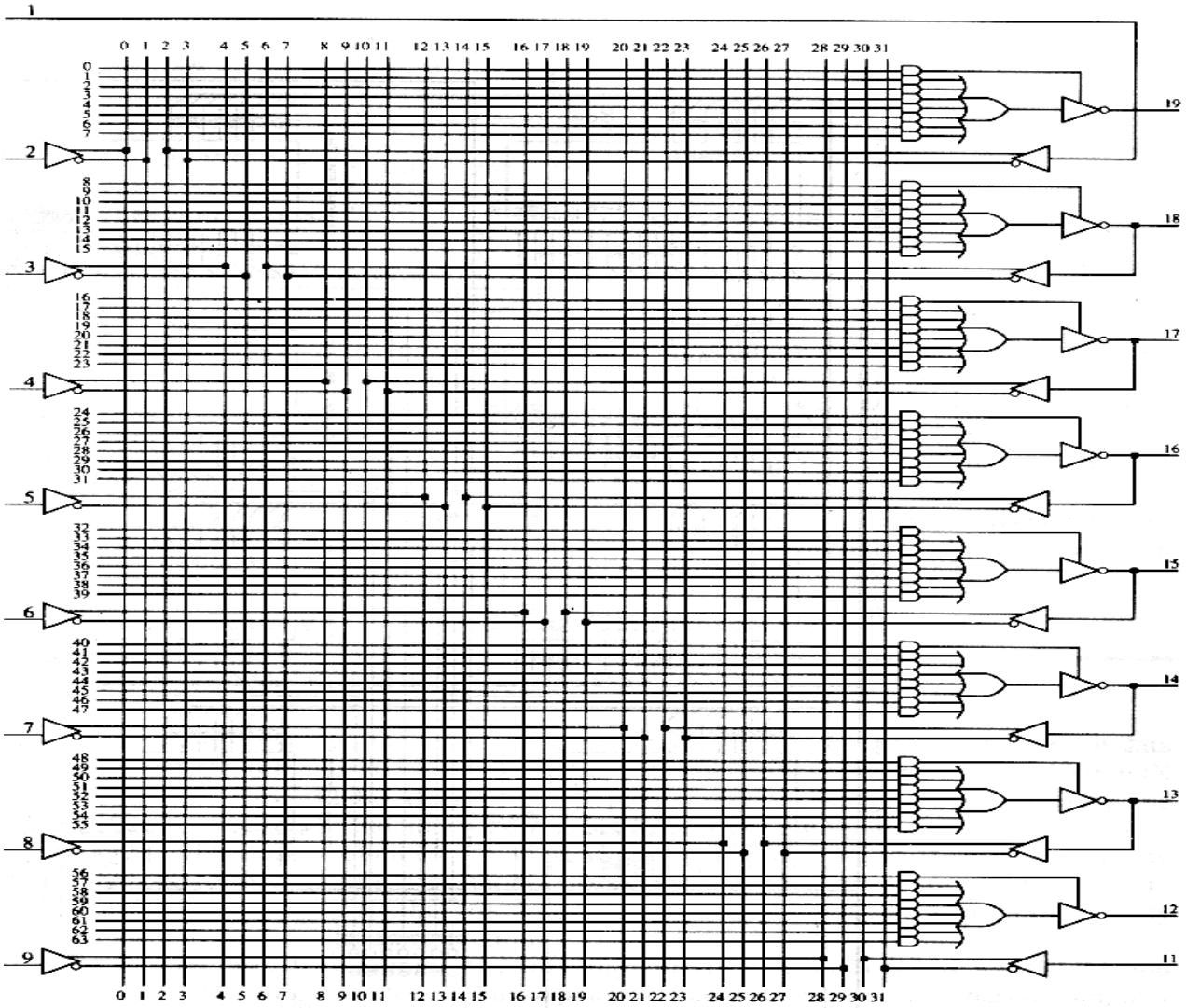
Example (2) of Address Decoding (Cont.)



Other Address Decoders

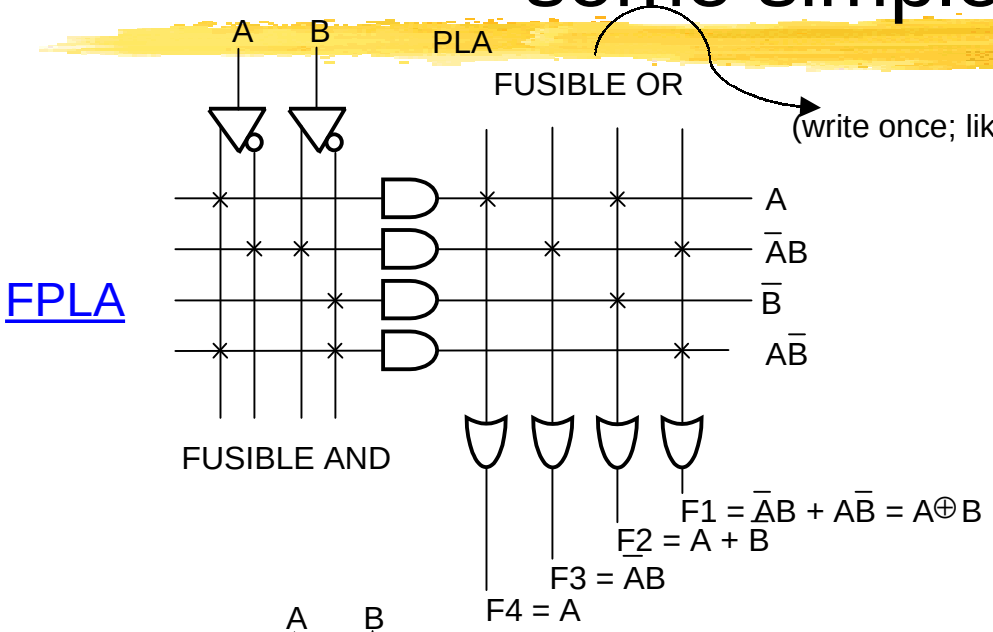
- The 74LS139 is a two-to-four line decoder (i.e. 2 inputs, 4 outputs) that is sometimes used for address decoding.
- PROMS and EPROMS can be used as decoders eg. A 82S147 (512x8). PROM can be used to completely replace the 74LS138 and NAND gate in the previous example provided it has been programmed with the correct bit pattern to select the 8 chips.
- Programmable Logic Devices (PLA - programmable logic array, PAL - programmable array logic, and GAL - gated array logic) may also be used as address decoders. Eg. AMD 16L8 PAL:

Other Address Decoders (Cont.)

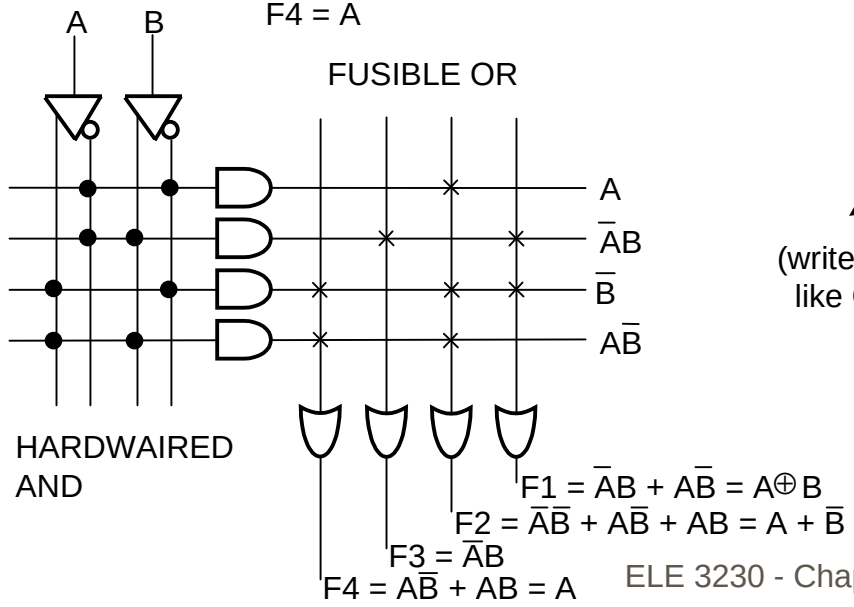


PAL16L8

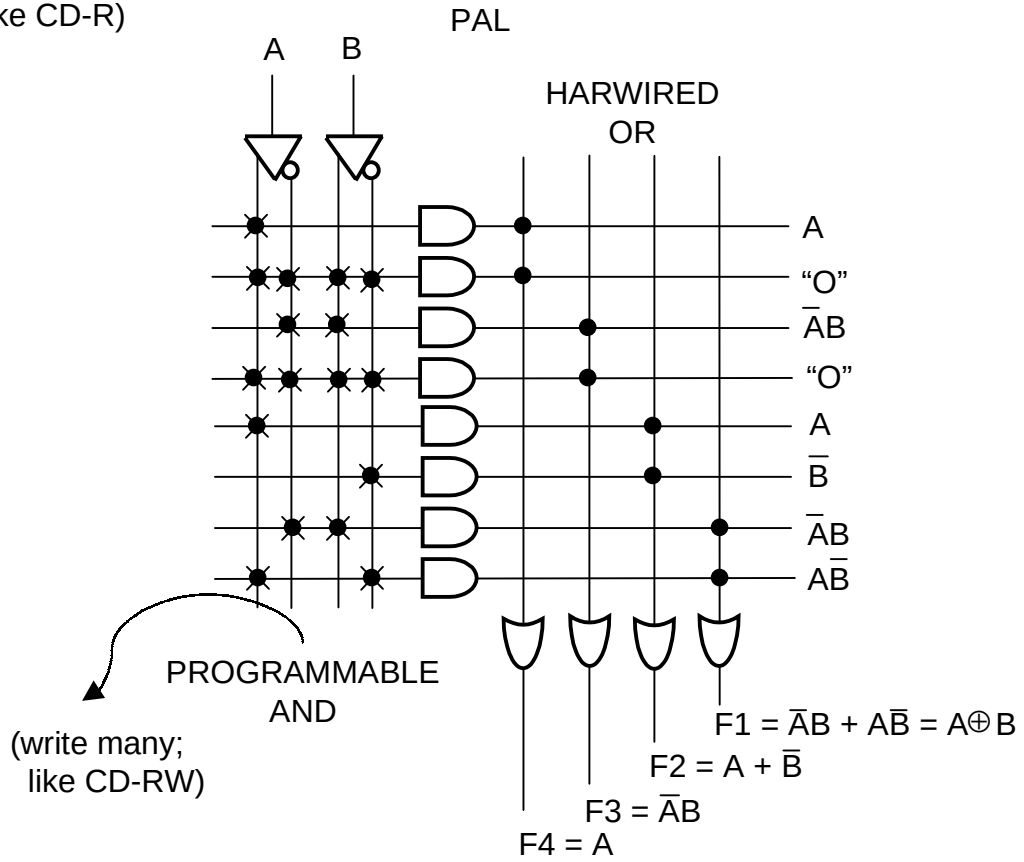
FPLA, PROM, and PAL programmed to implement some simple logic functions



FPLA



PROM



PAL