Design with Microprocessors

Year III Computer Sci. English

1-st Semester

Lecture 13: I/O interfaces (2)

Simple I/O ports. Parallel Interfaces.

I/O Example

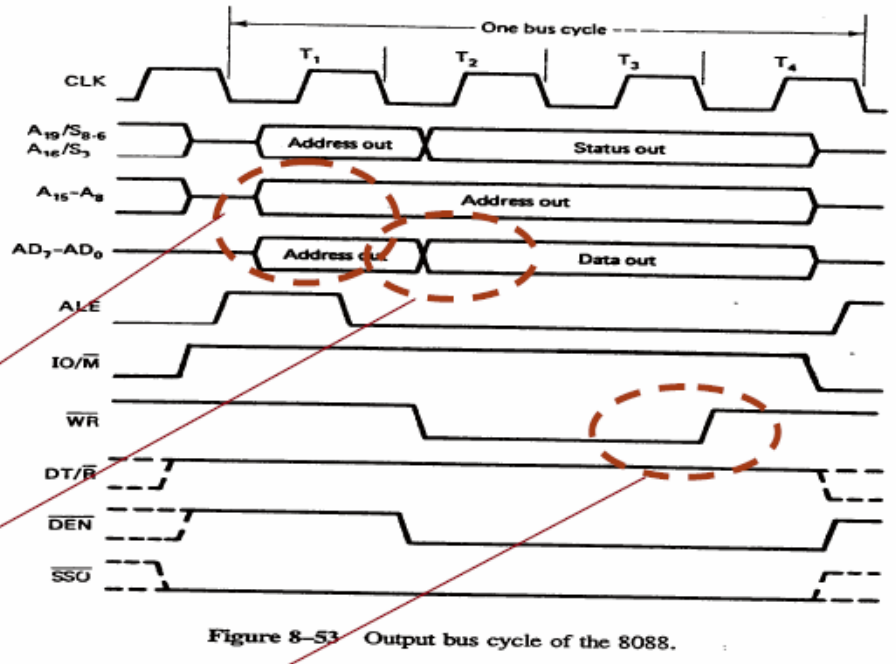


Figure 8–53 Output bus cycle of the 8088.

- Assume that AX = 76A9h.: Analyze the data transfer for a) 8088 b) 8086 when

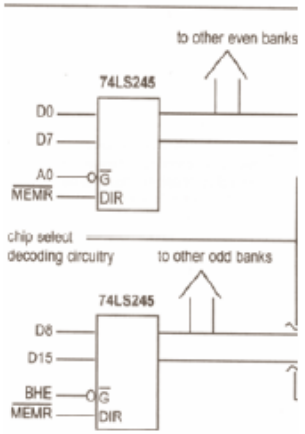
  MOV DX, 648h

  OUT DX,AX

- 8088 case
  - 1st bus cycle
    - T1: Address 0648h is put on pins AD0-AD7, A8-15 and latched when ALE is activated
    - T2: The low byte A9h is put on the data bus pins AD0-AD7 and $\overline{\text{IOWC}}$ is activated
    - T3: Setup time
    - T4: Byte is written to the port assuming zero wait states
  - 2nd Bus Cycle (Similar to 1st Bus Cycle)
    - T1: Address 0649h is put on pins AD0-AD7, A8-15 and latched when ALE is activated
    - T2: The high byte 76h is put on the data bus pins and $\overline{\text{IOWC}}$ is activated
    - T3: Setup time
    - T4: Byte is written to the port assuming zero wait states

Example continued

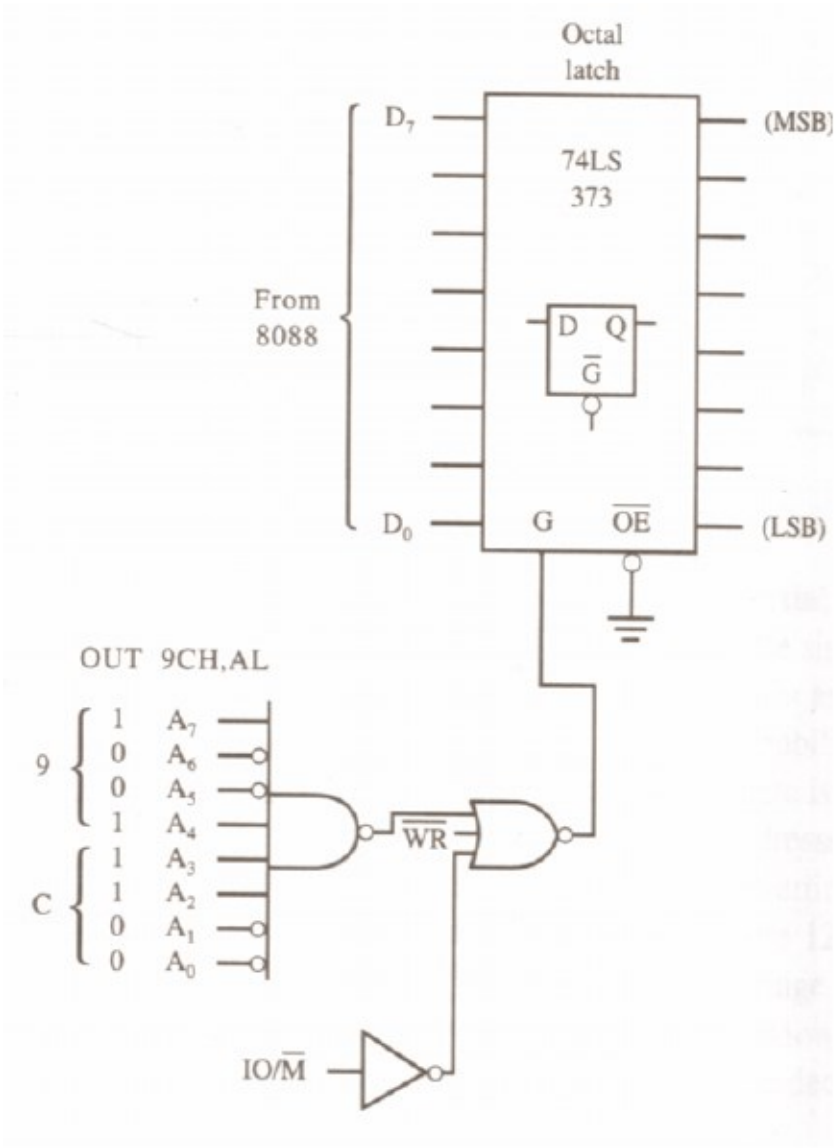
- 8086 case
  - T1: Address 0648h is put on pins AD0-AD15 plus BHE=low is latched by the 74LS373 when ALE is activated
  - T2: 76A9h, the contents of AX, is put on AD0-AD15 (A9h on AD0-AD7, 76h on AD8-AD15) and IOWC is activated
  - T3: Setup time
  - T4: During this interval, with the help of the signals A0=0 and BHE=0, the low and high bytes are written to the appropriate ports.
    - ➢It must be noted that since the operand is a 16 bit word and the port address is an even address, the 8086 CPU does not generate address 0649h
    - ➢Port address 648h is connected to the D0-D7 data bus and port address 649h is connected to the D8-D15 data bus



I/O Design in the 8088/86

- In every computer, when data is sent out by the CPU, the data on the data bus must be latched by the receiving device
- While memories have an internal latch to grab the data on the data bus, a latching system must be designed for ports
- Since the data provided by the CPU to the port is on the system data bus for a limited amount of time (50 - 1000ns) it must be latched before it is lost
- Likewise, when data is coming in by way of a data bus (either from port or memory) it must come in through a three-state buffer

Example: Using the 74LS373 in an output port design



The steps for the "OUT 9CH,AL" instruction are as follows:

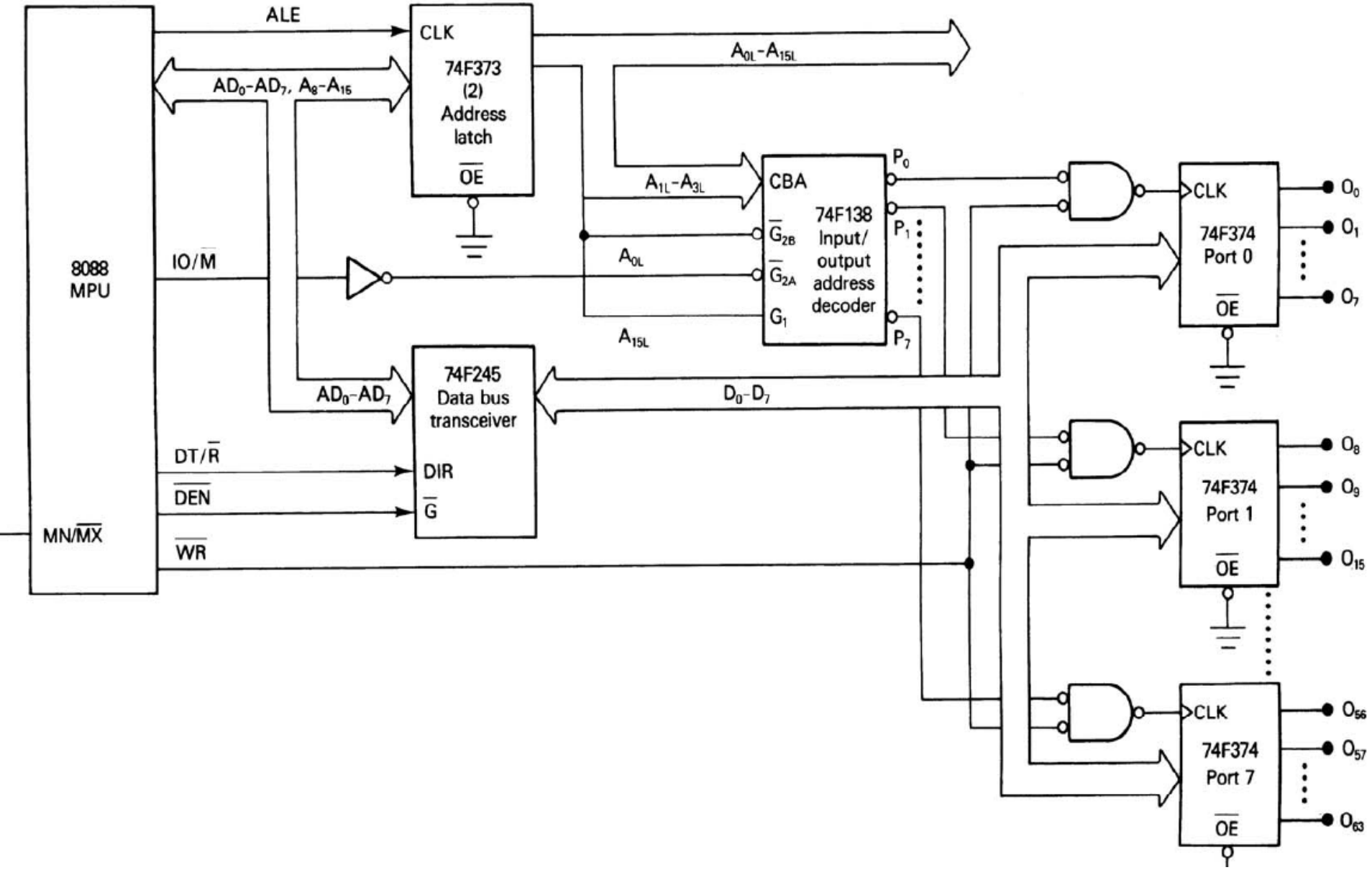
T1, address 9CH is provided to address bus A0-A7 through AD0-AD7 and the ALE signal.

T2, IOWC is provided and the contents of AL are released into the data bus pins AD0-AD7.

T3 is given for the signals to travel to the destination port.

during T4 the contents of D0-7 are latched into this 74LS373, with IOWC going from low to high.

Example - 64 line parallel output circuit - 8088



Time Delay Loop and Blinking a LED at an Output

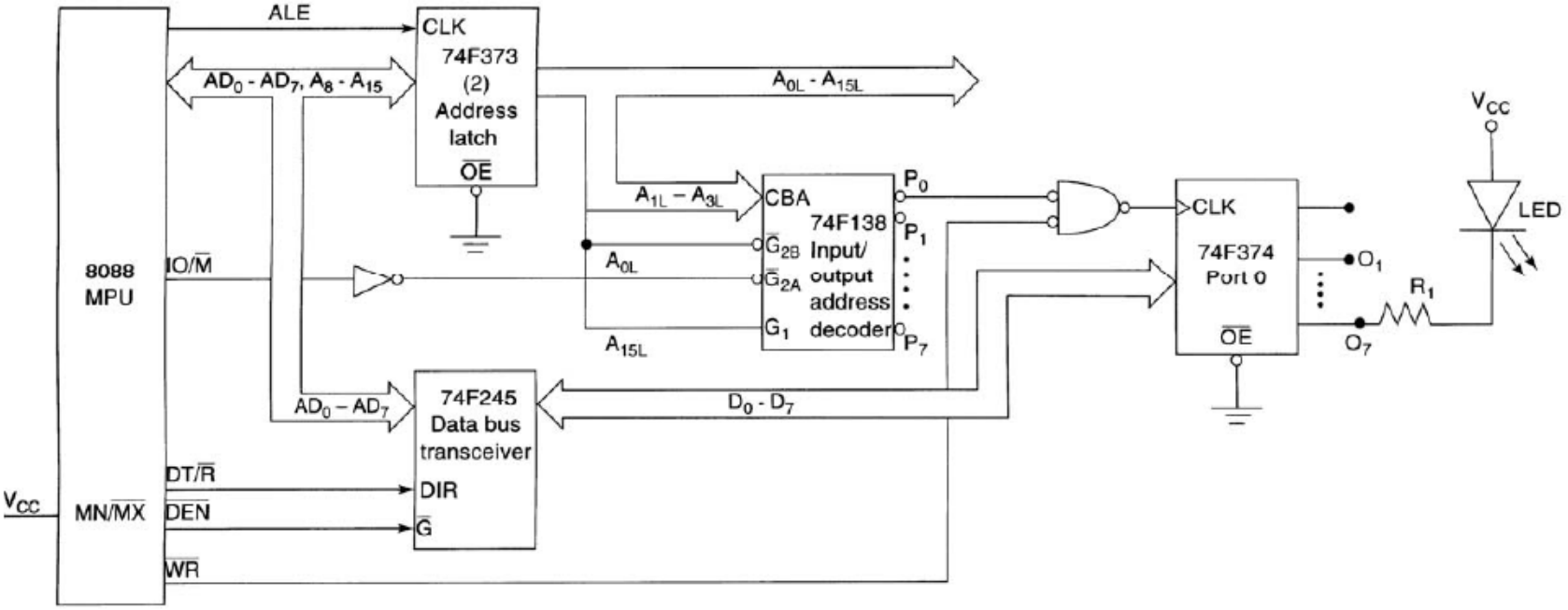


Figure 10–2 Driving an LED connected to an output port.

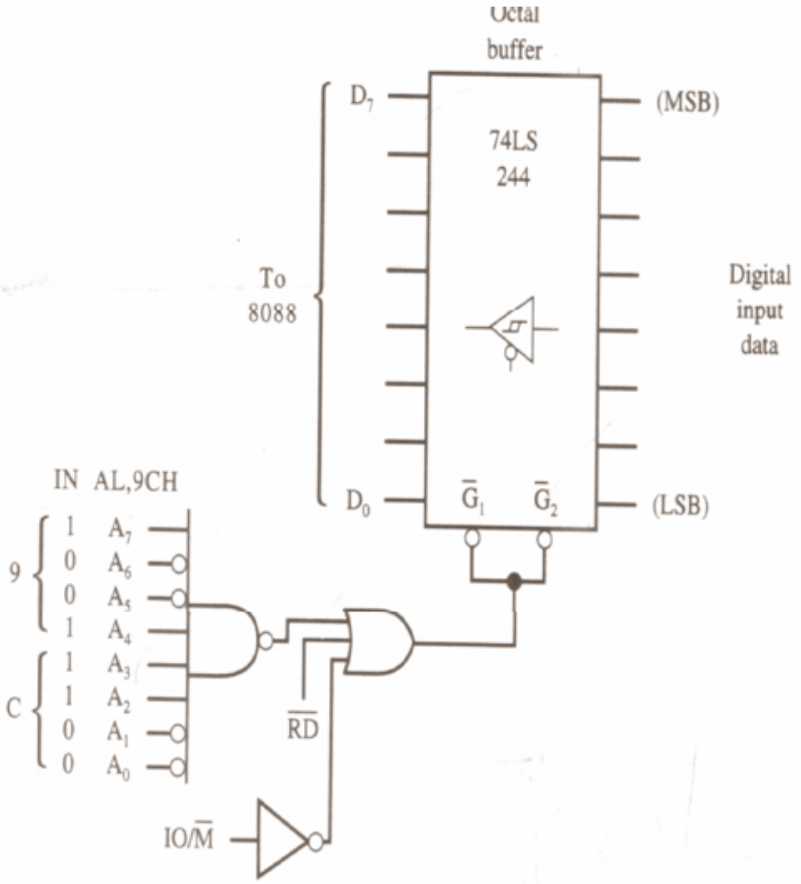
```
        MOV DX, 8000h     ;initialize address of port 0
        MOV AL, 00h       ; load data with bit 7 as logic 0
ON_OFF: OUT DX,AL         ; turned on
        MOV CX,0FFFFh     ; load delay count of FFFFh
HERE:   LOOP HERE ------------------------------------------>
        XOR  AL,80h       ; complement bit 7
        JMP  ON_OFF
```

Aprox.

17 T states * 64K * Frequency

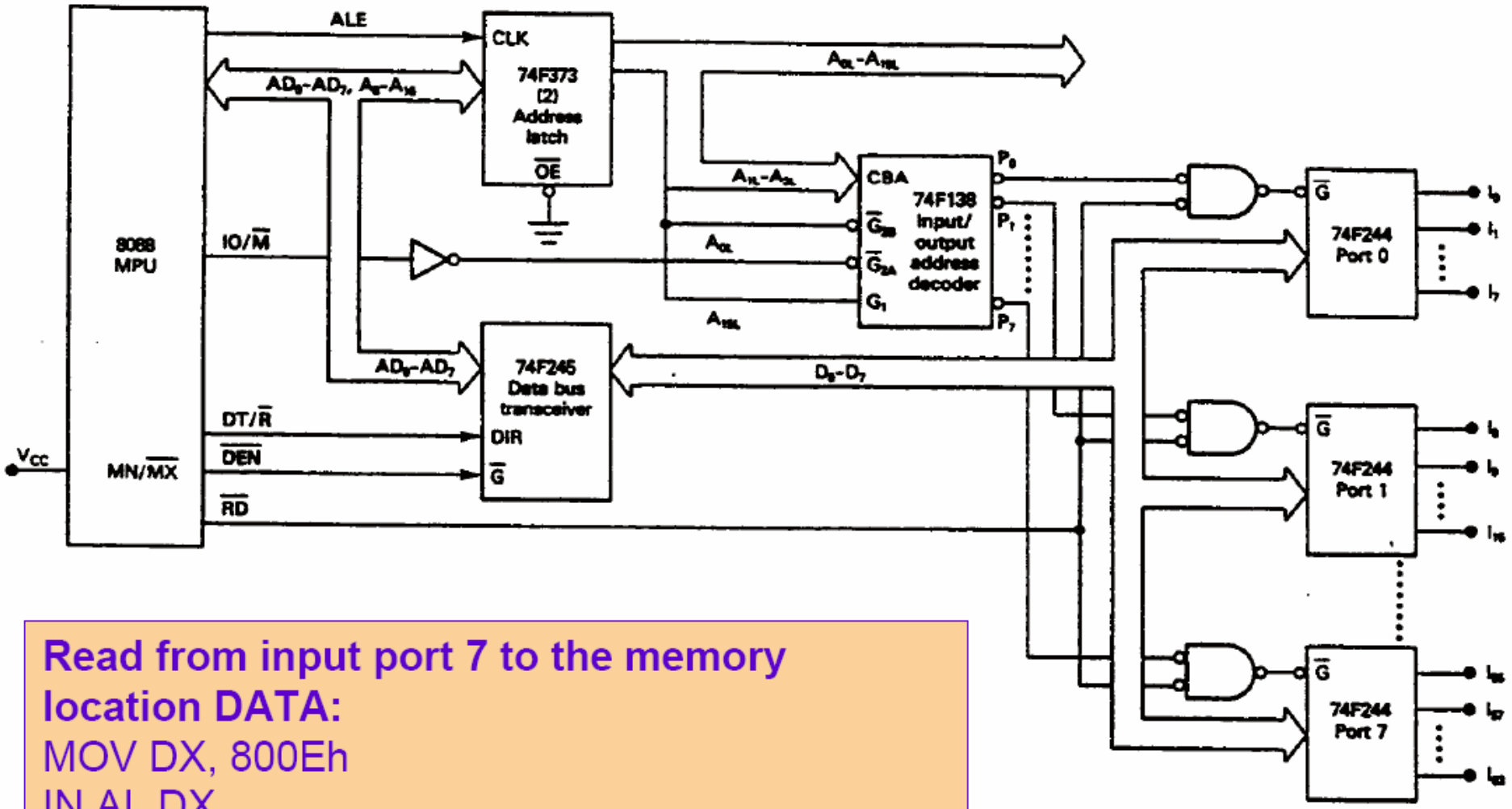
IN port design using the 74LS244

- Design for IN AL,9CH



- In order to prevent any unwanted data (garbage) to come into the system (global) data bus, all input devices must be isolated through the tri-state buffer. The 74LS244 not only plays this role but also provides the incoming signals sufficient strength (driving capability) to travel all the way to the CPU
- It must be emphasized that every device (memory, peripheral) connected to the global data bus must have a latch or a tri-state buffer. In some devices such as memory, they are internal but must be present.

Example - 64 line parallel input circuit



Read from input port 7 to the memory location DATA:

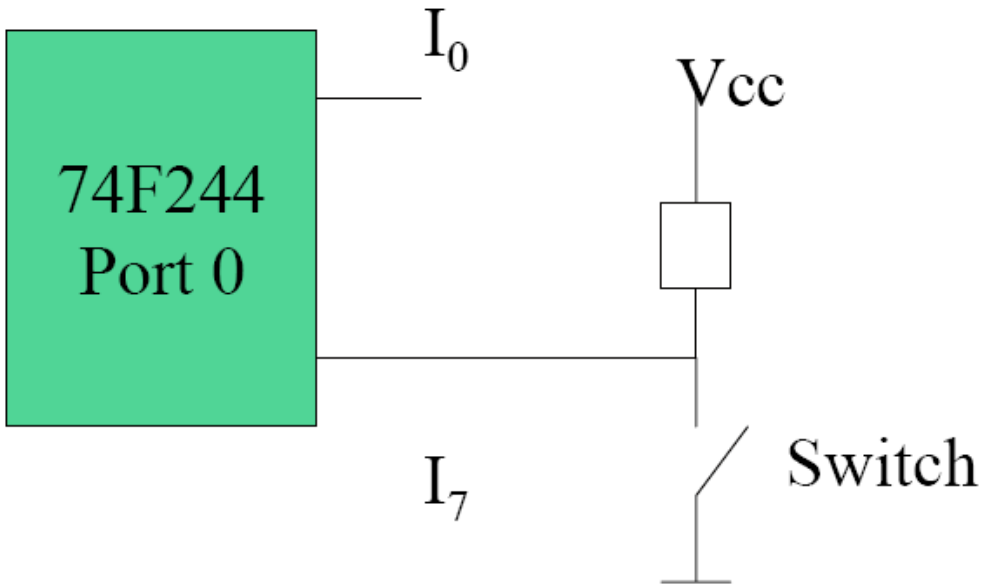
MOV DX, 800Eh

IN AL,DX

MOV DATA, AL

Example

- In practical applications, it is sometimes necessary within an I/O service routine to repeatedly read the value at an input line and test this value for a specific logic level.




```
Poll the switch waiting for it to close
        MOV DX,8000h
POLL:   IN AL,DX
        SHL AL,1
        JC POLL
```

Parallel printer interface

Standard parallel printer interface: CENTRONICS

week91011_06.pdf, **pp. 21-28.**