Contents of the Lecture

3. Computer Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Parallel and Serial Buses
- Bus Arbitration
- PCI Bus
- PCI Express Bus
- Other Serial Buses
- VME Bus

Introduction (1)

- Computer buses: electrical pathways for transmission of signals between various modules of a computer system
- Computer systems have several different buses:
  - A system bus for connecting the CPU to the memory
  - One or more I/O buses for connecting the peripheral devices to the CPU

Introduction (2)

- Certain devices connected to the bus are active and may initiate a transfer ⟶ *master*
- Other devices are passive and wait for transfer requests ⟶ *slave*
- Example: The CPU requests a disk controller to read or write a data block
  - The CPU is acting as a *master*
  - The controller is acting as a *slave*

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Electrical Considerations (1)

- Designing high-performance buses requires to minimize several undesirable electrical phenomena
  - Cause the decrease of systems' reliability
- The most important: *signal reflections*
- Signal reflections are the result of impedance discontinuities: connectors, capacitive loads, device inputs, board layer changes

Electrical Considerations (2)

- Signal reflections have the effect of voltage and current oscillations
- To eliminate signal reflections, bus termination must be used
- Termination:
  - Passive (resistive)
  - Active
- Resistive terminators can be connected in series or in parallel

Electrical Considerations (3)

- Series termination
- In the ideal case:

  $R_s + Z_s = Z_0$

  Z_s – source impedance

  Z_0 – line impedance

Electrical Considerations (4)

- Parallel termination
- A resistor is placed at the receiving end → split resistor network
- The equivalent resistance R_e should equal the line impedance Z_0
- May be used for bidirectional buses

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Data Transfer Synchronization

- Data Transfer Synchronization
  - Synchronous Buses
  - Asynchronous Buses

Data Transfer Synchronization

- Depending on the synchronization of data transfers, buses can be divided into:
  - Synchronous
  - Asynchronous
- Operations of synchronous buses are controlled by a clock signal → require an integral number of clock periods
- Asynchronous buses do not use a clock signal → bus cycles can have any duration

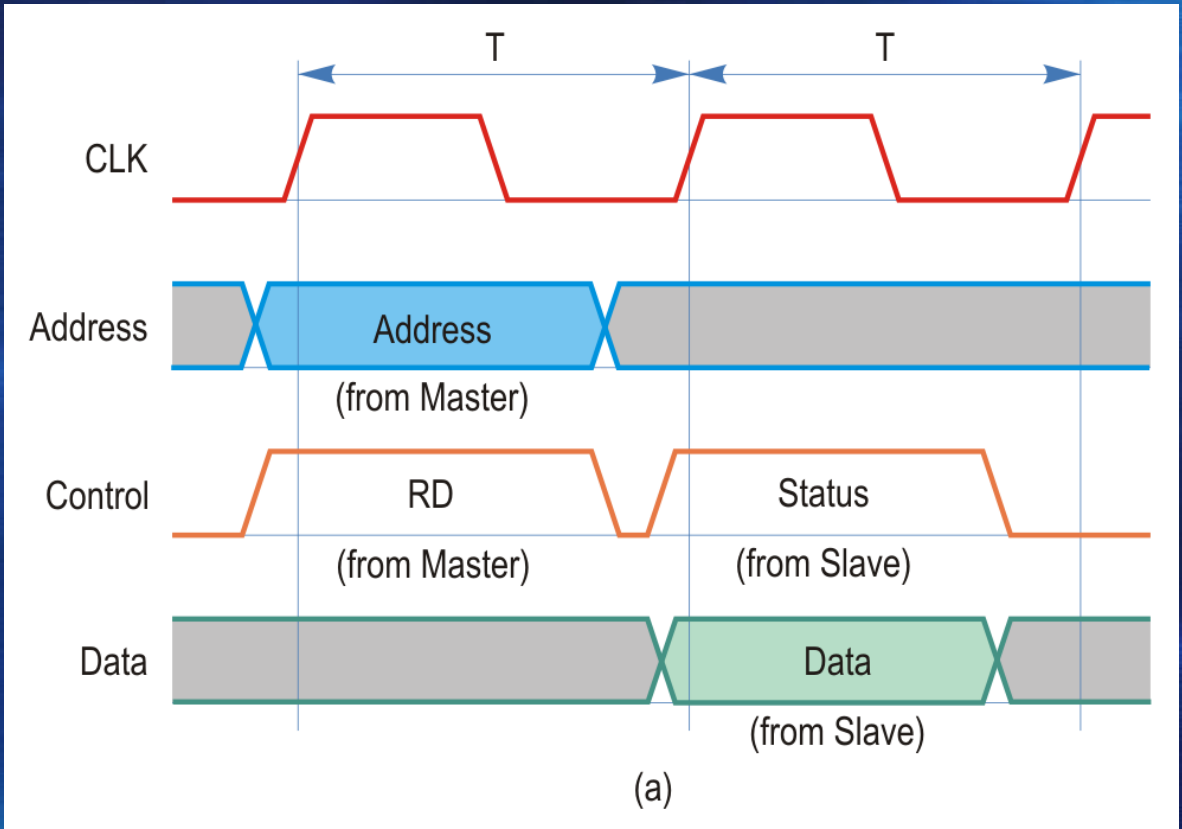
Data Transfer Synchronization

- Data Transfer Synchronization
  - Synchronous Buses
  - Asynchronous Buses

Synchronous Buses (1)

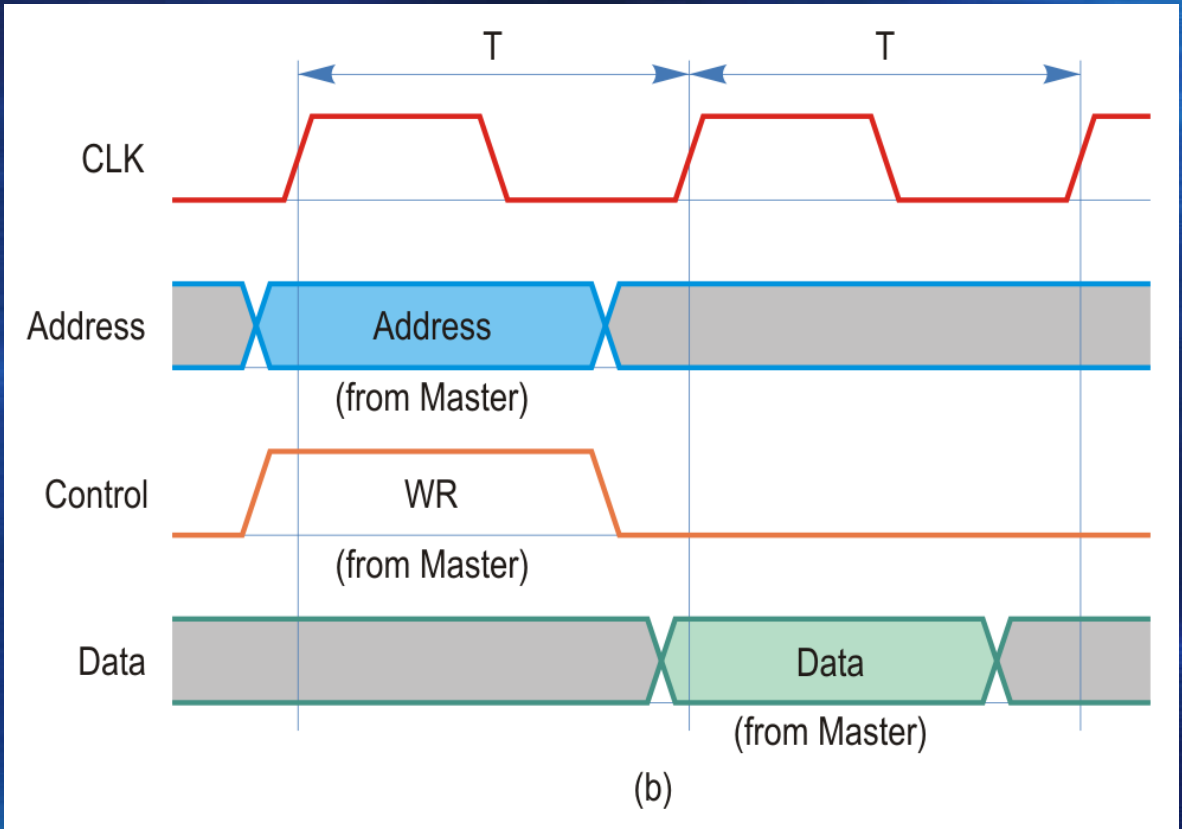
- Each word is transferred during an integral number of clock cycles
- This duration is known to both the source and destination units → synchronization
- Synchronization:
  - Connecting both units to a common clock signal → short distances
  - Using separate clock signals for each unit → synchronization signals must be transmitted periodically

Synchronous Buses (2)



Synchronous transfer – Read

Synchronous Buses (3)



Synchronous transfer – Write

Synchronous Buses (4)

- The requirement that the *slave* unit responds in the next clock cycle can be eliminated
- An additional control signal *ACK* or *WAIT* is provided, controlled by the *slave* unit
  - The signal is only asserted when the *slave* unit has completed its data transfer
- The *master* unit waits until it receives the *ACK* or *WAIT* signal → *wait states* are inserted

Synchronous Buses (5)

- Disadvantages of synchronous buses:
  - If a transfer is completed before an integral number of cycles, the units have to wait until the end of the cycle
  - The speed has to be chosen according to the slowest device
  - After choosing a bus cycle, it is difficult to take advantage of future technological improvements

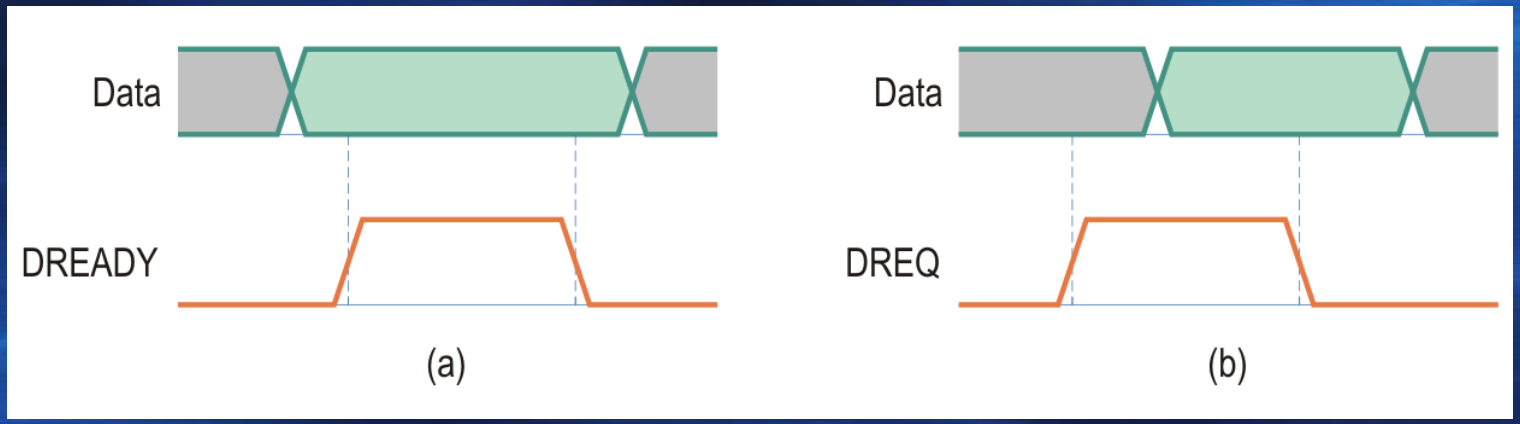
Data Transfer Synchronization

- Data Transfer Synchronization
  - Synchronous Buses
  - Asynchronous Buses

Asynchronous Buses (1)

- An asynchronous bus eliminates the disadvantages of synchronous buses
- Instead of the clock signal, additional control signals are used, and a logical protocol between the units (source, destination)
- The protocol may be:
  - Unidirectional – the synchronization signals are generated by one of the two units
  - Bidirectional – both units generate synchronization signals

Asynchronous Buses (2)

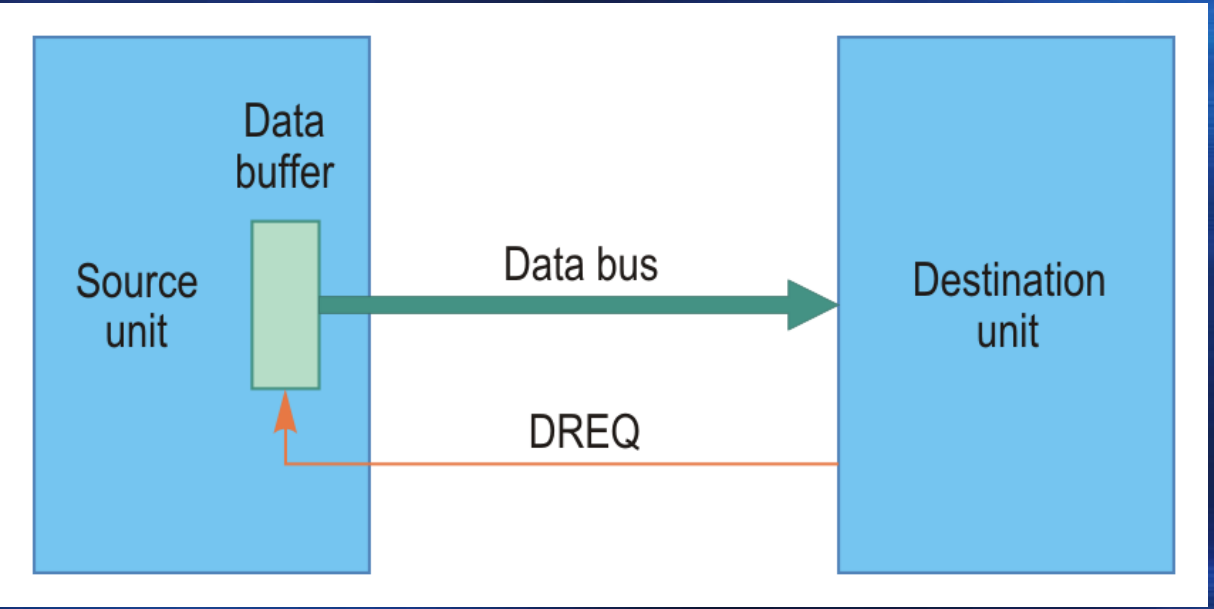


- Transfer through unidirectional protocol
- (a) Source-initiated transfer
  DREADY (*Data Ready*)
- (b) Destination-initiated transfer
  DREQ (*Data Request*)

Asynchronous Buses (3)

- The *DREADY* and *DREQ* signals can be used to:
  - Transfer the data from the source unit to the bus
  - Load the data from the bus by the destination unit
- Strobe signals
- Example: The source unit generates a data word asynchronously and places it in a buffer register

Asynchronous Buses (4)

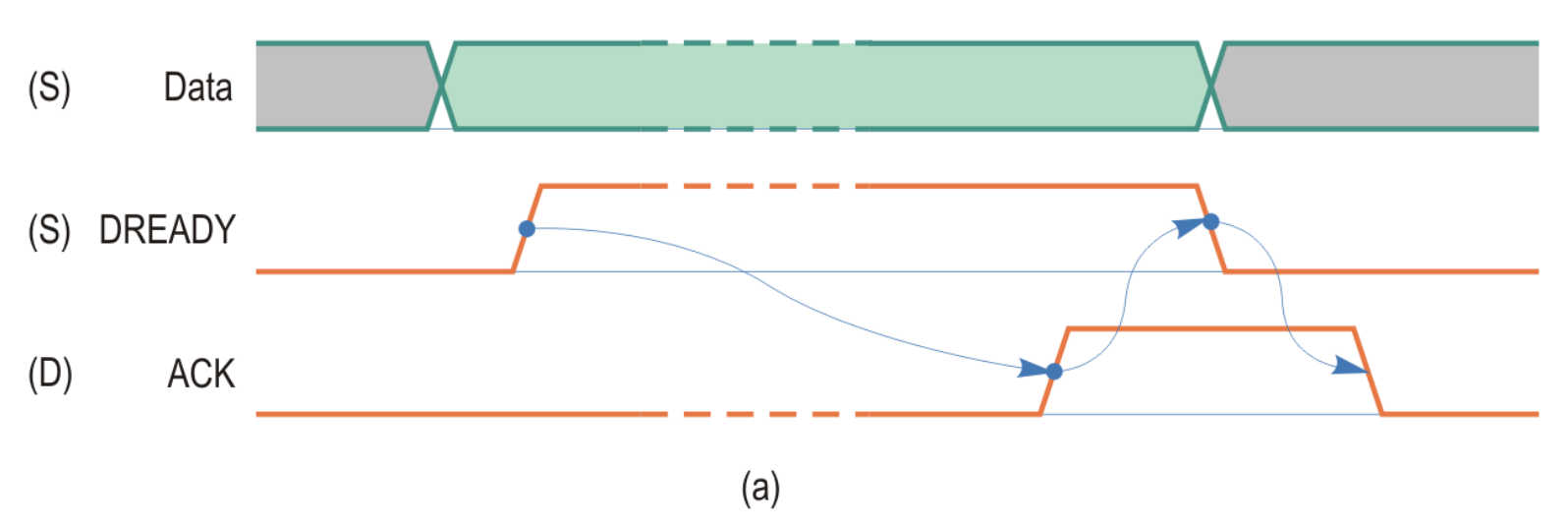


- The *DREQ* signal enables the clock input of the buffer

Asynchronous Buses (5)

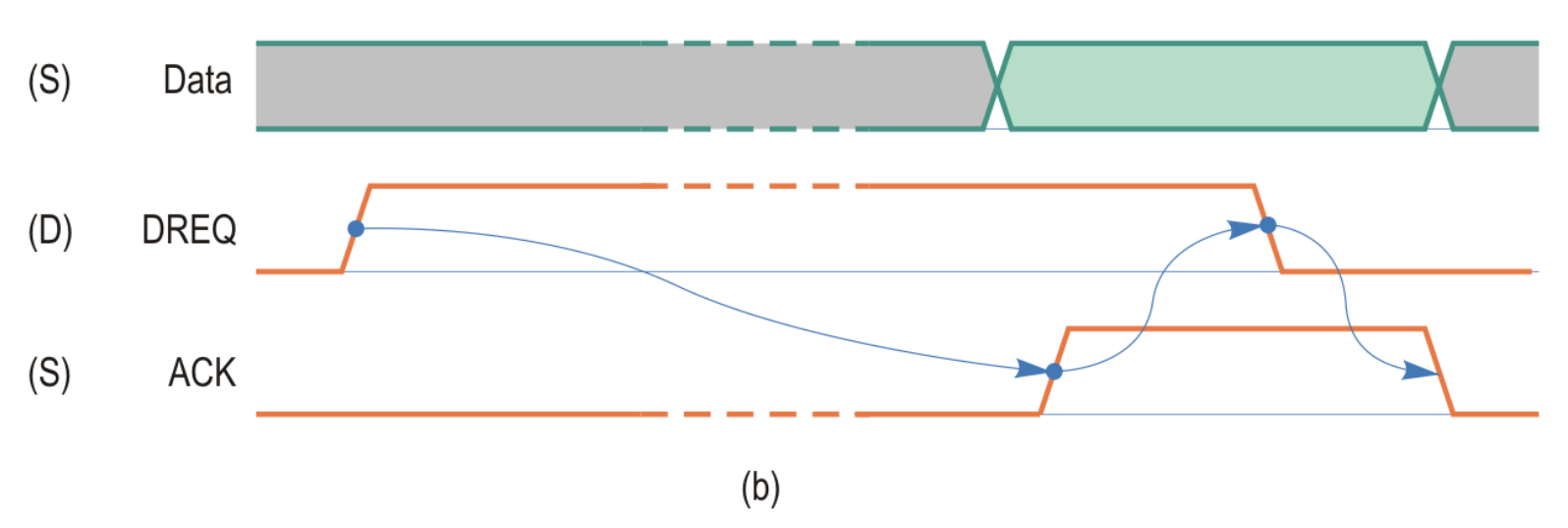
- Disadvantage of unidirectional protocol: does not allow to verify the successful completion of the transfer
  - Example: in a source-initiated transfer, the source does not have a confirmation of data reception by the destination
- Solution: introducing an acknowledge signal *ACK* $\rightarrow$ bidirectional protocol

Asynchronous Buses (6)



(a) Source-initiated transfer through bidirectional protocol

Asynchronous Buses (7)



(b) Destination-initiated transfer through bidirectional protocol

Summary

- Signal reflections may affect the reliability of computer systems
  - To eliminate or reduce signal reflections, bus terminators must be used
  - May be connected in series or in parallel
- Although synchronous buses have drawbacks, most buses are synchronous
- Asynchronous buses eliminate some disadvantages of synchronous buses
  - Bidirectional transfer protocols are more reliable

Concepts, Knowledge

- Signal reflections
- Series and parallel bus termination
- Synchronous buses
- Read/write operations on a synchronous bus
- Asynchronous buses
- Source-initiated transfer, unidirectional
- Destination-initiated transfer, unidirectional
- Source-initiated transfer, bidirectional
- Destination-initiated transfer, bidirectional