3. Computer Buses

- Introduction
- Electrical Considerations
- Data Transfer Synchronization
- Parallel and Serial Buses
- Bus Arbitration
- PCI Bus
- PCI Express Bus
- Other Serial Buses
- VME Bus

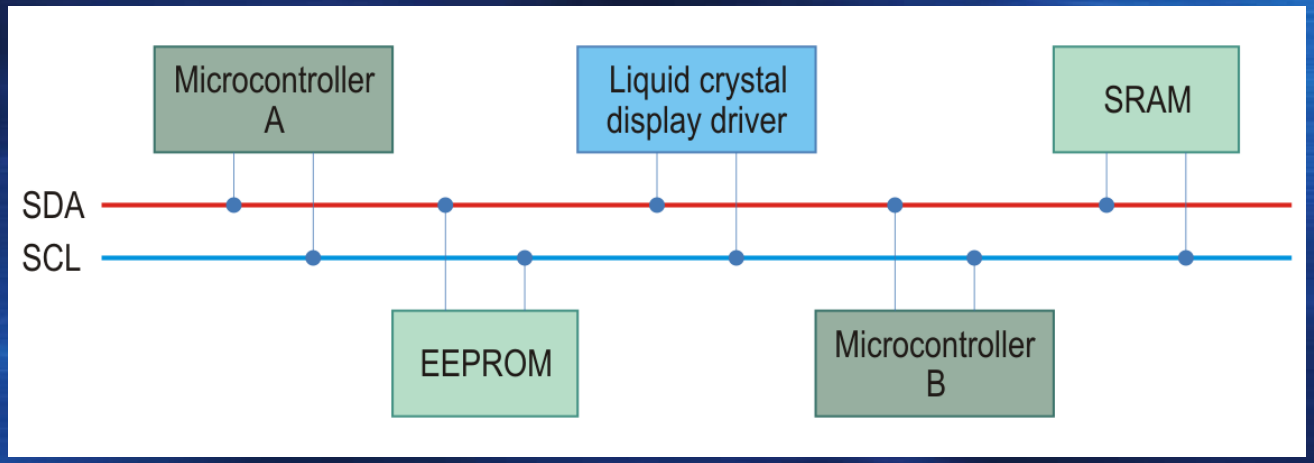
Other Serial Buses

- Other Serial Buses
  - I^2C Bus
  - SPI Bus
  - USB

I^2C Bus

- I^2C Bus
  - I^2C Bus Overview
  - START and STOP Conditions
  - Data Transfers
  - I^2C Bus Variants

I²C Bus Overview (1)



- I²C (*Inter-Integrated Circuits*) – Philips
- Bidirectional bus with two wires:
  - SDA (*Serial Data*)
  - SCL (*Serial Clock*)

I^2C Bus Overview (2)

- A device connected to the I^2C bus can operate as:
  - Receiver
  - Transmitter and receiver
- Each device has a unique address
- Transmitters and receivers can operate either in *master* or *slave* mode
- Multiple master devices can be connected to the bus
  - Arbitration procedure

I²C Bus

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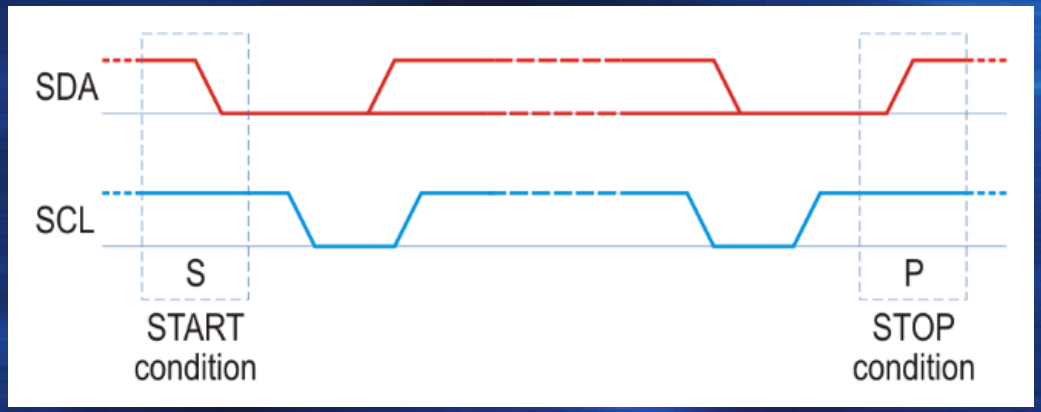
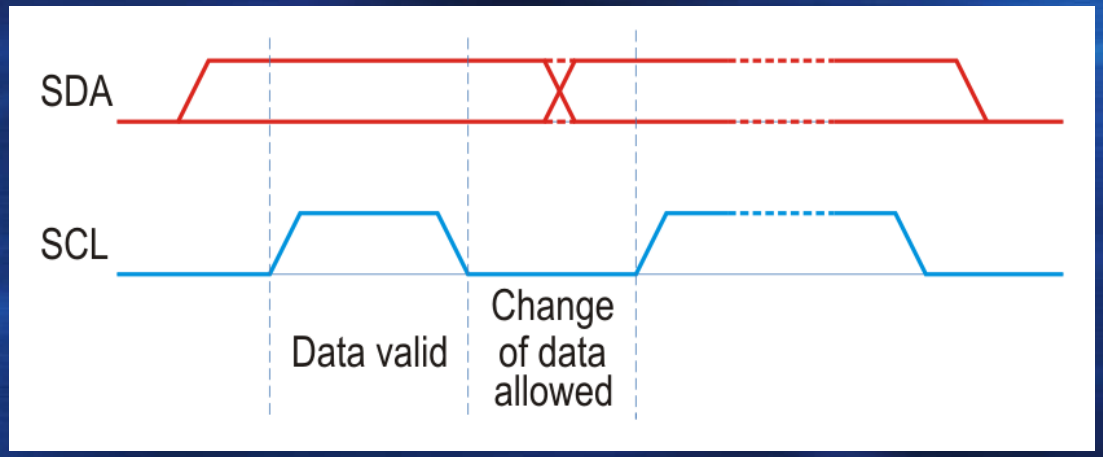
START and STOP Conditions (1)



- Generated by the master device
- START condition:
  - 1 → 0 transition on the SDA line, SCL = logical 1
- STOP condition:
  - 0 → 1 transition on the SDA line, SCL = logical 1

START and STOP Conditions (2)



- Data on the SDA line must be stable while SCL is logical 1
- Data can be changed only when SCL is logical 0

I²C Bus

- I²C Bus
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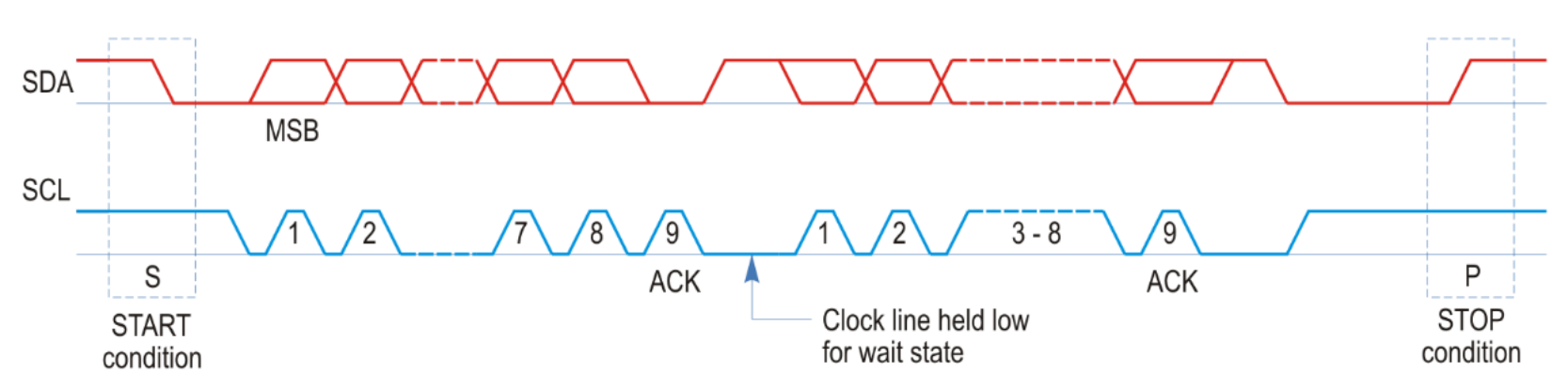
  - START and STOP Conditions
  - Data Transfers
  - I²C Bus Variants

Data Transfers (1)

- Categories of information sent on the I^2C bus, between the START and STOP conditions:
  - Slave device address
    - 7 bits or 10 bits
  - Read/write bit
  - Data bits, in segments of 8 bits each
  - Acknowledge bit
    - Sent after each data segment

Data Transfers (2)



- Example transfer
  - The number of bytes in a transfer is not restricted
  - The receiver can force the transmitter into a wait state

Data Transfers (3)

- Three formats for data transfers:
  - Write data from a master transmitter to a slave receiver
  - Read data by a master device
  - Multiple read and write transfers
- The address and direction of data are encoded in the first byte after the START condition
  - LSB = 0: write data from master
  - LSB = 1: read data from slave

I^2C Bus

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I^2C Bus Variants (1)

- Original I^2C bus
  - Maximum transfer rate of 100 Kbits/s
  - 7-bit addresses
- Version 2.0
  - Fast transfer mode, max. 400 Kbits/s
  - 10-bit addresses
  - Possibility to connect devices with 7-bit or 10-bit addresses

I^2C Bus Variants (2)

- Version 2.1
  - Shifting of voltage levels (Level-shifting) in order to connect devices with different supply voltages
  - Extended specifications for devices with voltages below 2.7 V
  - High-speed transfer mode ⟶ maximum 3.4 Mbits/s

Other Serial Buses

- Other Serial Buses
  - I^2C Bus
  - SPI Bus
  - USB

SPI Bus

- SPI Bus
  - SPI Bus Overview
  - SPI Bus Signals
  - SPI Bus Operation
  - Advantages and Disadvantages
  - Comparison to I^2C Bus

SPI Bus Overview

- SPI (*Serial Peripheral Interface*)
  - Developed by Motorola and adopted by numerous manufacturers
  - Synchronous serial bus
  - Full duplex communication
    - Four communication lines
    - Data are transferred in both directions
  - Master/slave communication mode
    - Several slave devices may be connected

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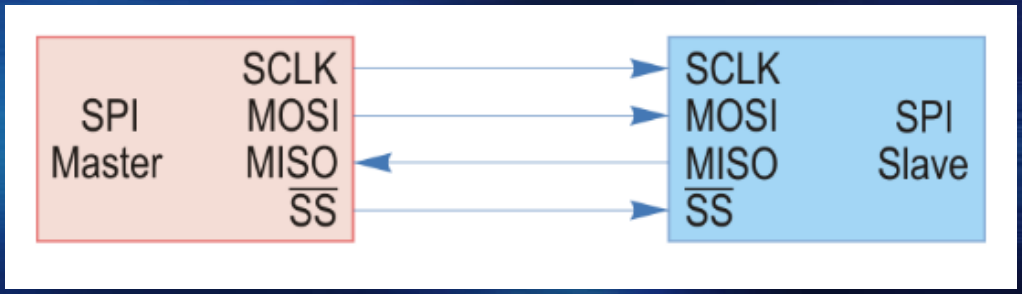
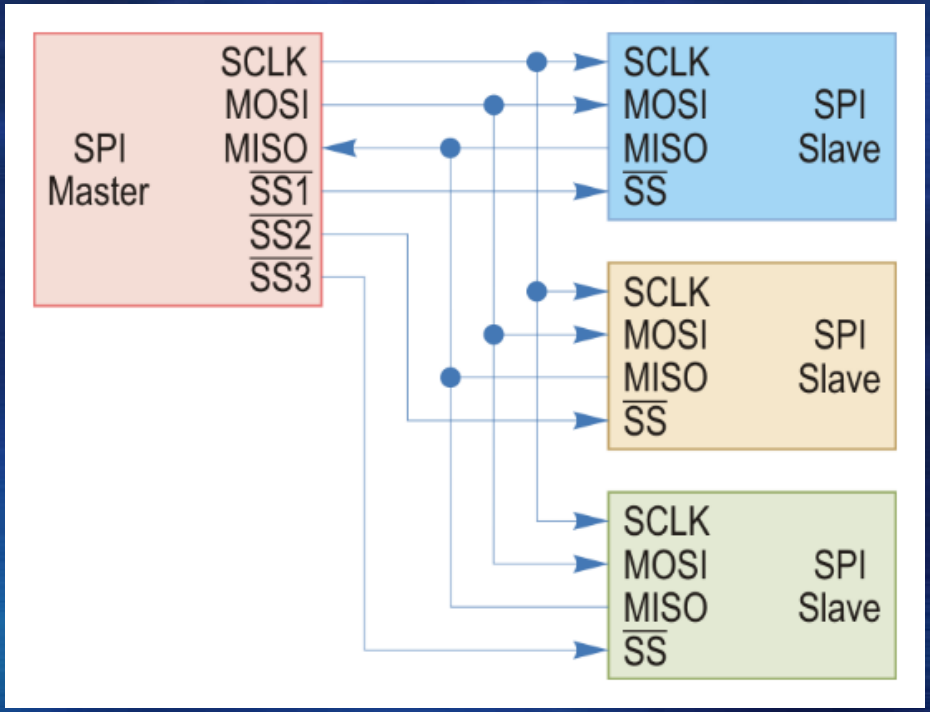
SPI Bus Signals (1)

- Four signals:
  - SCLK (*Serial Clock*)
  - MOSI (*Master Output, Slave Input*)
  - MISO (*Master Input, Slave Output*)
  - nSS (*Slave Select*)
- Configuration with a single slave device



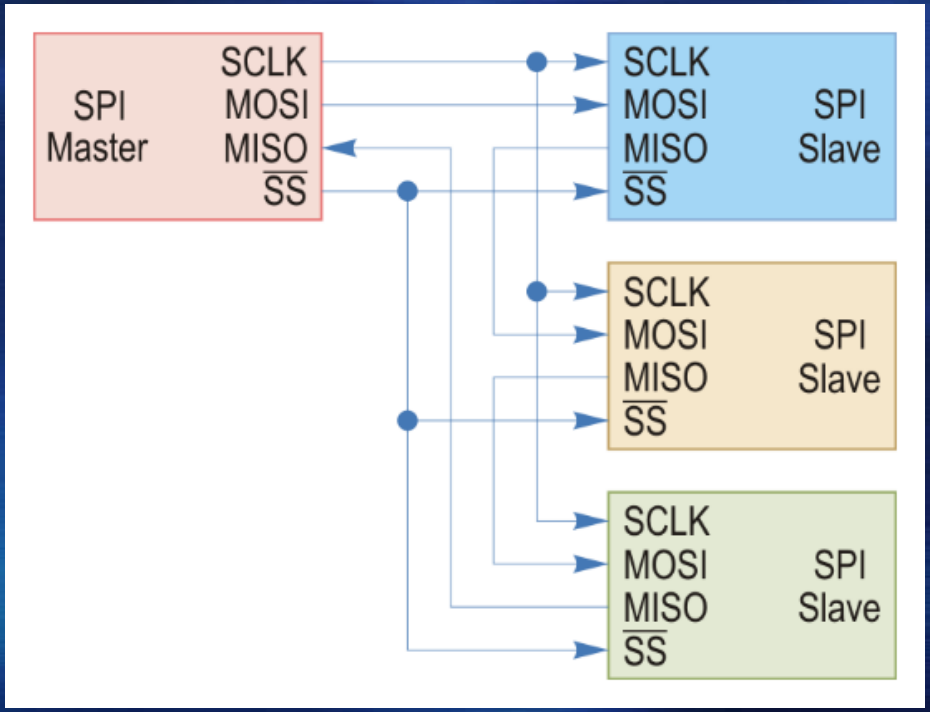
SPI Bus Signals (2)

- Configuration with three slave devices



SPI Bus Signals (3)

- Configuration with three slave devices connected in a daisy-chain



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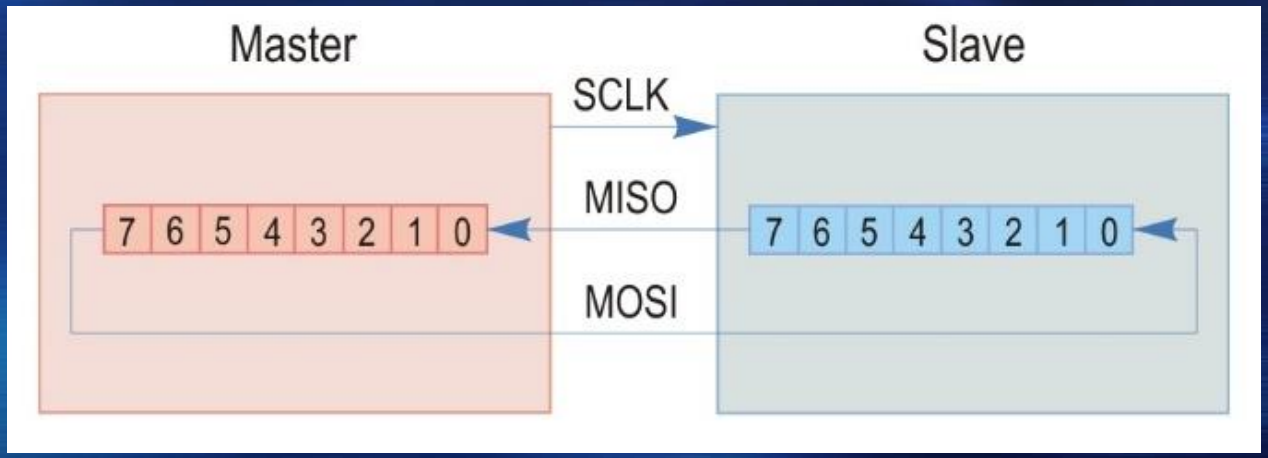
SPI Bus Operation (1)

- Data transmission
  - Configuring the frequency of the clock signal (1 .. 70 MHz)
  - Selecting the slave device
  - Optionally: waiting time (e.g., for analog-to-digital conversion)
  - Clock cycles for duplex communication:
    - M → MOSI line → S
    - S → MISO line → M

SPI Bus Operation (2)

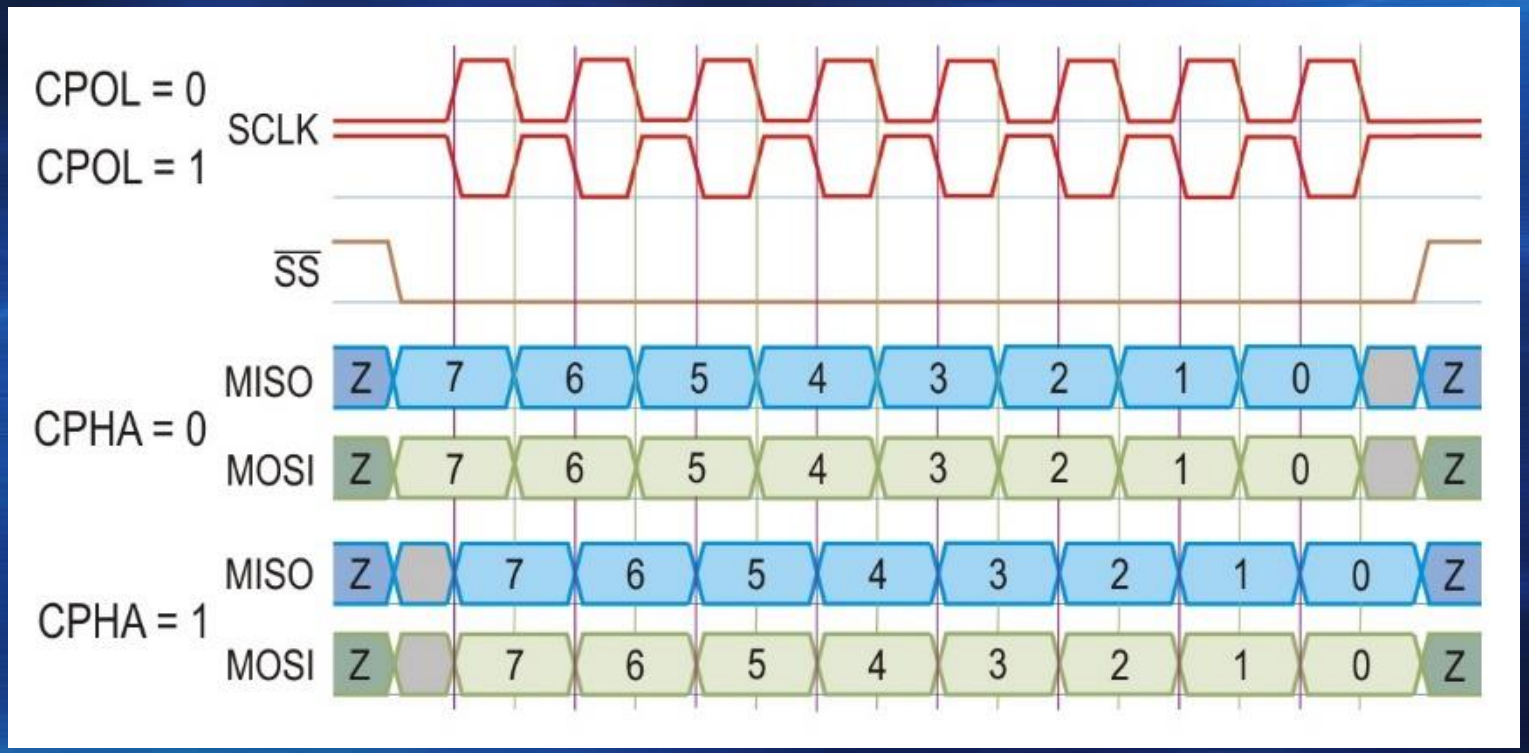
- Two shift registers are used
- Usually, the first bit is the MSB
- Extent: any number of clock cycles
- The word size depends on the application



SPI Bus Operation (3)

- Clock polarity and phase
  - Clock polarity (CPOL): determines the base (initial) value of the clock signal (0, 1)
  - Clock phase (CPHA): determines the edge upon which data are read and modified
  - CPOL = 0
    - CPHA = 0: read on the rising edge, modify on the falling edge
    - CPHA = 1: read on the falling edge, modify on the rising edge

SPI Bus Operation (4)



SPI Bus Operation (5)

- Modes
  - Mode: combination between the clock polarity (CPOL) and clock phase (CPHA)
  - The following convention is used:

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

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Advantages and Disadvantages

- Advantages
  - Duplex communication
  - High transfer speed
  - Simple hardware interface
- Disadvantages
  - Lack of data flow control
  - Lack of acknowledgement from slave device
  - Lack of standardization → several variants
  - Difficulty to create multi-master systems

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Comparison to I^2C Bus

- SPI is more advantageous for sending data streams (DSP, convertors)
- SPI has higher transfer rates
- SPI is more efficient for applications that require duplex communication
- SPI does not support device addressing
  - I^2C is more advantageous for systems with more than one slave device

Other Serial Buses

- Other Serial Buses
  - I^2C Bus
  - SPI Bus
  - USB

USB

- USB
  - USB Overview
  - USB Topology
  - USB Versions
  - USB Cables and Connectors
  - USB Electrical Interface
  - USB Transfer Types

USB Overview (1)

- USB – *Universal Serial Bus*
- Developed by a group of companies: HP, Compaq, Intel, Lucent, Microsoft, NEC
- *USB Implementers Forum* (www.usb.org)
- Motivations:
  - Simplify the connections with peripherals
  - Provide high data transfer rates
  - Ease of use ("*Plug and Play*")
  - Eliminate the restrictions due to insufficient hardware resources

USB Overview (2)

- Features
  - Detects the attachment of a peripheral device
  - Determines the resources it needs
  - Hot-plug capability
  - Tree-like interconnection, with up to 127 peripherals
  - The peripherals are powered with +5 V through the cable
  - Master/slave (host/device) architecture: data transfers initiated by the master

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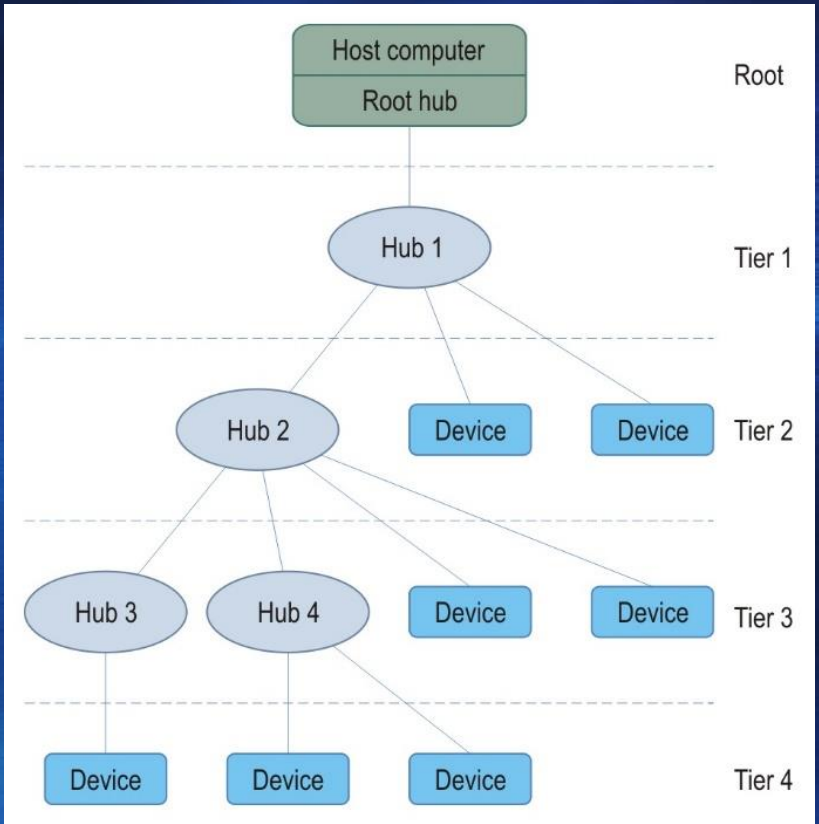
USB Topology (1)

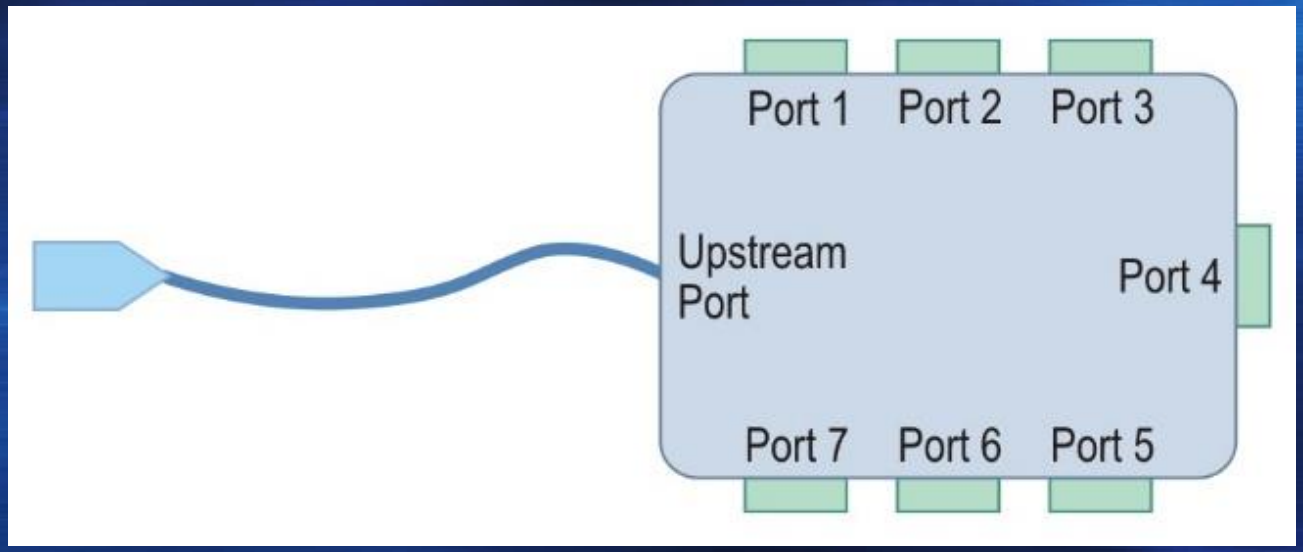


- Hubs
- Functions (devices)

USB Topology (2)

- USB Hubs
  - Recognize attachment of a peripheral
  - Provide a power of at least 0.5 W for each peripheral during initialization
  - Can provide a power of up to 2.5 W, 4.5 W, or 9 W for peripheral operation
  - Each hub consists of:
    - Repeater: switch
    - Controller: interface registers for communication with the host

USB Topology (3)



- Upstream port (for host)
- Downstream ports (for functions)
- Cascaded connection up to 5 levels

USB Topology (4)

- USB Functions
  - USB peripherals that are able to transmit or receive data or control information
  - A peripheral may contain multiple functions
  - Must respond to transaction requests sent by the host
  - Contain configuration information that describe their capabilities and resources needed
  - Configuring a function: allocating bandwidth and selecting configuration options

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USB Versions (1)

- USB 1.0: max. 12 Mbits/s
- USB 1.1: max. 12 Mbits/s
  - Low-speed channel (1.5 Mbits/s)
- USB 2.0
  - The maximum transfer rate increased 40 times, to 480 Mbits/s (High-Speed)
  - Uses the same cables, connectors, and software interfaces
  - Enables to use new types of peripherals: video cameras, scanners, printers, disk drives

USB Versions (2)

- USB On-The-Go (USB OTG)
  - Supplement to USB 2.0 (2006)
  - A device may have either the master or slave role (host, peripheral)
    - Protocol to exchange the host/peripheral role
  - Two devices can communicate with each other without a computer
    - Tablet → printer
    - Printer → camera

USB Versions (3)

- USB 3.0
  - Specification completed in 2008 by the USB 3.0 Promoter Group
  - SuperSpeed mode: 5 Gbits/s
  - Two simplex differential channels in addition to the existing differential channel → a total of 8 wires
  - Technology similar to PCI Express 2.0 → 8b/10b encoding (500 MB/s)

USB Versions (4)

- USB 3.1 (2013)
  - "SuperSpeed+ USB 10 Gbps" transfer mode
  - USB 3.1 Gen 2: marketing name
  - The encoding has been changed from 8b/10b to 128b/132b
  - Compatibility with USB 3.0 and USB 2.0
  - The *USB Power Delivery* specification indicates three power levels: 10 W (5 V, 2 A); 60 W (12 V, 5 A); 100 W (20 V, 5 A)

USB Versions (5)

- USB 3.2 (2017)
  - "SuperSpeed+ USB 20 Gbps" transfer mode
    - Operation on two lanes
    - Uses the existing wires intended for flipping capabilities of the Type-C connector
  - The same 128b/132b encoding
  - Compatibility with USB 3.1, 3.0, and 2.0
    - USB 3.2 Gen 1x1 (5 Gbits/s); USB 3.2 Gen 1x2 (10 Gbits/s); USB 3.2 Gen 2x1 (10 Gbits/s)

USB Versions (6)

- USB4 (2019)
  - Based on the Thunderbolt 3 protocol
  - The data rate has been increased
    - Version 1.0: up to 40 Gbits/s
    - Version 2.0: up to 80 Gbits/s
  - Multiple simultaneous data and display protocols → protocol tunneling
    - Protocols: USB 3.x SuperSpeed, PCI Express, DisplayPort
  - Packets can be specifically allocated for data connections between hosts

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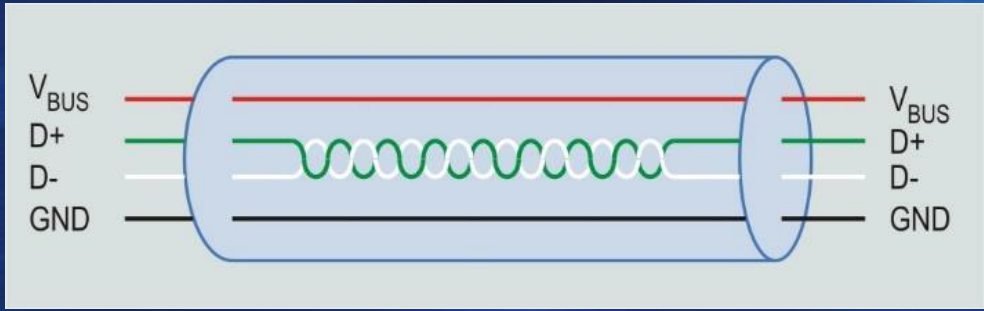
USB Cables and Connectors (1)

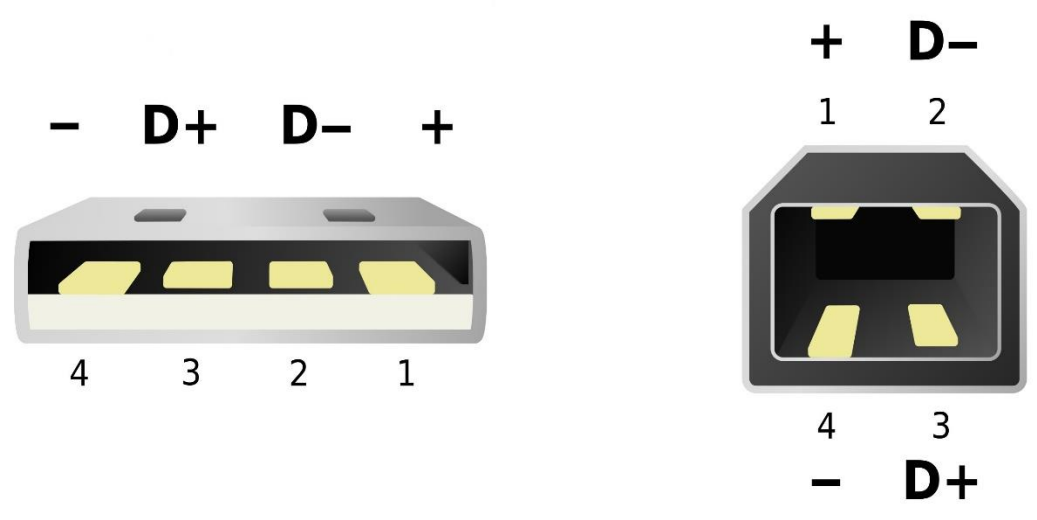


- USB 2.0 cable
  - Differential signals on the D+ and D- wires
  - Supply voltage for peripherals on the V_{BUS} wire
  - Terminations at each end of the cable
    - Provide correct voltage levels for peripherals
    - Allow detection of attachment and removal of devices
    - Differentiate between full-speed and low-speed devices

USB Cables and Connectors (2)

- The original USB specification defines Type-A and Type-B plug and socket connectors
- Hosts and hubs: Type-A socket (rectangular)
- Peripherals: Type-B socket (square)
- In general, cables have only plug connectors

USB Cables and Connectors (3)



- The data pins in the Type-A plug connector are recessed compared to the power pins
- Some devices operate in a different mode when the connector is only partially inserted

USB Cables and Connectors (4)

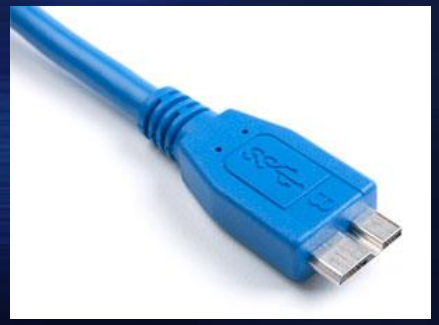
- Mini-USB and micro-USB connectors for tablets, smartphones, cameras
- Mini-A, Mini-B: 7 x 3 mm; not used in new devices
- Micro-A, Micro-B: 7 x 1.5 mm

USB Cables and Connectors (5)

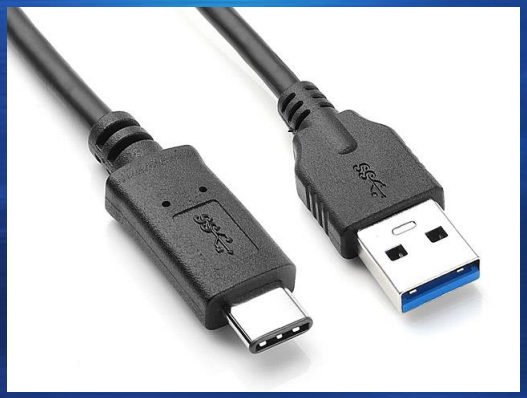
- USB OTG Connectors
  - Micro-AB socket connectors
  - Enable to insert either a Micro-A or a Micro-B plug connector
  - ID pin: used to detect the type of the plug connector inserted
    - Grounded in Micro-A, floating in Micro-B
    - When a Micro-A plug is inserted: the socket supplies voltage $\rightarrow$ host role for the device with the Micro-AB socket

USB Cables and Connectors (6)

- USB 3.0 Connectors
  - Type-A connectors
    - Compatible with USB 2.0 type-A connectors
    - Contain 5 additional pins
  - Type-B connectors
    - Not compatible with USB 2.0 connectors
  - Micro-B
    - One USB 2.0 micro-B connector
    - One additional connector



USB Cables and Connectors (7)



- Type-C Connectors
  - Specifications developed in 2014; updated in 2017, 2019
  - Used by both the host computer and USB devices
  - Contain 24 pins, including two pins for cable orientation detection → reversible
  - Size: 8.4 x 2.6 mm
  - Maximum current: 1.5 A or 3 A
  - Alternate modes: DisplayPort, HDMI

USB

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USB Electrical Interface

- Data are encoded → generation of a receive clock signal is simplified
- The encoding used is NRZI (*Non-Return to Zero Inverted*)
  - Bit of 1: no change in the voltage level
  - Bit of 0: change in the voltage level, without return to zero voltage between encoded bits
- Extra bits inserted to ensure enough transitions of the transmitted signals

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USB Transfer Types (1)

- Control Transfers
  - Used by the host drivers to configure the peripherals
- Bulk Transfers
  - Consist of large amounts of data
  - Used for printers, scanners etc.
  - Reliability ensured trough error detection code, retries of erroneous transfers
  - Transfer rate can vary

USB Transfer Types (2)

- Interrupt Transfers
  - Used for small amounts of data
  - A data transfer may be requested by a peripheral at any time
  - The transfer rate cannot be lower than that specified by the peripheral
  - Data consist of event notification, characters, or coordinates

USB Transfer Types (3)

- Isochronous Transfers
  - *Isos* – equal, uniform; *chronos* – time
  - Isochronous – with equal duration; that occurs at equal intervals
  - Used for data generated in real time, that must be delivered at the rate at which data are received
  - The maximum delivery delay must also be ensured

USB Transfer Types (4)

- The timely delivery of data is ensured at the expense of potential losses in the data stream
- Dedicated portion of bandwidth
- Isochronous transfers:
  - Timely data delivery
  - Lack of retries for erroneous data
- Asynchronous transfers:
  - Correct data delivery
  - Retries for erroneous data

Summary (1)

- I^2C (*Inter-Integrated Circuits*) bus
  - Developed for the communication between microcontrollers and various peripherals
  - To achieve bus control, a START condition has to be generated
  - To release the bus, a STOP condition has to be generated
  - Each byte sent is followed by an acknowledge bit
  - Operating modes: standard (100 Kbits/s), fast (400 Kbits/s), high-speed (3.4 Mbits/s)

Summary (2)

- SPI (*Serial Peripheral Interconnect*) bus
  - Enables duplex communication
  - The master device selects the slave device and generates the clock pulses
  - The master device must configure the polarity and phase of the clock signal
  - No address is sent
  - The word size depends on the application
  - There is no acknowledgement from the slave device

Summary (3)

- USB (*Universal Serial Bus*)
  - Main features:
    - When a peripheral is attached, its required resources are determined
    - Master/slave architecture
    - Star topology, with hubs and functions
  - USB OTG enables a USB device to initiate transfers with another device
  - USB 3.0 adds two differential channels → SuperSpeed mode (5 Gbits/s)

Summary (4)

- USB 3.1 uses the 128b/132b encoding → SuperSpeed+ USB 10 Gbps mode
- USB 3.2 introduces the SuperSpeed+ USB 20 Gbps mode
- USB4 increases the maximum data rate of USB 3.2 and introduces protocol tunneling
- Types of data transfers:
  - Control; bulk; interrupt; isochronous
  - Isochronous transfers enable to allocate a dedicated portion of bandwidth for data generated in real time

Concepts, Knowledge (1)

- Overview of I^2C bus
- START and STOP conditions on the I^2C bus
- Data transfers on the I^2C bus
- I^2C bus variants
- Overview of SPI bus
- Data transmission on the SPI bus
- SPI bus clock polarity and phase
- Advantages and disadvantages of SPI bus
- Comparison between I^2C and SPI buses

Concepts, Knowledge (2)

- USB features
- USB hubs and functions
- USB OTG version
- USB 3.0 version
- USB 3.1 version
- USB 3.2 version
- USB4 version
- Functions of USB terminators
- Electrical interface of USB
- Transfer types on the USB