Synchronization of the bit-clock in the receiver

Necessity

- the recovery and synchronization of the local bit-clock in the receiver is required for two reasons:
- the sampling of the coded received signal should be performed with a clock synchronized to it;
- the decoding of the received encoded sequence also requires a clock signal synchronized with the encoded signal
- the decoding of the biphasic, Miller and CMI codes, which have the minimum duration of the level of the coded signal of a half bit-period, requires a local clock with $f_{local} = 2 \cdot f_{bit}$.
- in these cases, the bit clock is obtained by a frequency division of the local clock(f_{local}). But this division might insert an 180º uncertainty between the local clock and the coded signal, due to the initial condition of the divider; this uncertainty should be removed.
- the decoding of the AMI code and its variants require a clock with $f_{local} = f_{bit}$;
- the phase shift between the received encoded signal, and the local RxCk has the following causes:
- the different starting moments of the two oscillators; this generates the initial phase shift φ_0 which takes a random value between 0º and 180º;
- the difference between the frequencies of the two pilot oscillators that deliver the two clock signals; it generates a dynamic phase shift which varies according to: $\varphi_d(t)=\Delta\omega \cdot t$; (1)
- the distortions inserted by the channel
- the 180º uncertainty induced by the initial state of digital frequency dividers

- the phase difference between the two oscillators varies in time acc. to:

$$\Delta\Phi(t) = \varphi_d(t) + \varphi_0 + \pi + \varphi_{channel} \quad (2)$$

- by synchronization between the locally generated clock and the received coded signal, we mean the synchronism between the transitions of the coded signal, considered as a phase reference, and the negative transitions of the locally generated clock f_{local}, whose frequency equals f_{bit} or $2 \cdot f_{bit}$ depending on the code.

- the synchronization is accomplished in 3 steps:

- the removal of the initial phase shift φ_0, named fast or coarse synchronization; this operation is performed only once at the beginning of the transmission;
- the removal of the 180º uncertainty, called resynchronization; this is required only by the decoding of the Miller code. The decoding of the other codes presented does not require this operation;
- the removal of the dynamic phase shift $\varphi_d + \varphi_{channel}$ (caused by the frequency diff. and by channel phase hits) between the received coded signal and the locally generated clock, called dynamic synchronization. It operates during the whole transmission, after the other two steps have been performed. If the fast synchro is missing, the removal of the initial phase shift is also performed by the dynamic synchro.
- the dynamic and fast (when used) synchros are accomplished by means of Phase-Lock Loops (PLL).

PLL. General Aspects

– it is an ensemble of circuits that provides a local signal whose phase is aligned to the phase of an incomming reference signal. Its block diagram is shown in figure 1.

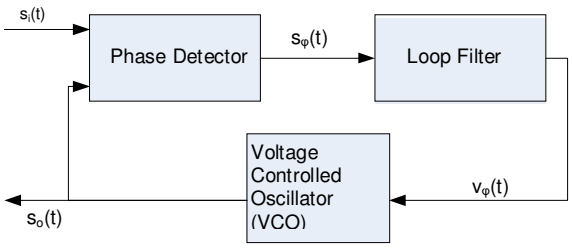


Figure 1. Block diagram of a PLL

- the phase detector (comparator) (PhD(C)) outputs a error-voltage signal whose amplitude is (ideally) proportional to the phase difference between the incoming (reference) signal $s_i(t)$ and the locally generated $s_o(t)$.
- the loop filter (LF) is a low-pass filter which retains only the low-frequency components of the error-voltage, e.g. attenuates the high-frequency components of the noise, and generates a control voltage which modifies dynamically the momentary frequency of the locally generated signal to decrease the phase offset between the $s_i(t)$ and $s_o(t)$.
- ideally, this process continues until the phase offset reaches zero, which corresponds to a constant value of the error-voltage (usually this constant value equals zero)
- in many of the practical implementations, the momentary frequency of the VCO is adjusted in order to decrease and bring towards zero (or below an imposed value), the error-voltage and, equivalently, the phase offset between the reference (input) signal and the locally-generated (output) signal .
- if the error-voltage equals zero, the frequency of the signal provided by rthe VCO is denoted as free-running frequency f_{OL}.

Types of PLLs

- *analogue or linear loops* (APLL or LPLL)
  - the phase detector is implemented with analogue circuits (e.g. analogue multiplier), the loop filter might be an active or passive analogue filter. This type of PLL uses a VCO.
- *digital loops* (DPLL)
  - is actually an analogue PLL that has the PhC implemented with digital circuits (gates, JK flop-flops, etc.). It might include a digital frequency divider and can be used as a frequency multiplier.
- *all digital loops* (ADPLL)
  - all blocks in the loop are implemented with digital circuits, and the VCO might be replaced by a controlled divider.
- *software PLL* (SPLL)
  - it is implemented using programable circuits

Descriptions and Functionalities of the component blocks

Phase Detector- PhD

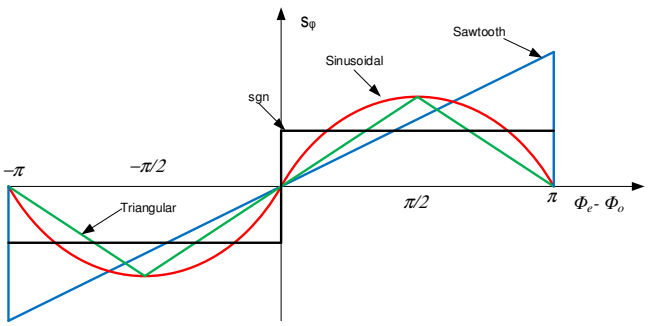
- it outputs an error signal $s_\varphi(t)$ which varies with the offset $(\Phi = \Phi_i - \Phi_o)$ between the momentary phases of the input (reference) signal $s_i(t)$ (Φ_i - the phase of the reference signal) and of the output (locally generated) signal $s_o(t)$ (Φ_o - the phase of the local signal).

- the PhD can be implemented with analogue or digital circuits.

- according to the dependency-law between the error-voltage and the phase-offset $(\Phi = \Phi_i - \Phi_o)$, the PhC could be divided in one of the following types, see figure 2:

- PhD with *linear dependency* (*or sawtooth)*
  - usually these comparators are implemented with digital circuits, while the imput signals are rectangular ones. These circuits are also named Phase-Frequency Detectors (PFD).
- PhD with *sinusoidal dependency*
  - these PhD are implemented with analogue circuits, e.g. analogue multipliers, and the input signals are harmonic, e.g. sine or cosine signals.
  - it provides an output sinchonized signal which has a phase offset of π/2, with respect to the input reference signal. The error voltage provided by this PhD is expressed by:

$$A\sin(\omega_i t)\cdot\cos(\omega_o t) = A\sin(\omega_i t)\cdot\cos(\omega_i t + \Phi(t)) = U\sin(\Phi(t)) + \sin(2\omega_i t + \Phi(t)) \qquad (3)$$



- PhD with *triangular dependency*
  - implemented with digital circuits and the input signals are rectangular
- PhD with *signum (sgn) dependency*
  - provides only the phase offset's sign; it is implemented with digital circuits, while the input signals might be either analogue or digital.

Figure 2 Types of dependencies of the Phase Detector

Voltage Controlled Oscillator -VCO

- it is an oscilator generating a (co)sinusoidal (or rectangular) waveform whose frequency deviation from the the free-running frequency (f_{OL}) is proportional to the error-voltage $V_\varphi(t)$.

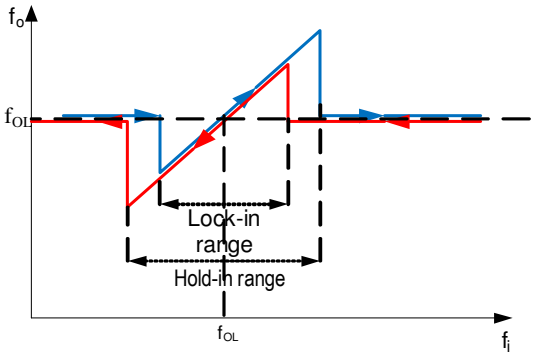
- If the error-voltage equals zero, the frequency of the generated waveform equals f_{OL}.

- So the output voltage is expressed as, see the FM lectures:

$$s_o(t) = V_0\cdot\cos\left(2\pi f_{OL}t + K_{VCO}\int_{-\infty}^{t} v_\varphi(\tau)d\tau\right) \qquad (4)$$

Loop Filter - LP

– it usually is a LP filter, which affects the dynamics and stability of the loop, because its transfer function affects the behaviour of the loop at the frequency variations of the input signal. In the same time, the charactyeristic of this filter affects the widths of the lock-in and hold-in ranges (see below) and the lock-in (synchronization) time.



Lock-In Range

– it is the frequency range (band) of the input reference signal within which the PLL is able to modify the frequency of the local signal so that its phase would be equal to the phase of the incoming reference signal, see figure 3.

- this rule applies for the case when the local signal is not initially synchronized to the incoming one.

Figure 3. Frequency variation of the local signal vs. the frequency of the reference signal

Hold-in Range

– it is the frequency range of the input signal within which the frequency of the locally generated signal, after it has been synchronized to the reference signal, can be modified so that its phase would follow the phase of the reference signal, i.e. the phase offset between the two signals would tend to zero, see fig. 3.

Lock-in (Synchronization) Time

– it is the time interval required by the PLL to ‚capture" then phase of the incoming signal, i.e. to make the phase of the local signal equal to the phase of the reference (incoming) signal.

Dynamic Synchronization - it is an ADPLL

- due to the $\Delta\omega$ (1) perfect phase synchronization between the local clock and the transitions of the received code signal is practically impossible.

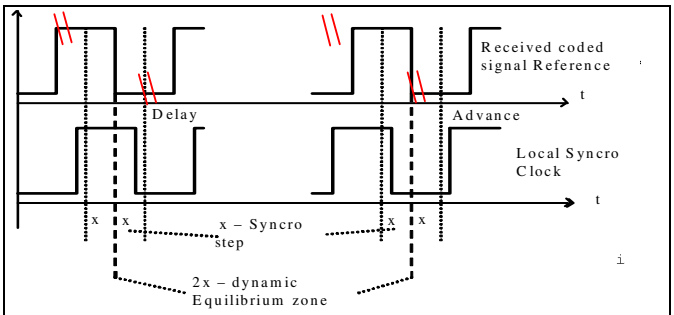


Figure 4. Dynamic equilibrium zone

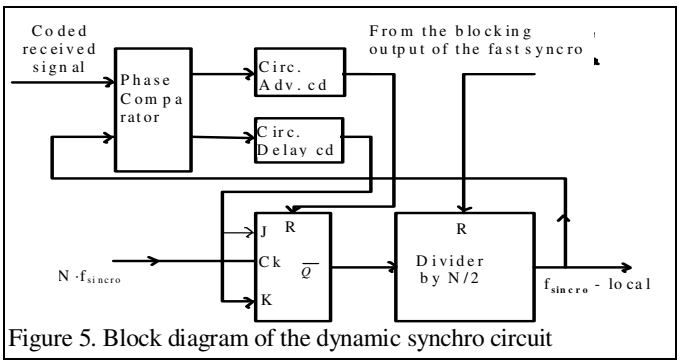


Figure 5. Block diagram of the dynamic synchro circuit

- the aim of the dynamic synchro is to keep the modulus of the phase shift (offset) between the two signals below an a priori established value, called *synchronization step*.
- the considered transitions of the two signal are aligned only at random moments; the transitions of the local clock are either ahead or behind the transitions of the coded signal, which is the reference signal, but the modulus of the phase offset would always be smaller *than the preset value x.*
- the phase-width of the "dynamic equilibrium" is 2x, see figure 4.
- the block diagram of the dynamic synchro circuit is shown in figure 5
- the phase comparator senses the relative position between the transitions of the reference RCS (received coded signal), and the negative transitions of local clock; it generates a command so that a controlled phase shift, in advance or delay, is accomplished.
- if the local clock is delayed, compared to the reference RCS, the CP will activate the Advance-clock circuit which will act upon the first cell in dividing chain, by inserting additional transitions which will shift the local clock in advance.
- if the local clock is in advance, compared to the ref. RCS, the CP activates the Delay-clock circuit which acts upon the first cell in dividing chain, by deleting transitions, thus shifting the local clock behind.
- the CP controls only the sign (sense) in which the local clock is phase-shifted; it does not control the phase shift's modulus inserted at every correction.
- the phase of the local clock signal is modified by temporarily modifying the dividing factor of the high-frequency f_{atack} clock; this is named *"phase-shift by controlled frequency division"* method.
- the CP would always indicate the phase-shift from the closest transition of the reference signal; therefore the modulus of the maximum possible phase-shift will be 180º.
- for decoding AMI, BnZs, HDB3, 4B3T, MLT-3 and b4b5 codes, $f_{sincro} = f_{bit}$,
- for decoding biphasic, Miller, CMI, $f_{sincro} = 2f_{bit}$.
- as an example of the phase shift by controlled division, we describe a dynamic synchro that synchronizes a local clock f_{sincro}, employing a divider clock with a frequency $f_{atack} = 2^n = 32 \cdot f_{synchro}$.

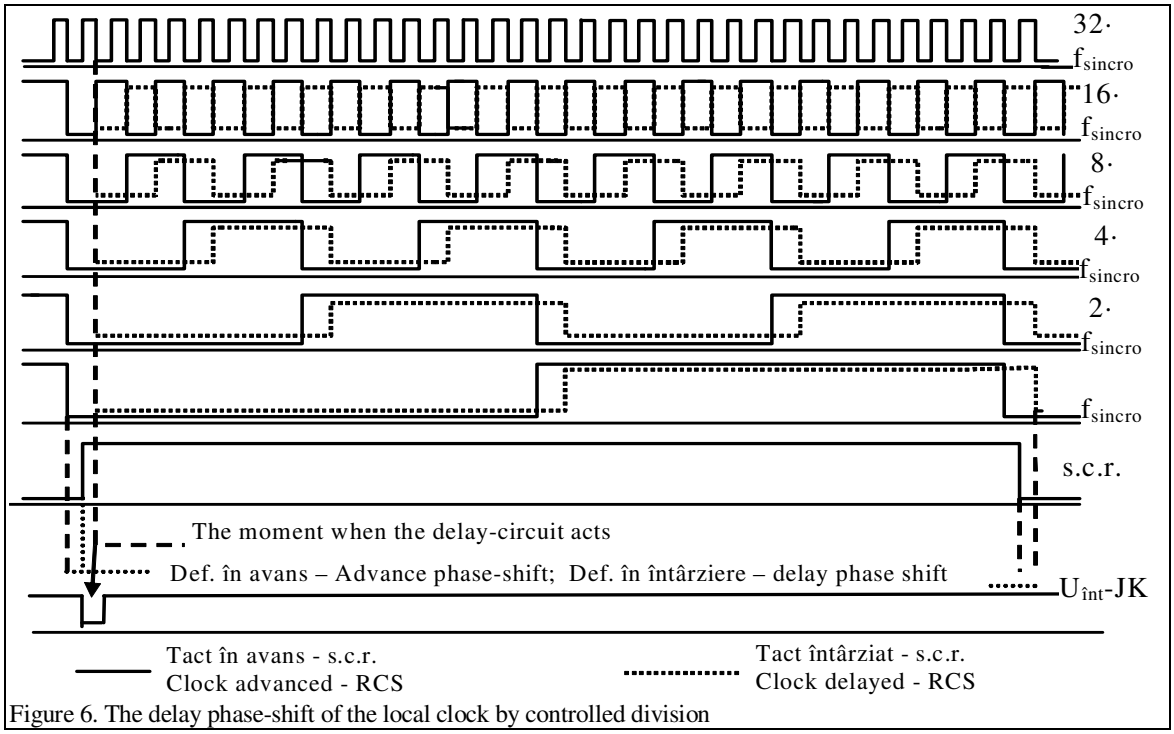


Figure 6. The delay phase-shift of the local clock by controlled division

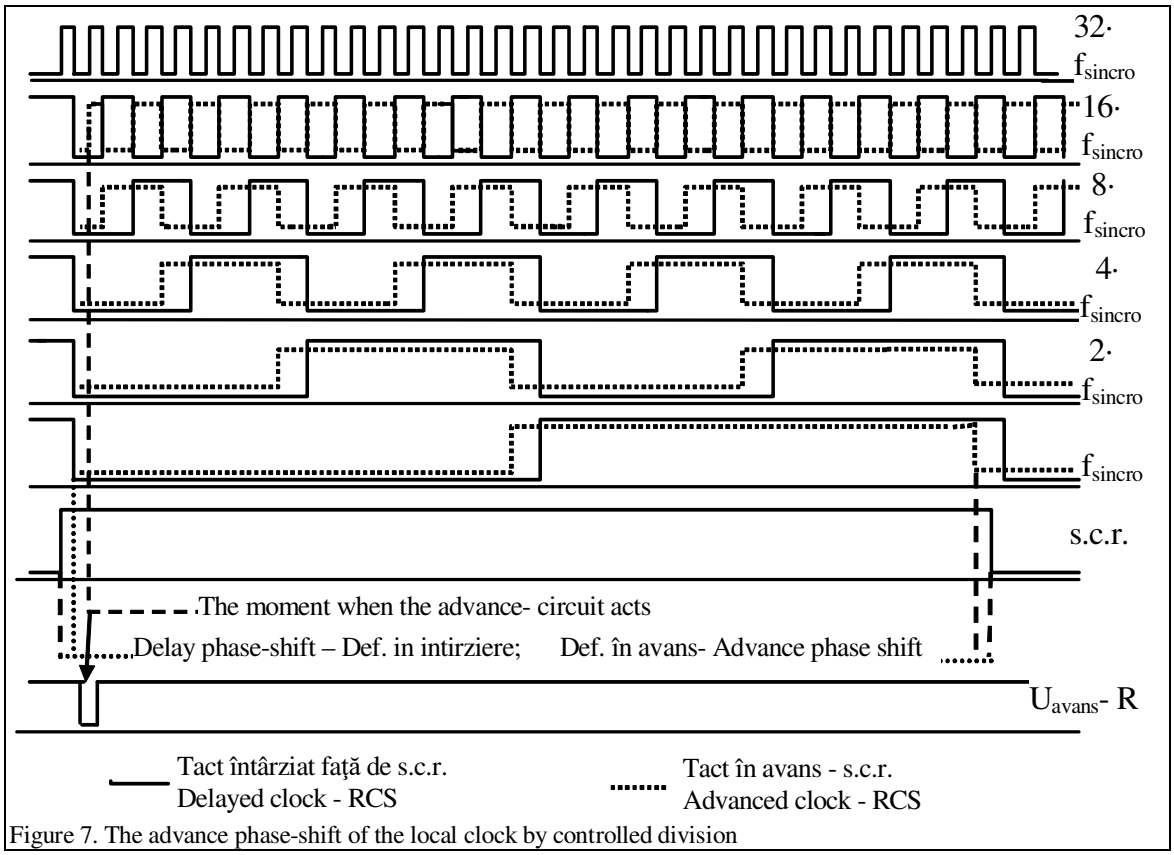


Figure 7. The advance phase-shift of the local clock by controlled division

- Fig. 6 shows the case when the $f_{synchro}$ is advanced, compared to ref. signal, and has to be delayed;
- the CP acts upon the J-K inputs of the first cell of the dividing chain, inhibiting the flip-flop during one active clock transition. So, a transition of its output signal is suppressed, and the transitions of the $f_{synchro}$ signal are delayed with one period of the f_{atack} signal.
- the dashed lines indicate the states of the circuit after the delay circuit takes its action.
- Fig. 7 presents the case when the $f_{synchro}$ is delayed, compared to ref. signal, and has to be advanced
- the CP acts upon the Reset (or Set if another configuration is employed for the divider) input of the first cell of the dividing chain.

- If the Reset is activated when the inverted Q is in "0", an additional transition is inserted in the signal at output of this cell, generating the advance in phase of $f_{synchro}$ with a period of the f_{atack} signal.
- generalizing, an additional transition is inserted in the signal at the output of this cell if we activate the Reset when the inverted Q is in "0", or if we activate the Set when the Q output is in "0".
- the dashed lines indicate the states of the circuit after the advance circuit takes its action.
- *in both cases the advance or delay circuit operates only once during the period of the $f_{synchro}$ signal.*
- the dynamic synchro *can act only if there are transitions in RCS*; otherwise the dynamic synchro *has no phase-reference* (transition of the RCS) and *will either keep the phase-shifting sense established at the last phase comparison performed, or would take no action until a transition of the RCS occurs.*
- this fact shows the necessity of a number, as great as possible, of transitions in the RCS.
- the phase step with which the correction is performed, corresponds to a period of the f_{atack} signal, both for the delay and advance correction.
- expressed in degrees this equals (30) where n is the number of cells of the dividing chain:

$$\Delta\Phi_p = \frac{360°}{\frac{f_{atack}}{f_{sincro}}} = \frac{360°}{N} = \frac{360°}{2^n}; \quad N = 2^n; \tag{5}$$

- the phase amplitude of this step can be modified by changing the number of cells of dividing chain and by changing, correspondingly, the f_{atack} frequency to maintain the value of the frequency of the signal that has to be synchronized, $f_{synchro}$.
-this dynamic synchronization circuit might be regarded as a ADPLL of order 0. Its lock-in range equals its hold-in range and its width is given in (6).a.

- its lock-in time is expressed by (6).b, where t_m denotes the average time interval between two consecutive transitions of the input reference signal (i.e. the duration of a synchronization step), while $\Delta\Phi_{max}$ denotes the maximum initial phase offset that has to be compensated; if no fast synchro is used, $\Delta\Phi_{max} = 180°$.

$$BW_{LK} = BW_{HD} = \left[\frac{f_{atac}}{N+1}; \frac{f_{atac}}{N-1}\right]; a. \quad t_s = \left\lceil \frac{\Delta\Phi_{max}}{\Delta\Phi_p} \right\rceil \cdot t_m; b. \tag{6}$$

- $\Delta\Phi_{max}$ can be reduced by using the fast (coarse) synchronization circuit, see the next paragraph
- this PLL does not reach a static equilibrium, but since the the modulus of the phase offset is smaller than an imposed arbitrarily small value $\Delta\Phi_p$, it can be considered to ensure a *dynamic equilibrium.*
- another version of the dynamic synchro circuit that allows a phase-step $\Delta\Phi_p = 360°/N$, with N a natural number is presented in Annex 1 of this material and will be discussed in the laboratory classes.
- this type of synchronization circuit is also employed by other classes of modems to synchronize the symbol and the bit clocks.

Fast (Coarse) Synchronization

- the block diagram of the fast synchro circuit is shown in figure 8, and its principle of operation is described in figure 9.
- the fast synchro operates in three steps:

- The initial synchronization that is performed only once at the beginning of the reception of a message;
- The disabling of the fast synchro circuit during the reception, so that the dynamic synchro would not be affected;
- The "re-enabling" of the fast synchro circuit at the end of the reception of a message, so that it should be able to act at the beginning of reception of the next message.

- at the beginning of the step, the sensor of the first transition is assumed to be "activated", blocking, by the activation of the Q output of the 16-counter, the generation of the local clock $f_{synchro}$.
- when the first transition of the RCS occurs, the transition sensor gives a pulse which resets the 16-counter, Q ="0", which releases the reset of the dividing chain of the dynamic synchro, thus allowing the generation of the local clock $f_{synchro} = 2f_{bit}$.
- assuming that the divider with N starts to count at the arrival of the first transition of the RCS and that the time interval between two transitions of the RCS is approximately equal with the period of $f_{synchro}$, we see that the first negative transition of the local clock will be coincident with the next transition of the RCS. This indicates the removal of the initial phase-shift.
- But the N-counter (from the dynamic synchro) would actually start counting only at the occurrence of the first negative transition of the $f_{atack} = N \cdot f_{sincro}$, i.e. with a maximum delay of a period of the f_{atack} signal.

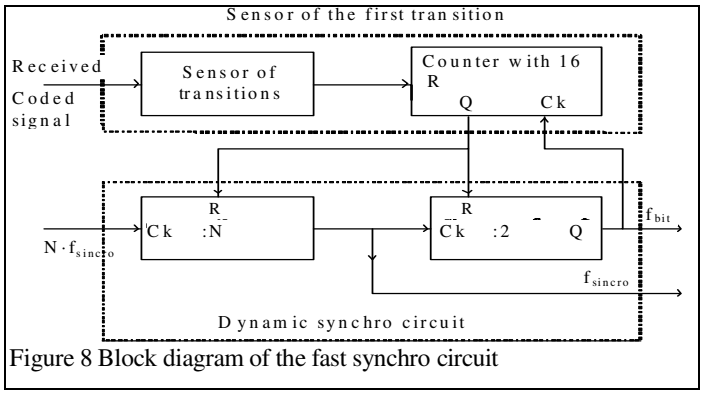


Figure 8 Block diagram of the fast synchro circuit

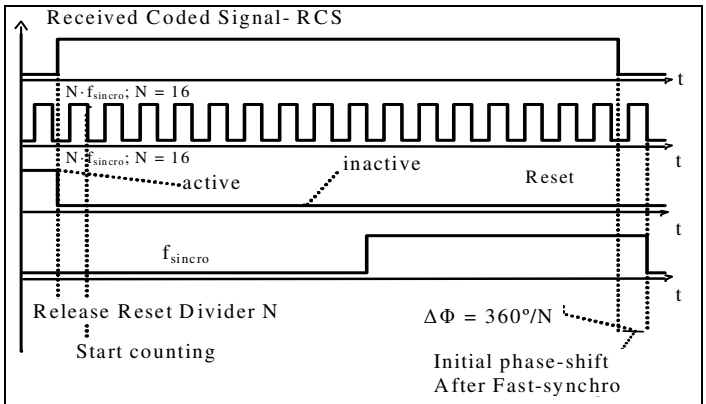


Figure 9. Operating principle of the fast synchro circuit

This fact makes the negative transition of the $f_{synchro}$ to occur with a delay of maximum $\Delta\Phi_{max}$, compared to the arriving moment of the second transition of the RCS, see fig. 19 and (7):

$N=2^n$; →

$\Delta\Phi_{max}=360°\cdot f_{sincro}/(N\cdot f_{sincro})=360°/2^n$; (7)

- (7) holds valid when all the cells of the N-counter are reset by the output of the 16-counter of the fast synchro.

- if the fast synchro opeartes only upon the first *m* stages from the otput of the 2^n-divider, then the maximum initial phase-shift would be:

$$\Delta\Phi_{imax}=360°/2^m; \quad (8)$$

- note that, if m = n, during a period of the $f_{synchro}$ signal, the fast synchro circuit decreases the initial phase to the value of the phase-step of the dynamic synchro, bringing the system in the dynamic equilibrium zone, from where the synchronization is taken over by the dynamic synchro circuit; if m < n, the initial phase-shift is decreased to the value provided by (8)

- once the initial phase shift is removed, the fast synchro circuit should be disabled during the rest of the reception, to allow the dynamic synchro to compensate the dynamic phase shift and the phase-shifts inserted by the transmission channel

- the disabling of the fast synchro circuit during the reception, employs the fact that the maximum time interval between two consecutive transitions of the RCS is 2-bit periods, or 4 periods of the $f_{synchro}$ signal. So, the 16-counter from the fast synchro circuit is reset by the transition sensor, after two bit periods and is it is not able to reach the "1"value, which would disable the N-counter of the dynamic synchro circuit. *This accomplishes the second step of the fast synchro operation.*

- at the end of reception, for 8 bit periods, the 16-counter is no longer reset, there are no transitions since there is no RCS; its output will jump to "1", resetting the N-counter of the dynamic synchro and so the fast synchro circuit is "re-armed" *fulfilling the third step of operation of the fast synchro.*

Resynchronization

- as mentioned earlier, the resynchronization is intended to remove the uncertainty of 180° which might occur between the bit-clock at the transmission end and the bit-clock at the receiving end.
- it is performed only once at the beggining of the transmission, after the action of the fast synchro circuit; this synchronization is required by the Miller code.
- the biphasic code does not require it, due to its differential structure. This property makes it suitable for burst-type transmissions, as the ones in the local computer networks. This goes for the CMI code as well.

Annex 1

Dynamic Synchronization Circuit with $\Delta\Phi_p = 360°/N$

- the synchronization involves the alignment of a locally-generated clock of frequency f_s, to the recovered symbol-clock, employed as phase reference in a synchronization system, performing the two steps: initial synchronization and dynamic synchronization.
- some applications require specific values of the phase-step of the dynamic synchronization circuit.
- as an example we consider the demodulation of the PSK or A+PSK signals which impose two contradictory requirements on the dynamic synchronization:
  - it should ensure the highest possible accuracy, which would involve a small value of the phase-step $\Delta\Phi_p$
  - it should have a small time response, or a high speed with which the circuit follows the phase of the received signal, in order to be efficient in acse of phase-hits or clock slips; it would require a greater value of the phase-step.
- in many cases the values of the phase step provided by the dynamic synchro presented in the BB lectures, i.e. $\Delta\Phi_p=360°/2^n$, do no satisfy the above requirements
- therefore the phase step should take values with a finer granularity, such as $\Delta\Phi_p=360°/N$, with N any natural number.
- a dynamic synchro circuit, built with an arithmetic-adder and a shift-register, which ensures such a phase step is presented below
- the particular case presented below ensures a phase step given by (A3.1) using $f_{atack} = 1344 f_{local}$ and performing frequency division by 1343, to advance the local clock, and to 1345, to delay it:

$$\Delta\Phi_p=360°/1344\approx 0.268°; \qquad (9)$$

This variant is shown in figure A.1. In this circuit f_{local} is considered to be a symbol clock f_s; it also indicates how a bit clock $f_{bit} = 3f_s$ is also synchronized.

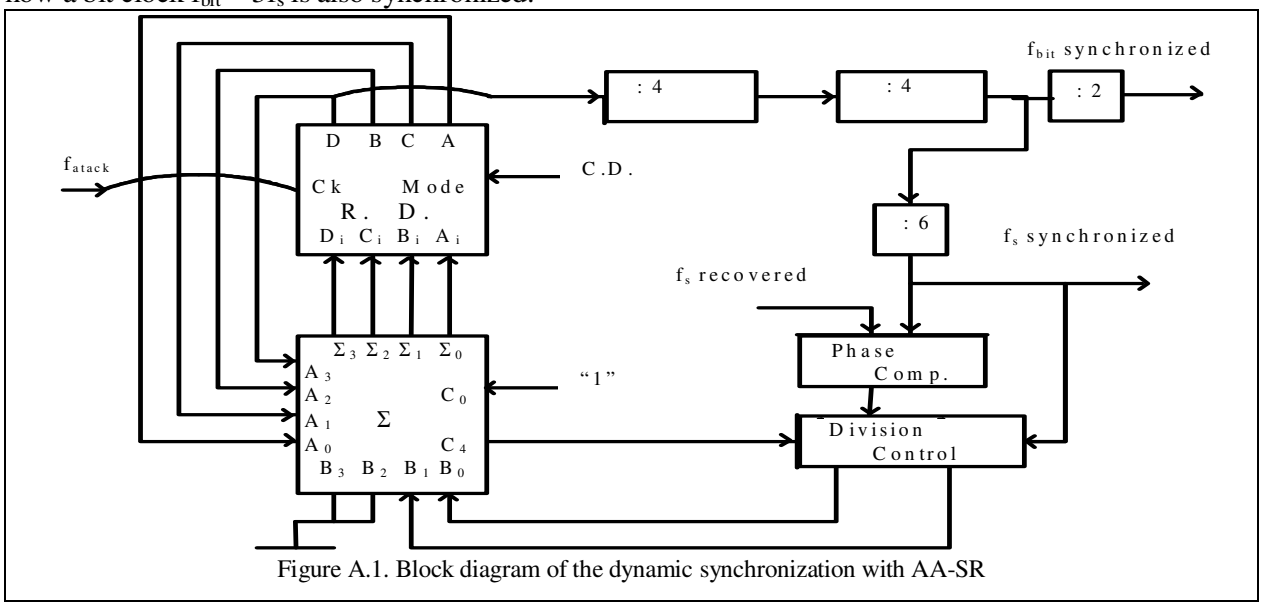


Figure A.1. Block diagram of the dynamic synchronization with AA-SR

HOMEWORK: - Describe the operating principle of the circuit above.

Hint: if the B_i = "0" the adder+R.D. circuit divides by 16. The $f_{atack} = 14 \cdot 6 \cdot 16 \cdot f_s = 1344 \cdot f_s = N_0 \cdot f_s$, but the method employs the division of this frequency by $N_1 = 15+14 \cdot 95 = 1345$, or by $N_2 = 13+14 \cdot 95 = 1343$, to accomplish the delay or advance of the local clock.

Compute the phase-step for advancing and for delaying the synchronized clock, and show that it is approximately equal to $\Delta\Phi_p=360°/N$.