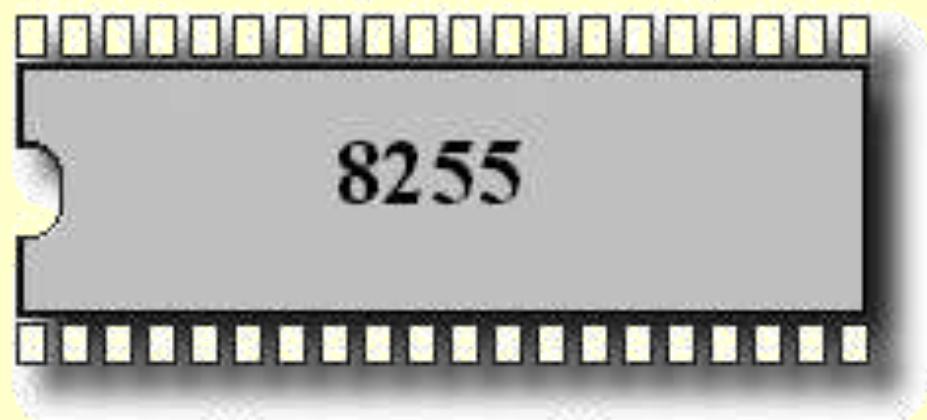


C13. INTERFATA PARALELA PROGRAMABILA (PPI) I8255A (PIO)

- 1. Descriere PIO**
- 2. Arhitectura PIO**
- 3. Programare PIO**
- 4. PIO in PC**
- 5. Aplicatii**



<http://www.advancedmsinc.com/iocards/8255.htm>
<http://www.eisti.fr/~ga/phy/iitr/ii05/tr.pdf>

1. Descriere PIO

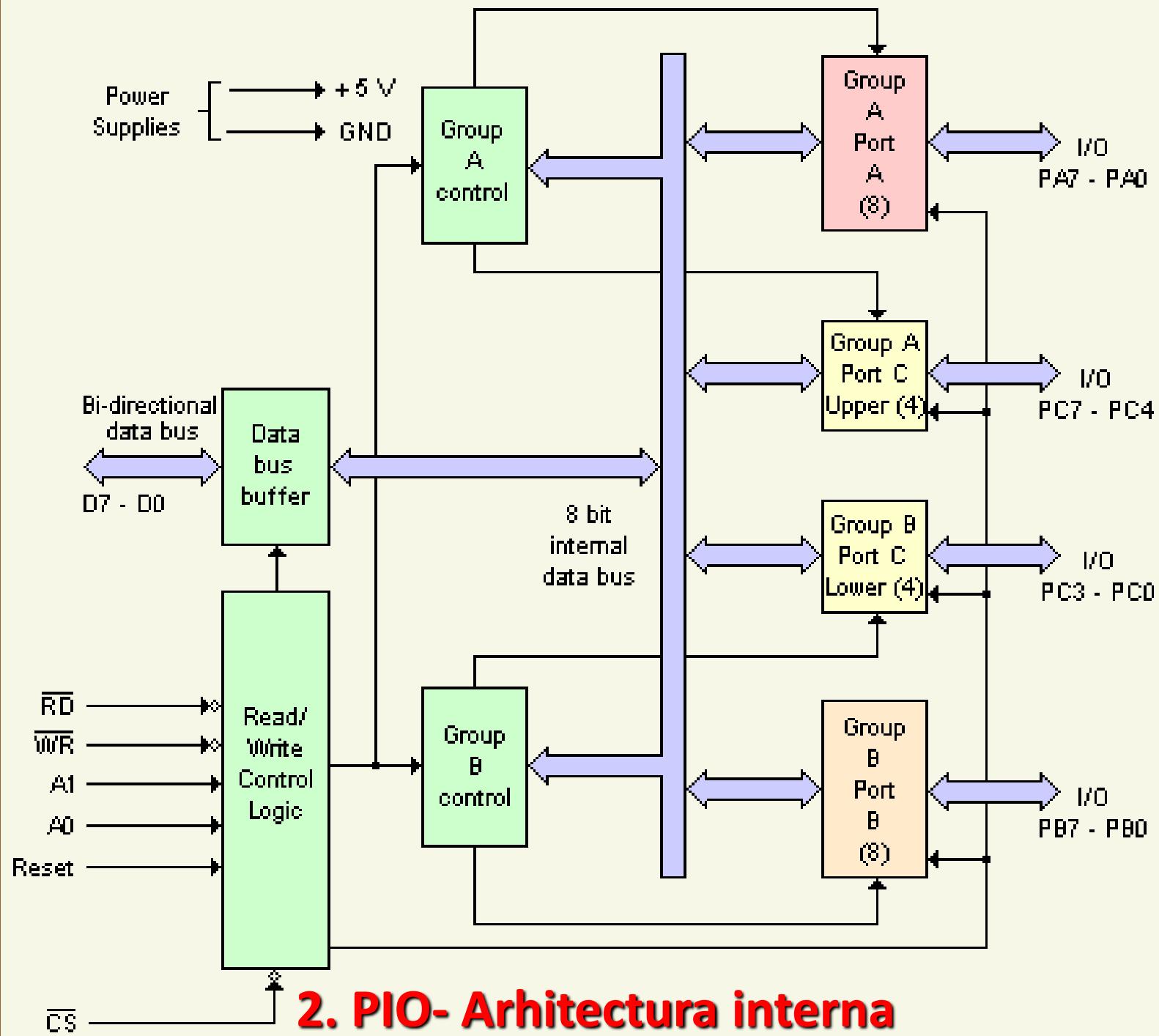
- I8255A implementeaza o interfata paralela programabila pentru operatii I/O
- I8255A are 24 I/O care se pot programa in 2 grupuri
- PIO opereaza in urmatoarele 3 moduri:

Mod 0: Basic Input/Output — Port A, port B, port C (H&L) pot fi configurate independent ca I/O pentru citire sau pastrare date (iesirile sunt pe registre intrarile nu)

Mod 1: Strobed Input/Output — Port A si port B

Pot fi independent configurate ca busuri de intrare sau iesire strobate
Semnalele de la portul C sunt rezervate ptr. semnale de control (handshake)

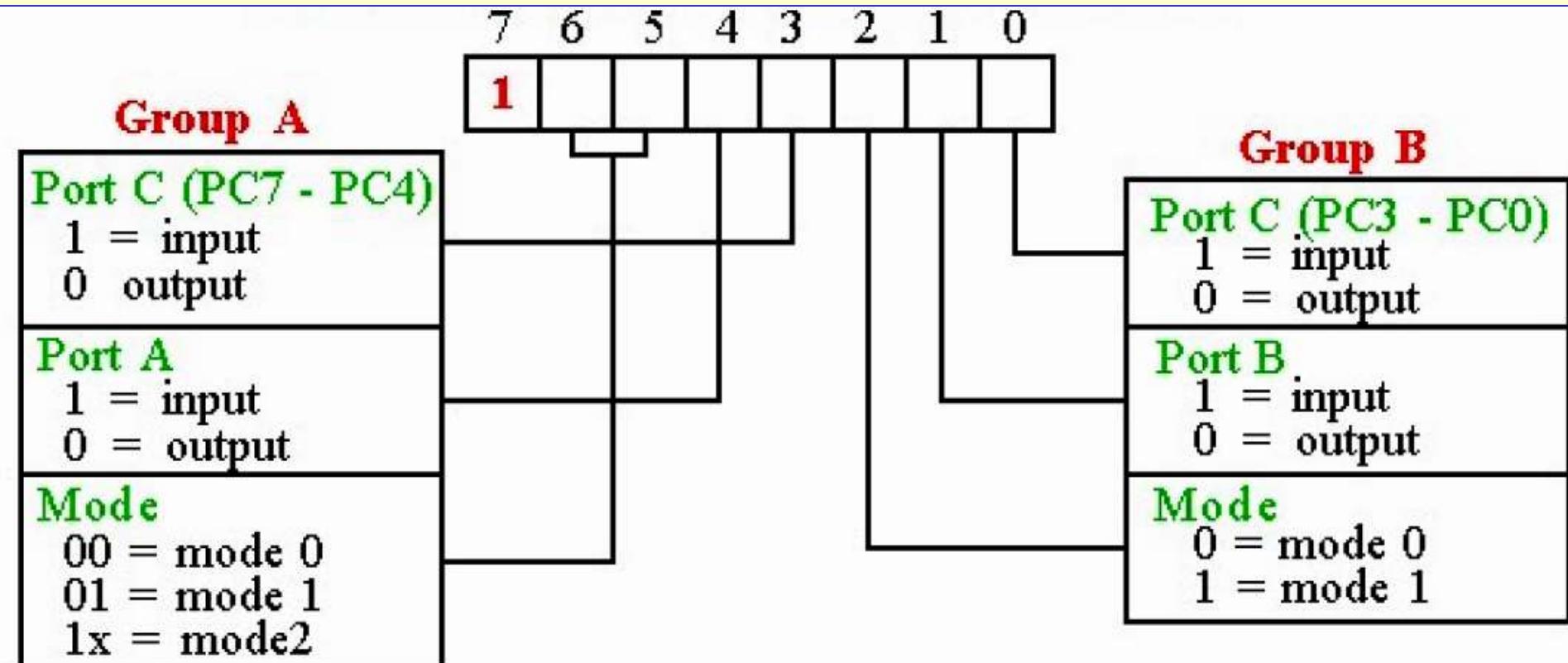
Mod 2: Bidirectional Bus — Port A poate fi configurat ca bus bidirectional, port C furnizeaza semnalele de control; portul B poate lucra in mod 0 sau mod 1.



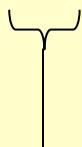
Adrese		Registre
A1	A0	Registrul/Port
0	0	Port A data (all modes)
0	1	Port B data (all modes)
1	0	Port C data (mode 0) and status (modes 1 and 2)
1	1	Control register mode definition and port C bit set/reset

- **adresele PIO rezervate in PC: 60h-63h ;**
- **La PC-AT PIO inlocuit cu microcontroler , adr. 60h-64h**

3. Programare PIO



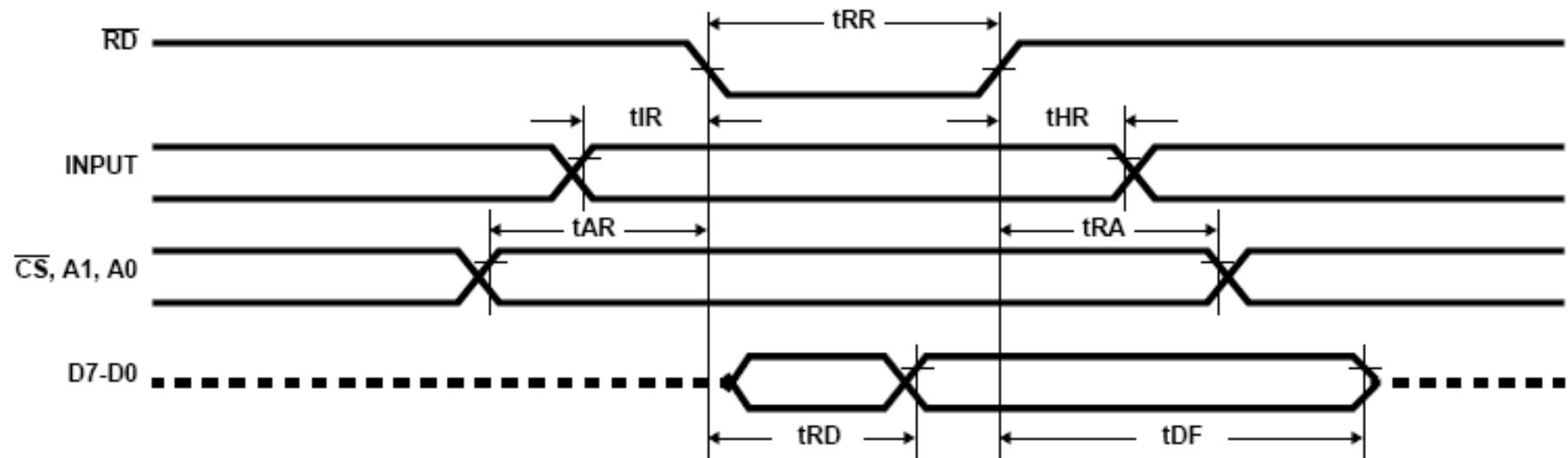
D₇ D₆ D₅ D₄ D₃ D₂ D₁ D₀



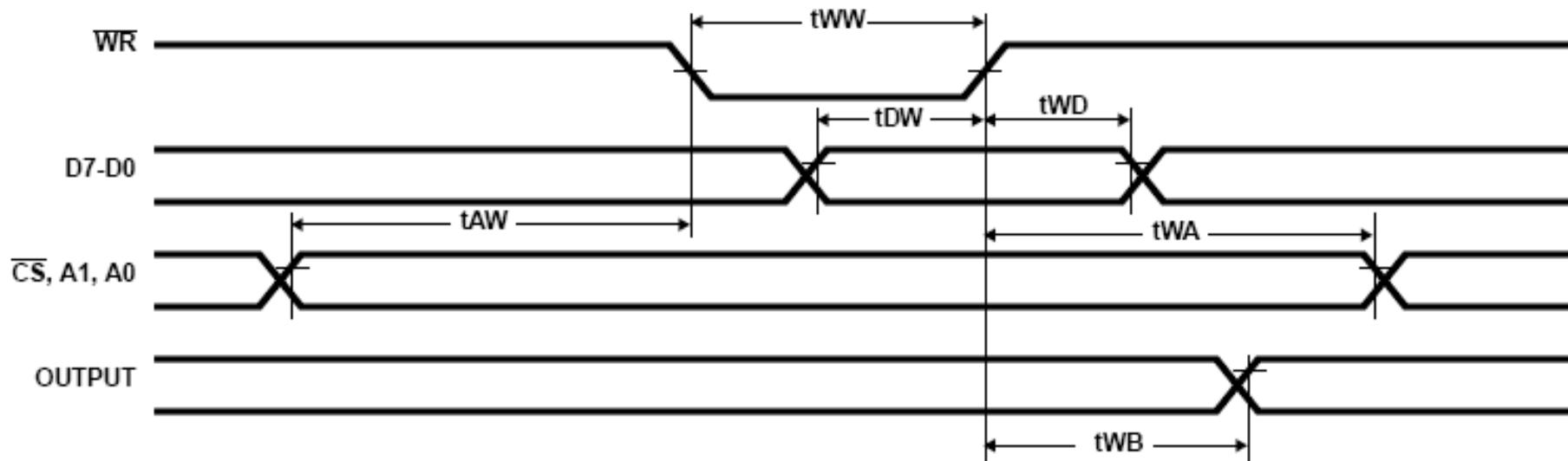
1 = I / O Mode
0 = BSR Mode

Mode 0: Basic Input/Output (D7=1, D6=D5=D2=0)

Mode 0 (Basic Input)



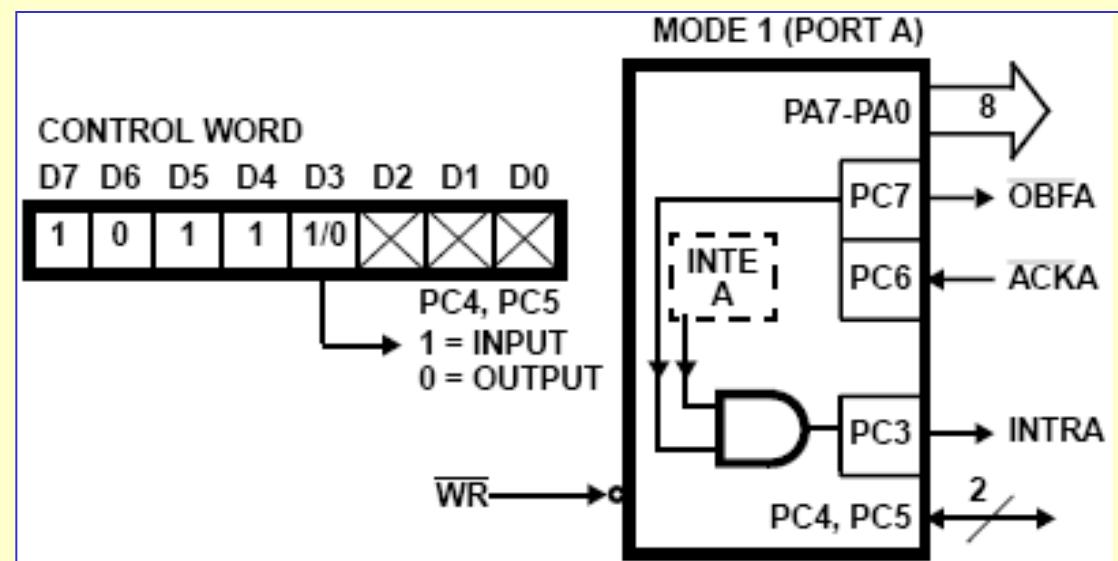
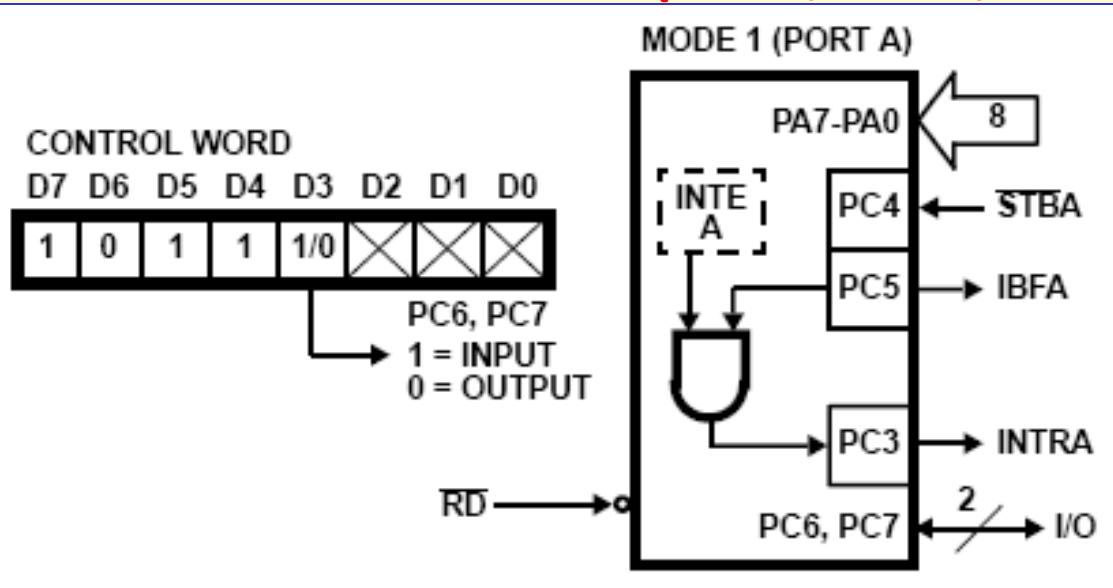
Mode 0 (Basic Output)



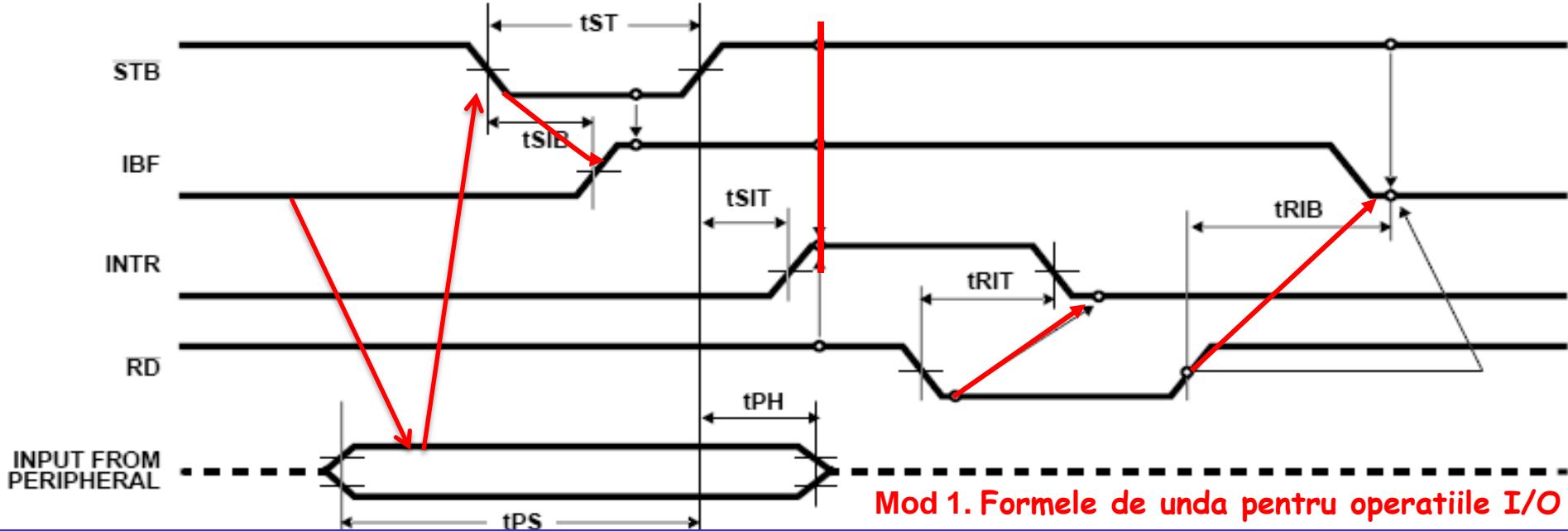
Mode 0. Formele de undă pentru operațiile de I/O

Mode 1: Strobed Input/Output

(D7=1, D6=0, D5=D2=1)



Configurarea porturilor A,C ca IN/OUT



Input Control Signal Definition

STB (Strobe Input)

A “low” on this input loads data into the input latch

IBF (Input Buffer Full F/F)

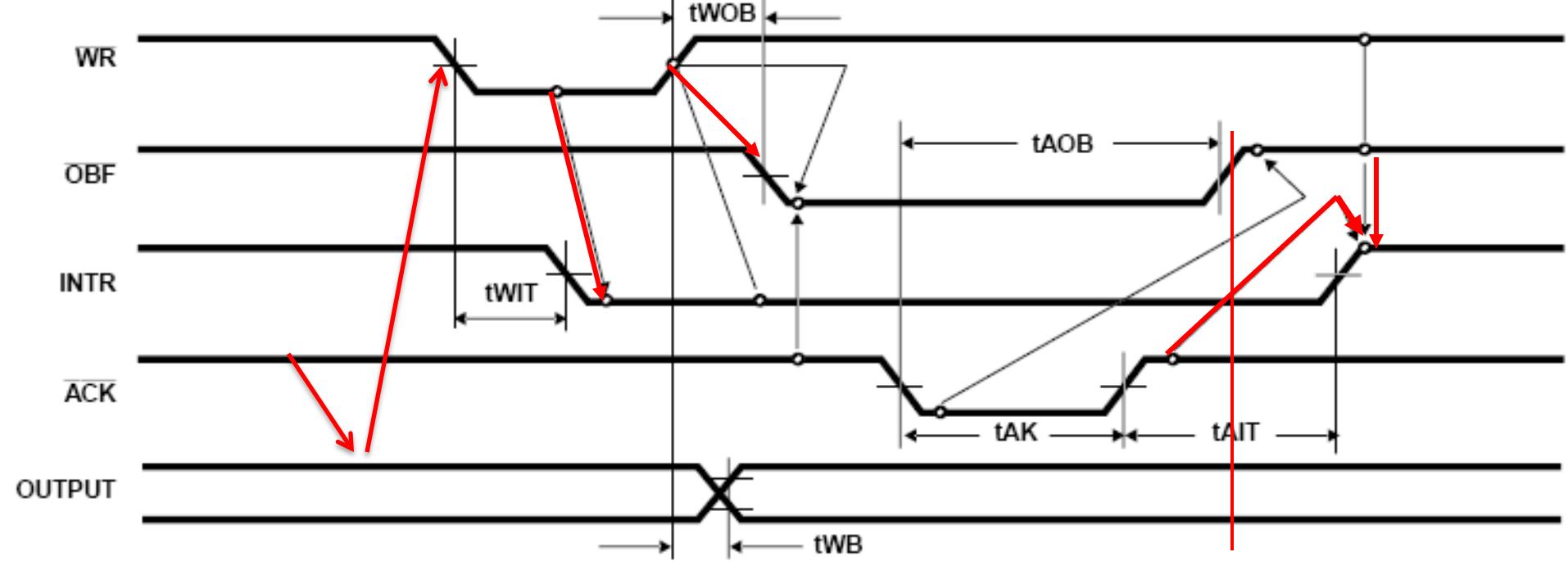
A “high” on this output indicates that the data has been loaded into the input latch: in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of RD. This procedure allows an input device to request service from the CPU by simply strobbing its data into the port.

INTR (Interrupt Request)

A “high” on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition: STB is a “one”, IBF is a “one” and INTE is a “one”. It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobbing its data into the port.

INTE A Controlled by bit set/reset of PC4.

INTE B Controlled by bit set/reset of PC2.



Output Control Signal Definition

-OBF – (Output Buffer Full F/F) The OBF output will go “low” to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the part at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

-ACK – (Acknowledge Input). A “low” on this input informs the 8255A that the data from Port A /Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data.

INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a “one”, OBF is a “one” and INTE is a “one”. It is reset by the falling edge of WR.

INTE A Controlled by Bit Set/Reset of PC6.

INTE B Controlled by Bit Set/Reset of PC2.

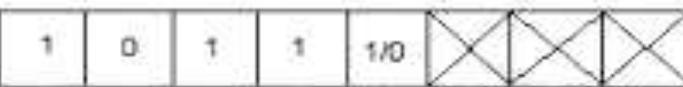
Port C with Port A & Port B Both Configured as Mode 1

Bit	Mode 1 Input	Mode 1 Output	Description
PC0	intrb	intrb	Always output.
PC1	ibfb	-obfb	Always output.
PC2	-stbb	-ackb	Always input.
PC3	intra	intra	Always output.
PC4	-stba	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC5	ibfa	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC6	I/O	-acka	I/O direction configured by bit 3 of the control register in “mode 1 input.”
PC7	I/O	-obfa	I/O direction configured by bit 3 of the control register in “mode 1 input.”

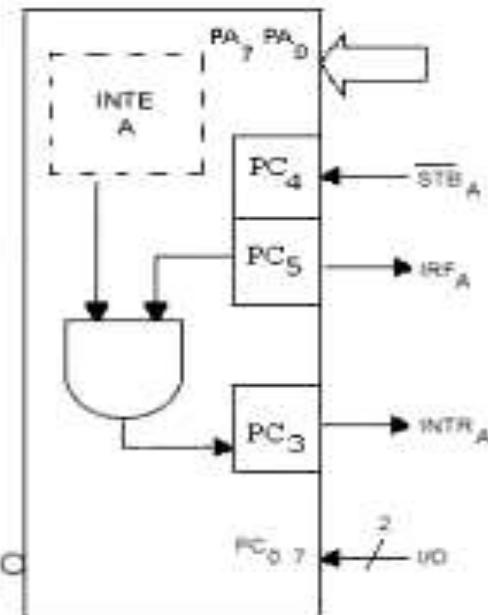
MODE 1 (PORT A)

CONTROL WORD

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------



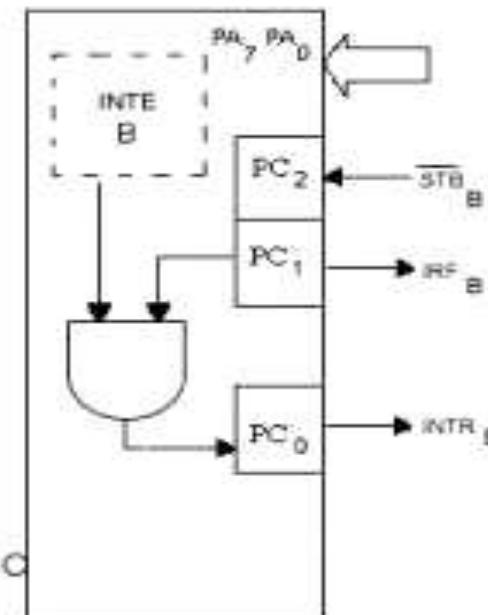
PC_{0:7}
1 = INPUT
2 = OUTPUT

 \overline{RD} $\rightarrow C$ 

MODE 1 (PORT B)

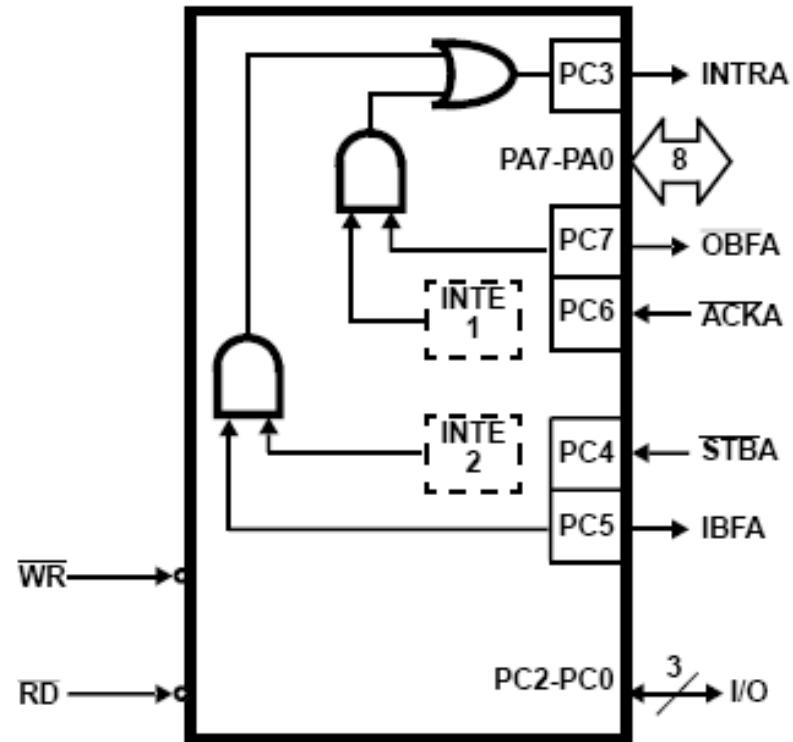
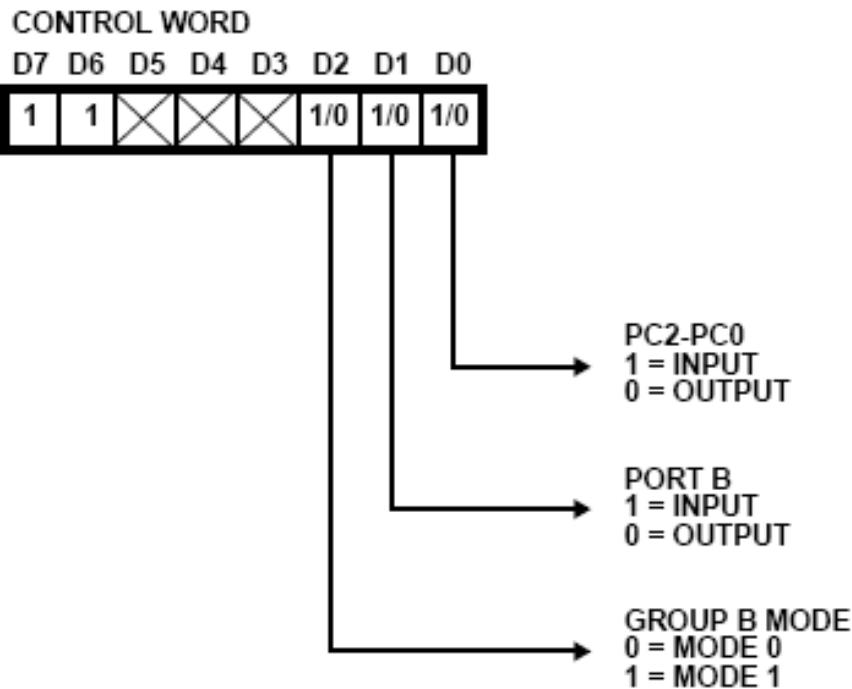
CONTROL WORD

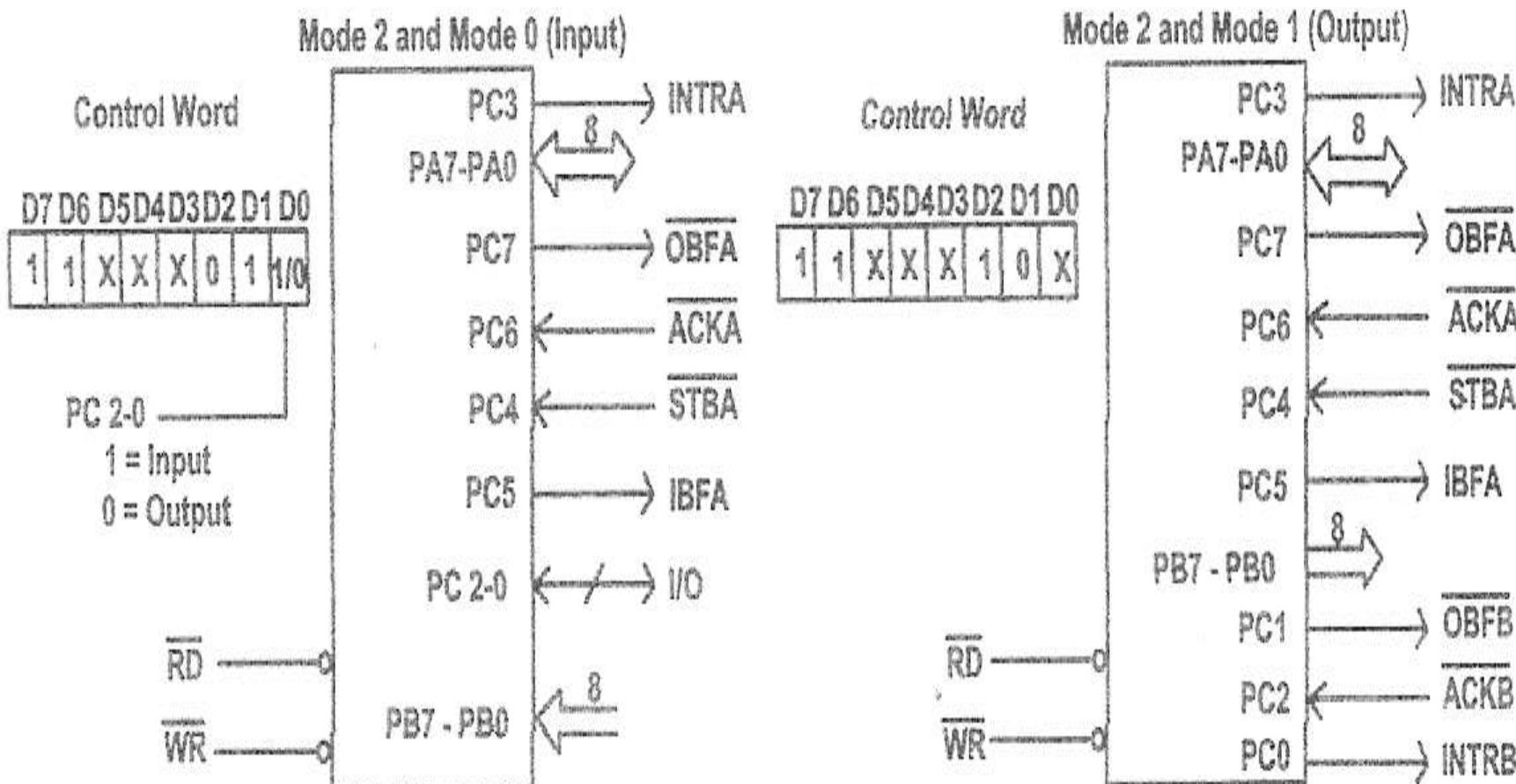
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

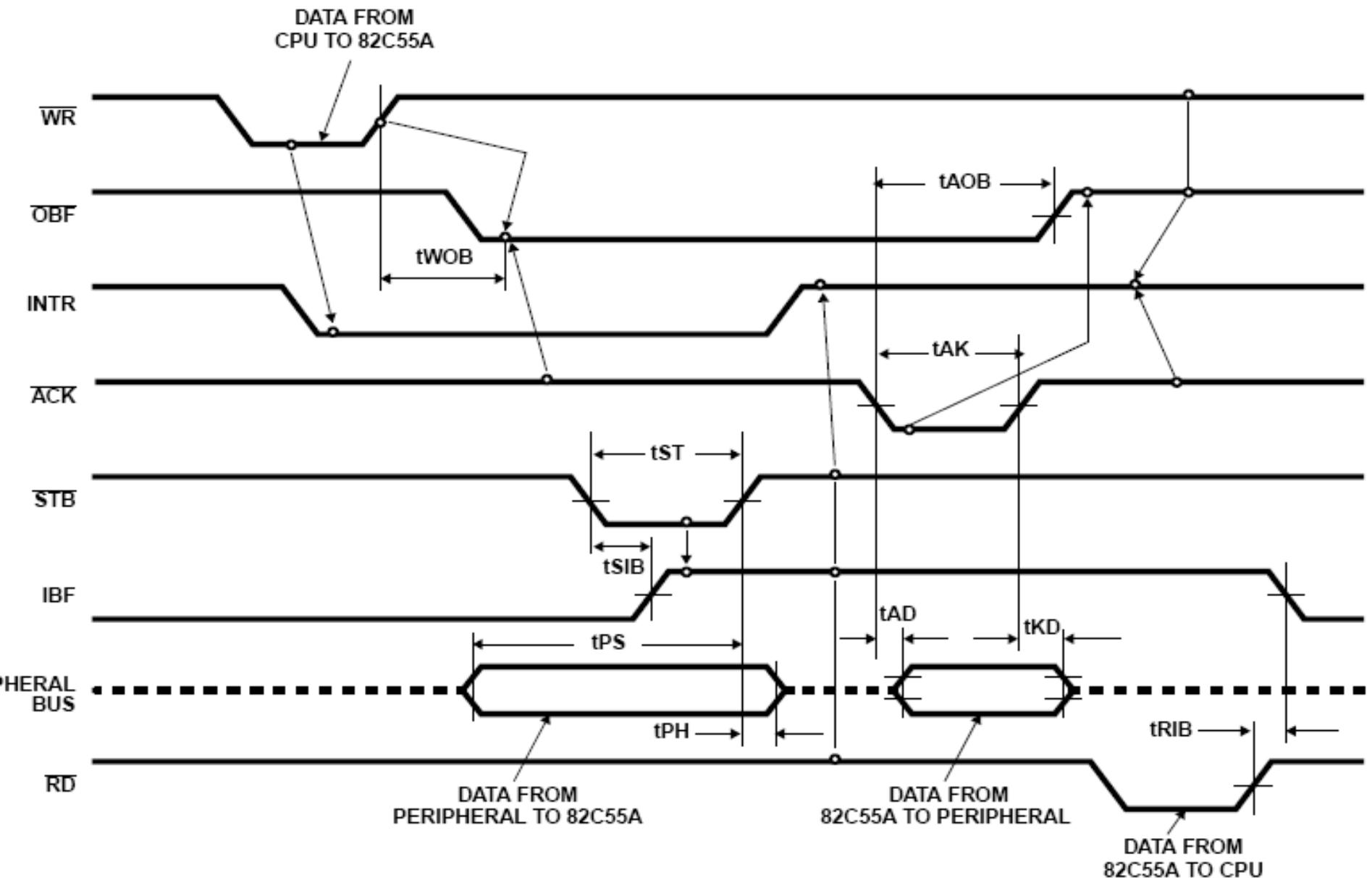
 \overline{RD} $\rightarrow C$ 

Mode 2: Strobed Bidirectional Bus

(D7=1, D6=1, D5=D2=XX)



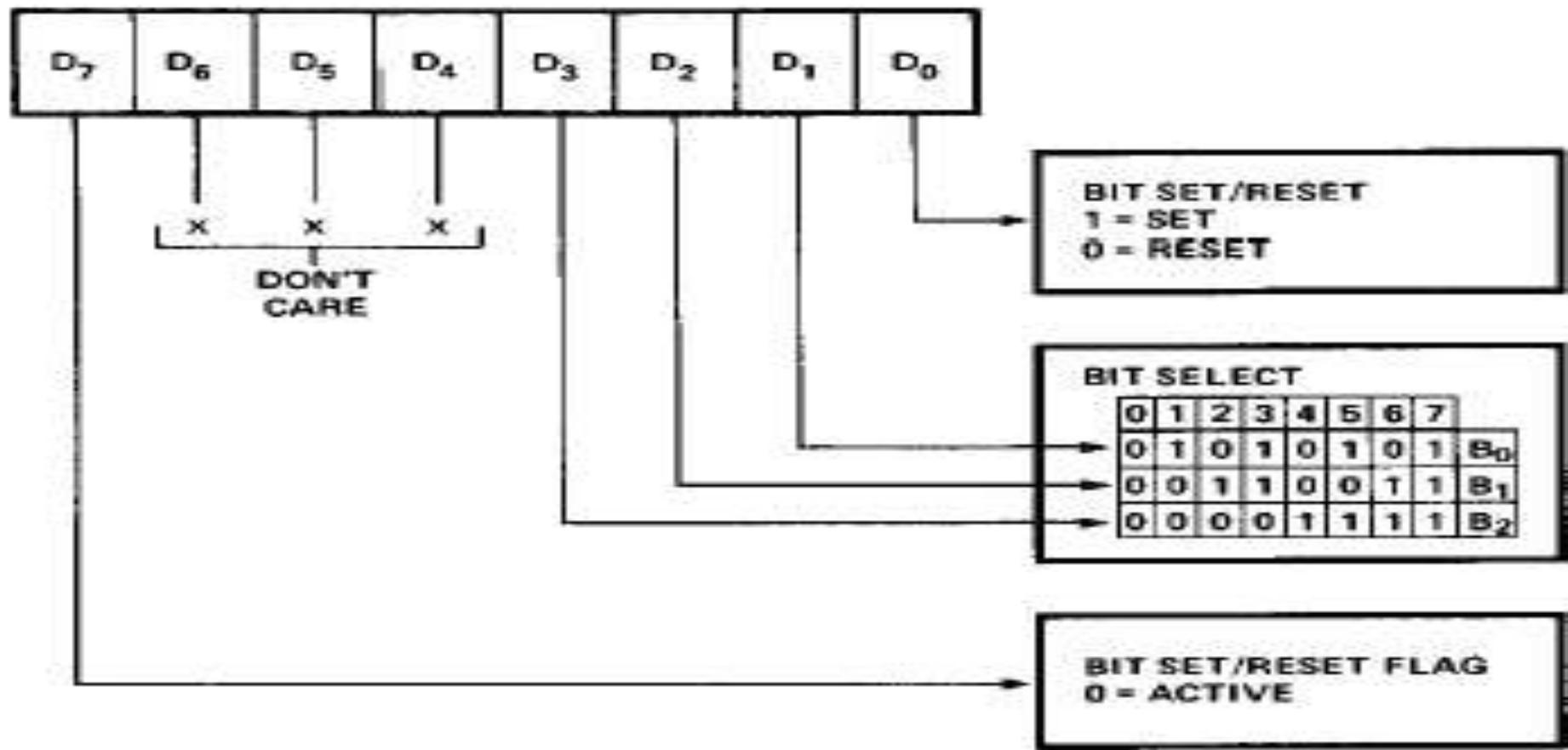




Any sequence where \overline{WR} occurs before \overline{ACK} and \overline{STB} occurs before RD is permissible. ($INTR = IBF \cdot MASK \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot MASK \cdot \overline{ACK} \cdot \overline{WR}$)

Mod 2. Formele de undă pentru operațiile I/O

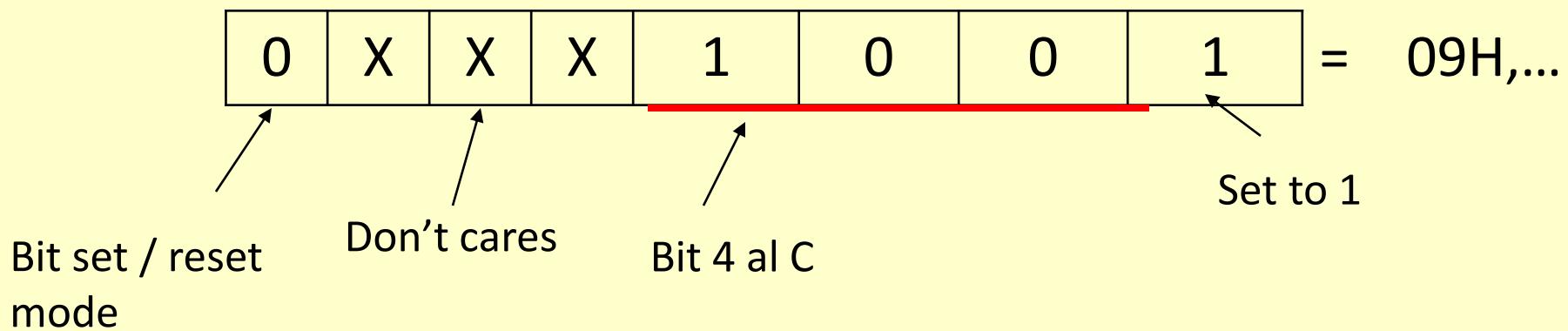
CONTROL WORD



C port bits set/reset

1 = I/O Mode
0 = BSR Mode

Ex. 1: Setez bitul 4 al Portului C la 1 (Adr port A 7Ch)



MOV AL, 09H

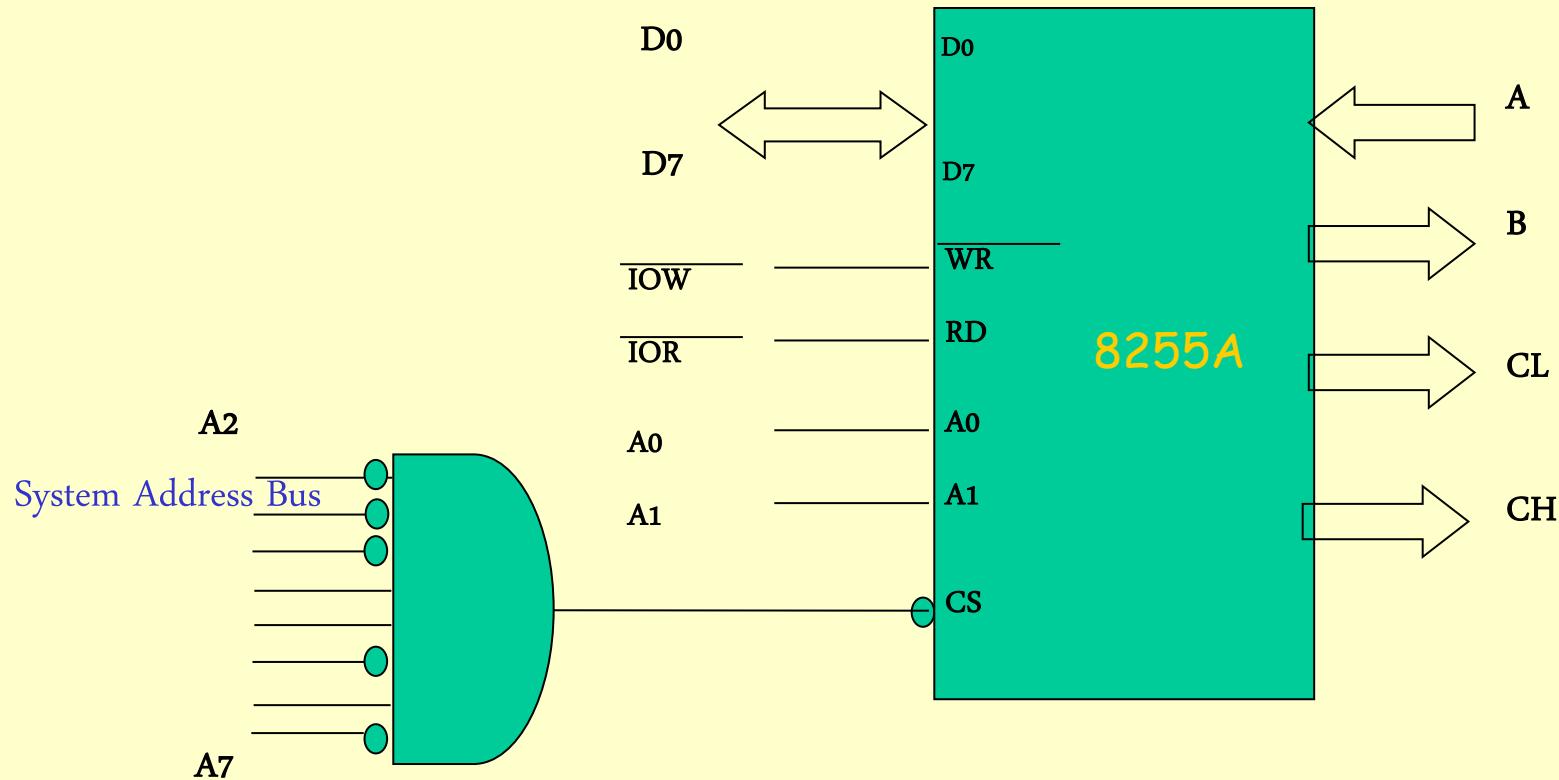
OUT 7FH, AL

8255 Modurile de lucru -rezumat

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA ₀	IN	OUT	IN	OUT	↔	
PA ₁	IN	OUT	IN	OUT	↔	
PA ₂	IN	OUT	IN	OUT	↔	
PA ₃	IN	OUT	IN	OUT	↔	
PA ₄	IN	OUT	IN	OUT	↔	
PA ₅	IN	OUT	IN	OUT	↔	
PA ₆	IN	OUT	IN	OUT	↔	
PA ₇	IN	OUT	IN	OUT	↔	
PB ₀	IN	OUT	IN	OUT	—	
PB ₁	IN	OUT	IN	OUT	—	
PB ₂	IN	OUT	IN	OUT	—	
PB ₃	IN	OUT	IN	OUT	—	
PB ₄	IN	OUT	IN	OUT	—	
PB ₅	IN	OUT	IN	OUT	—	
PB ₆	IN	OUT	IN	OUT	—	
PB ₇	IN	OUT	IN	OUT	—	
PC ₀	IN	OUT	INTR _B	INTR _B	I/O	
PC ₁	IN	OUT	IBF _B	OBF _B	I/O	
PC ₂	IN	OUT	STB _B	ACK _B	I/O	
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A	
PC ₄	IN	OUT	STB _A	I/O	STB _A	
PC ₅	IN	OUT	IBF _A	I/O	IBF _A	
PC ₆	IN	OUT	I/O	ACK _A	ACK _A	
PC ₇	IN	OUT	I/O	OBF _A	OBF _A	

4. Aplicatii cu PIO.

Implementarea porturilor pe 16 biti

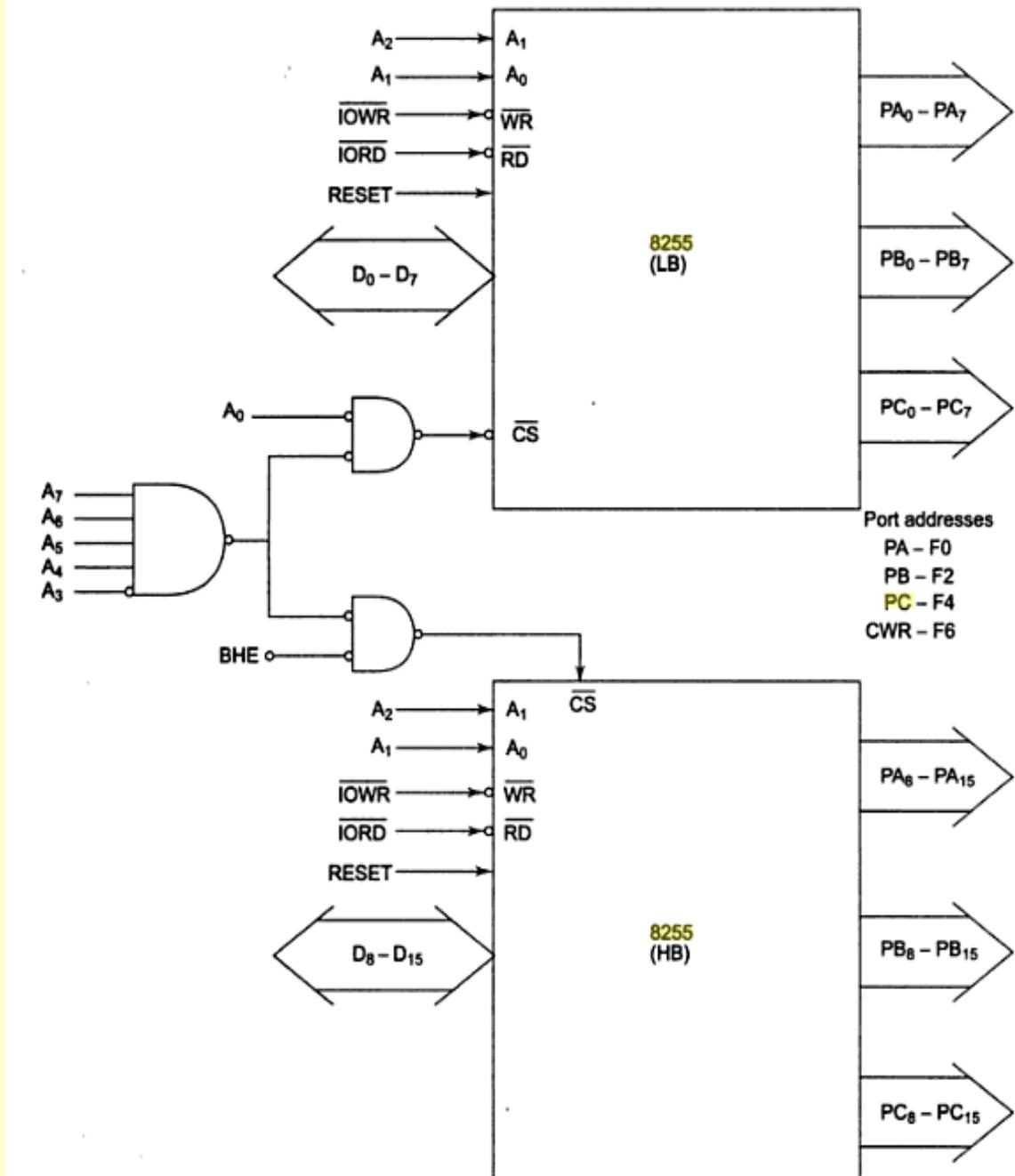


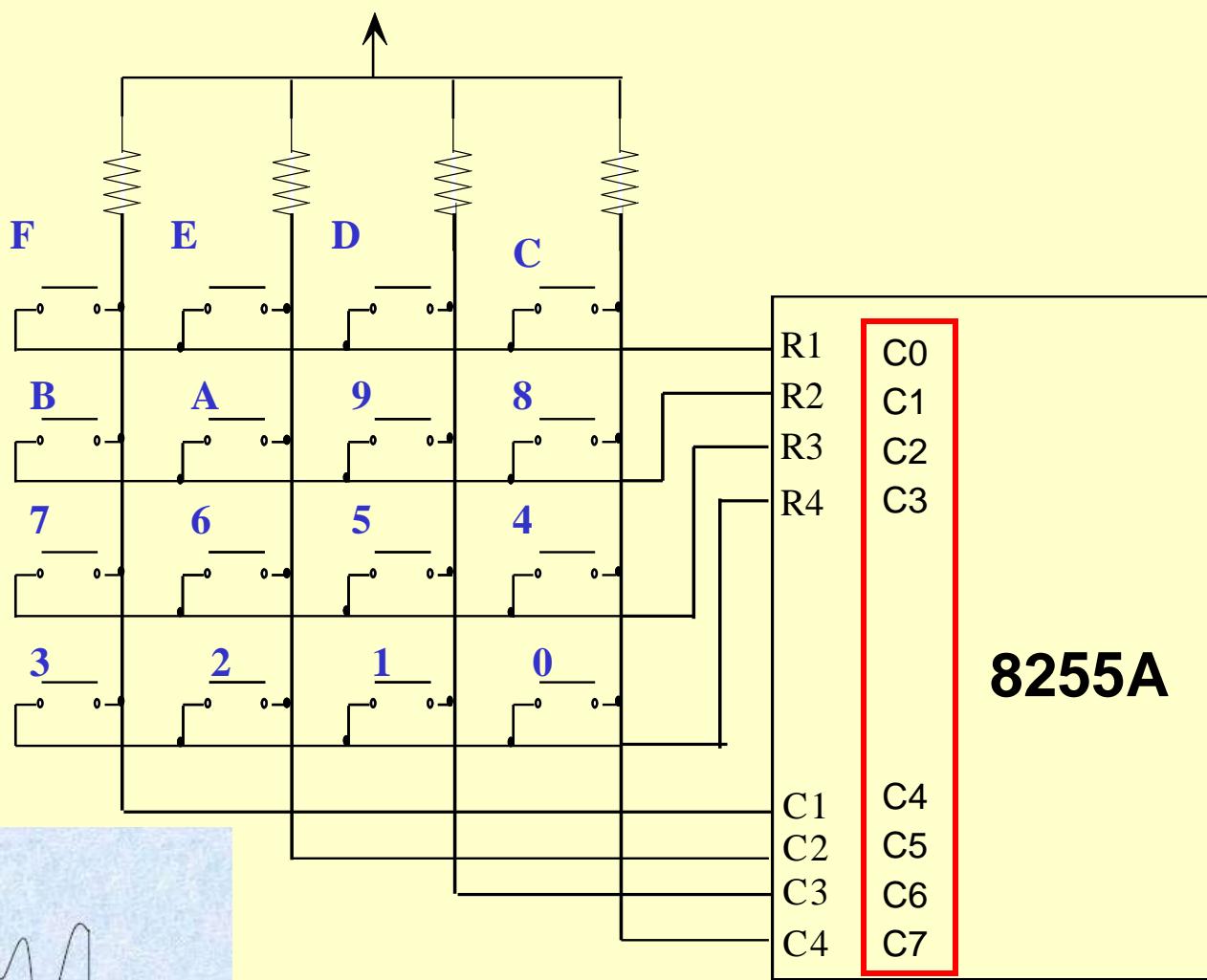
Problema.

Interfatați un port pe 16-bit cu 8255 ports la 8086.

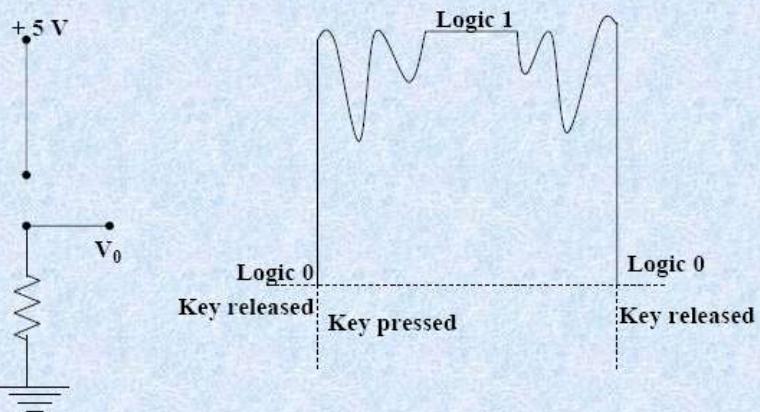
Adresa portului A este F0h.

Solutie. Pentru implementarea unui port de 16biti se folosesc 2x8255. Unul pe partea L a DBUS (D0-D7) , iar celalalt pe partea H a DBUS (D8-D15). Fig. urmatoare.





Example



Tema 1. Scrieti o aplicatie care furnizeaza in AL codul hexa al tastei apasate.

KEYBOARD

ZERO TO ALL ROWS

READ COLUMNS

ALL KEYS OPEN ?

READ COLUMNS

KEY PRESSED ?

Yes

No

D
E
T
E
C
T

WAIT 20ms

READ COLUMNS

NO
KEY
PRESSED
?

FLOW CHART

D
E
B
O
U
N
C
E

OUTPUT ZERO TO ONE ROW

READ COLUMNS

KEY FOUND ?

NO

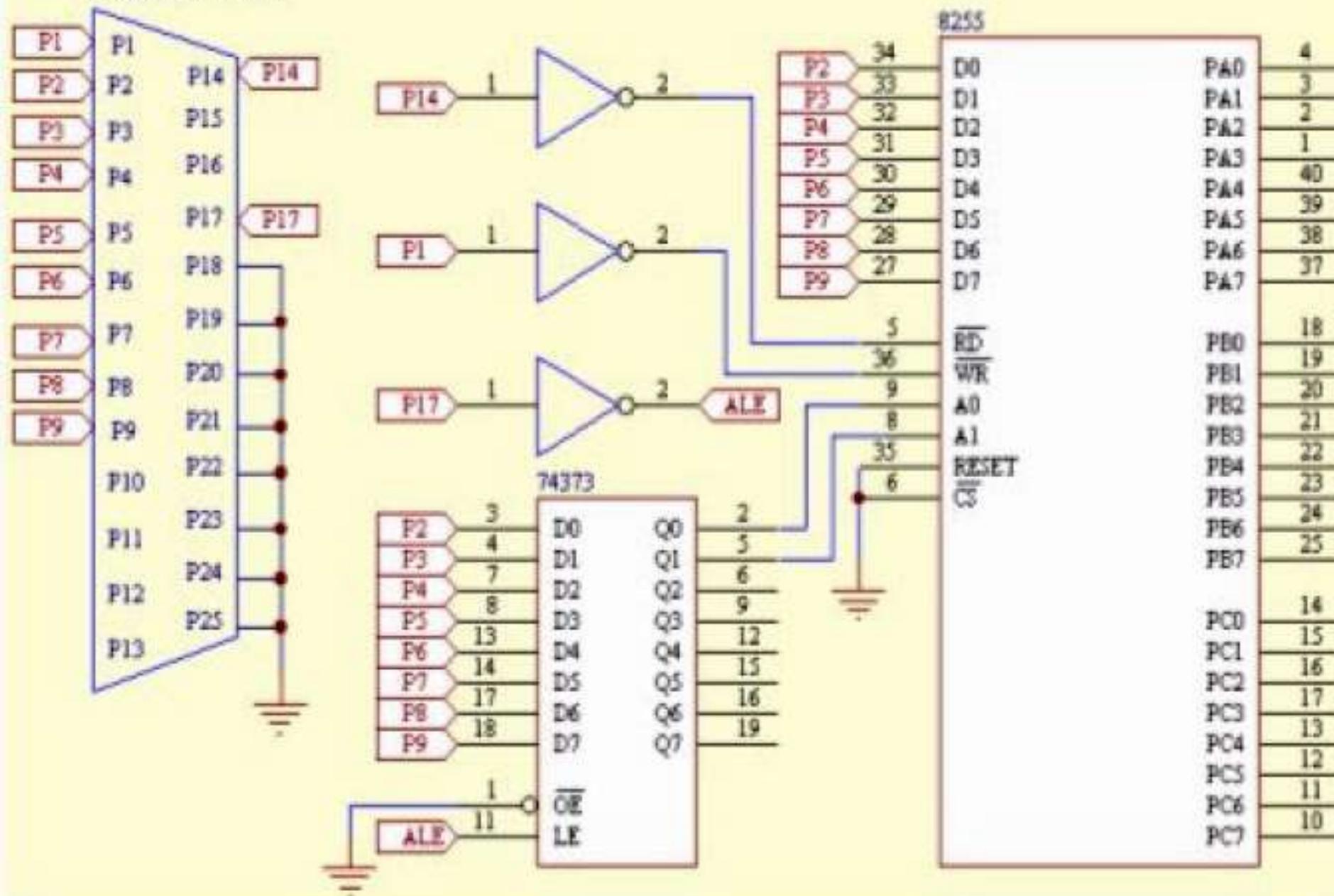
YES

CONVERT TO HEX

RETURN

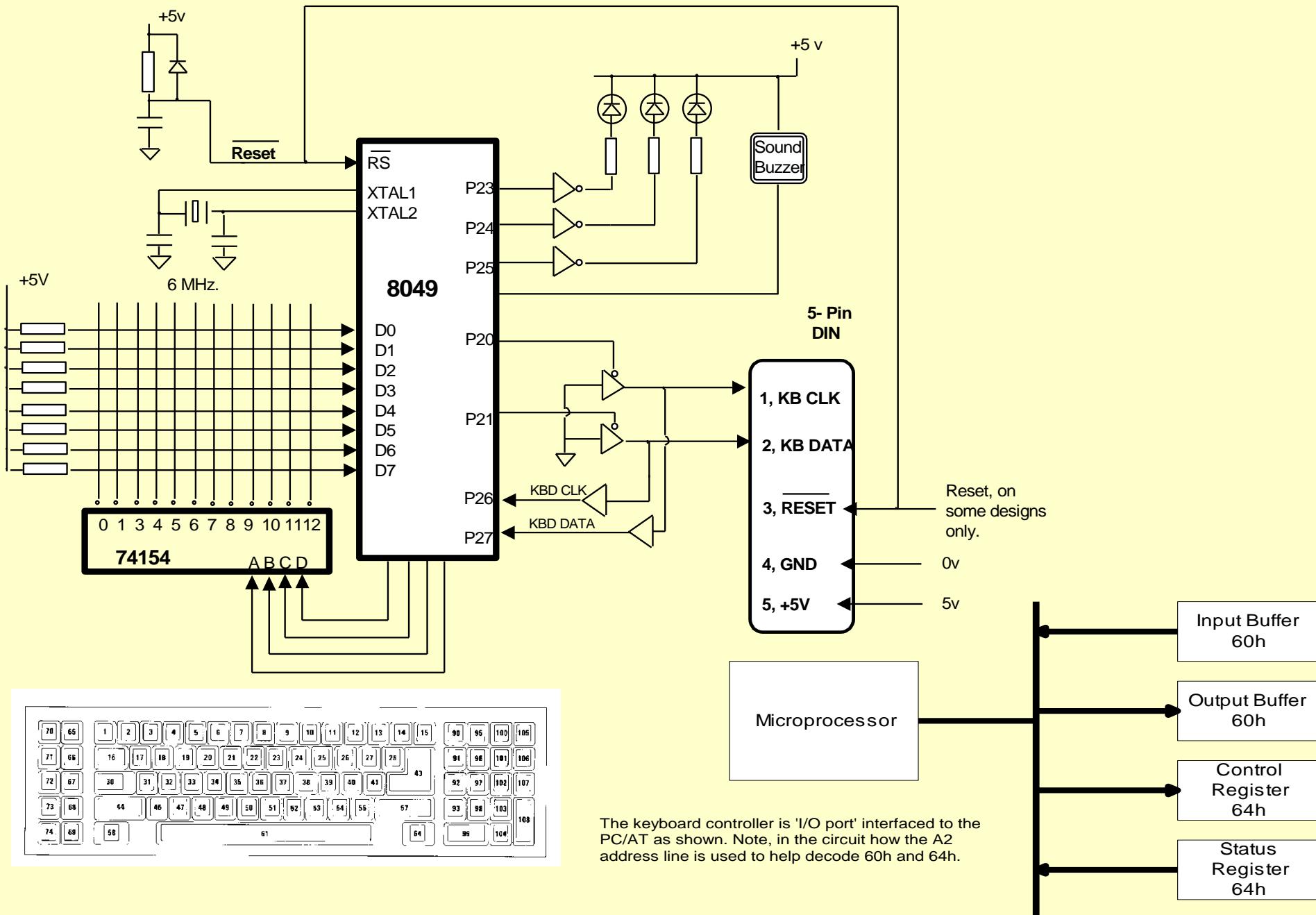
E
N
C
O
D
E

Parallel Port



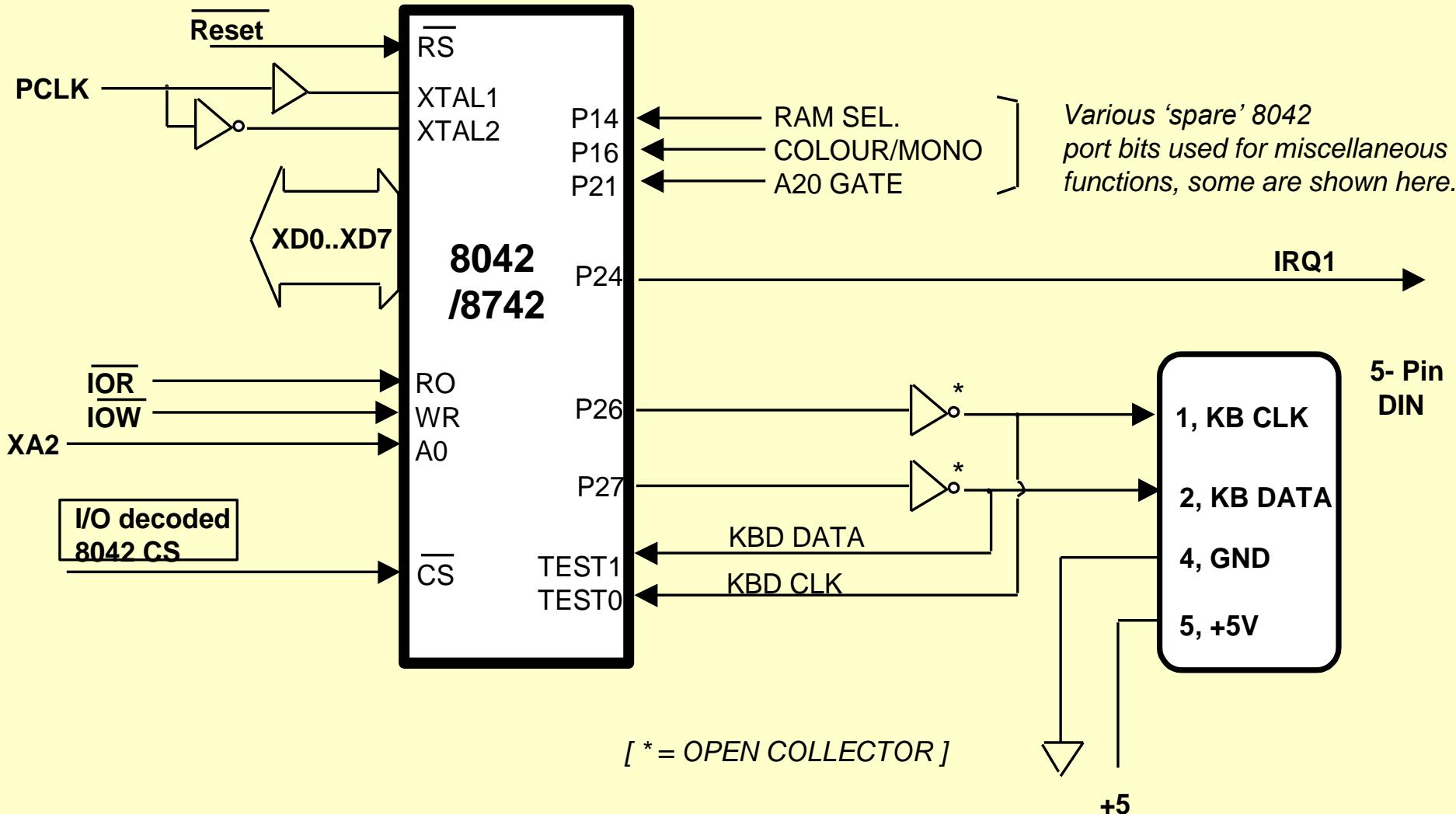
Tema2. Analizati schema si stabiliti functionarea ei.

The Keyboard Circuit



The keyboard controller is 'I/O port' interfaced to the PC/AT as shown. Note, in the circuit how the A2 address line is used to help decode 60h and 64h.

The Key Board Controller



DISTR, DOSSTR = Data Input and Data Output Strobes.