MICROPROCESSOR SYSTEMS (µP 2)

GOAL :

PC Hardware Study:

- 8086, Pentium
- Memory (Main, Cache)
- Programmable Interfaces (Timer, PIC, DMAC, PIO)
(architecture, programming, applications)
- SPP/EPP/ECP, COM, USB, I2C/SPI
- Buses (ISA, PCI)

REFERENCES

-Lupu, E. , Mesaroş, A. , Suciu, A.F. MICROPROCESSORS. Architectures and Applications Ed. RISOPRINT Cluj-Napoca 2002

-Lupu, E. SISTEME CU MICROPROCESOARE. Resurse hardware. Prezentare, programare şi aplicaţii. Ed. Albastră Cluj Napoca 2004, ISBN 973-650-109-4

-Tischer M., Jennerich B. *"LA BIBLE PC" PROGRAMMATION SYSTEME.* MICRO Application 2003

-Sztojanov, I. şi col. *De la poarta TTL la Microprocesor (vol. II)* Ed. TEHNICĂ

-Buchanan, W. *PC interfacing, Communications and Windows Programming* Addison Wesley 1999

-N. Mathivanan Microprocessors, PC Hardware and Interfacing PHI Learning Pvt. Ltd., 2003 ISBN 8120323173, 9788120323179 .....

-*www.pcguide.com, www.intel.com ,.....*

-*.....*

- ***SLIDES:*** *http://users.utcluj.ro/~elupu/Curs/index.php*

Evaluation:

Final Mark

- 70% exam (theory + problems) ≥ 4.5

- 30 % laboratory tests ≥4.5

BONUS:

- Course attendance >50% roundup final mark else rounddown

- Homework +PRJ

" Life is hard, especially if you're stupid. " John Wayne

C1
8086/88 MIN/MAX MODES

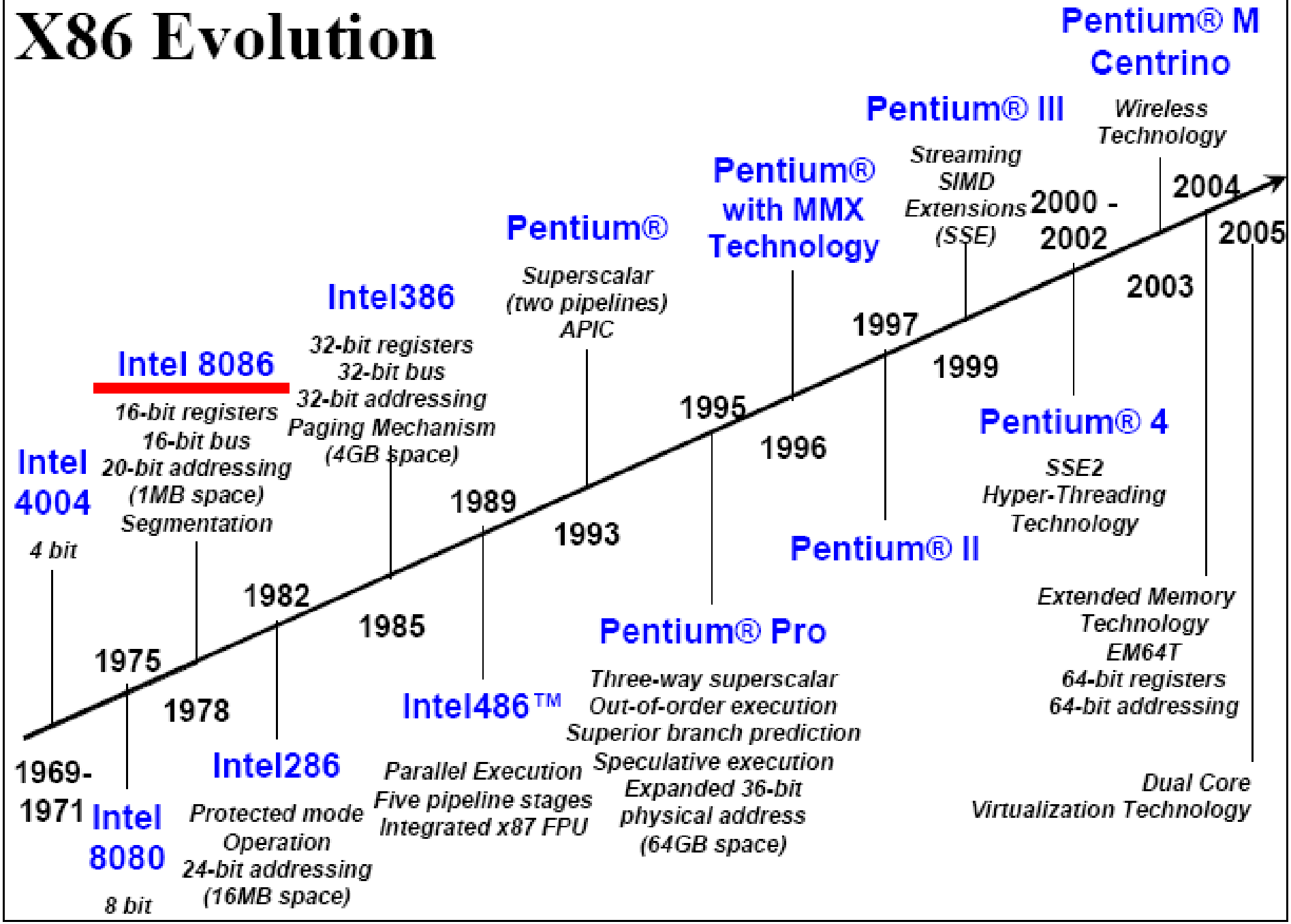
OUTLINE

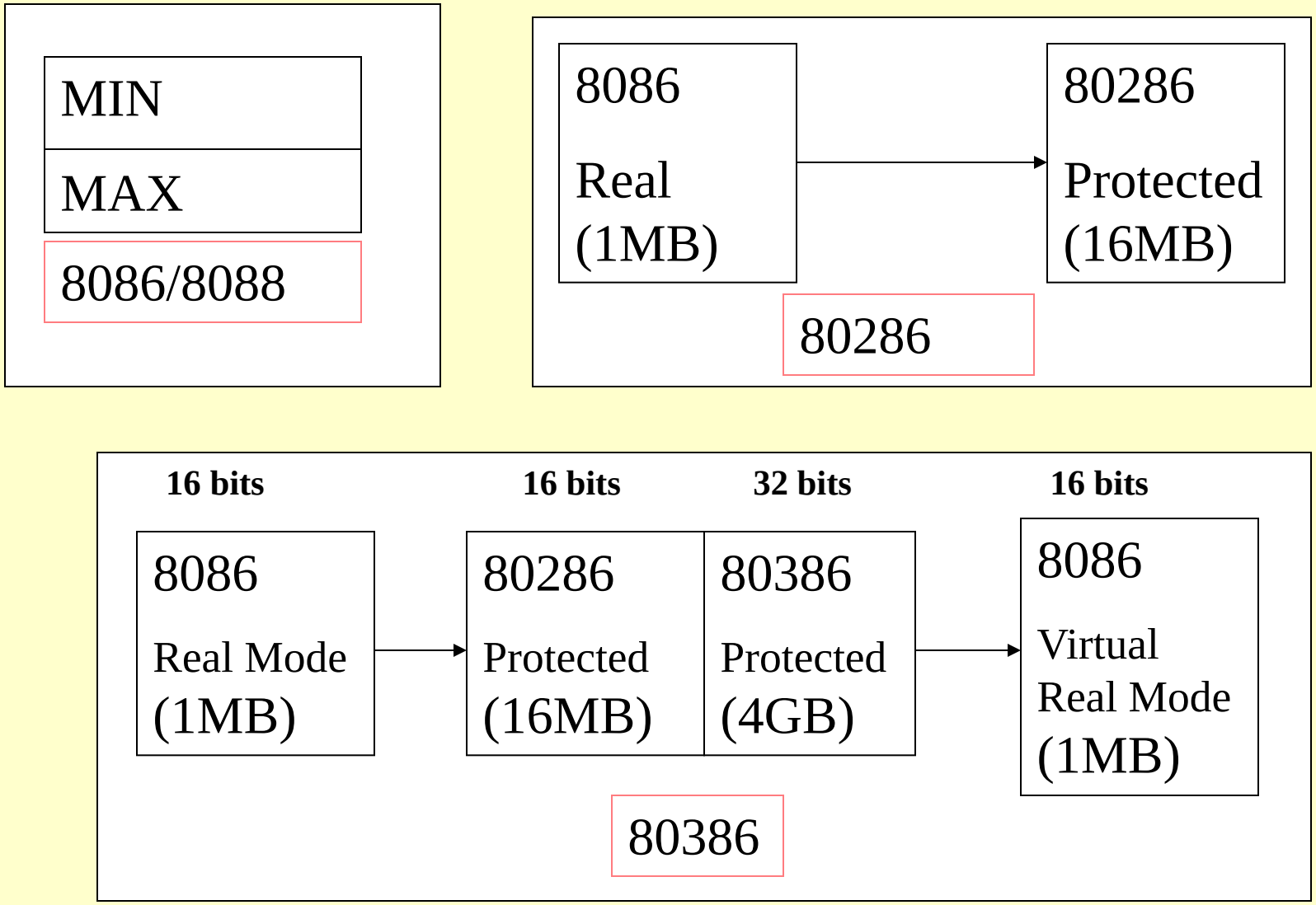
- 8086/88 MIN/MAX modes
- Pin out
- Microsystems using 8086/88 in minimum mode
- 8284 Clock Generator
- 8086 timing
- Microsystems using 8086/88 in maximum mode
- Bus Controller 8288

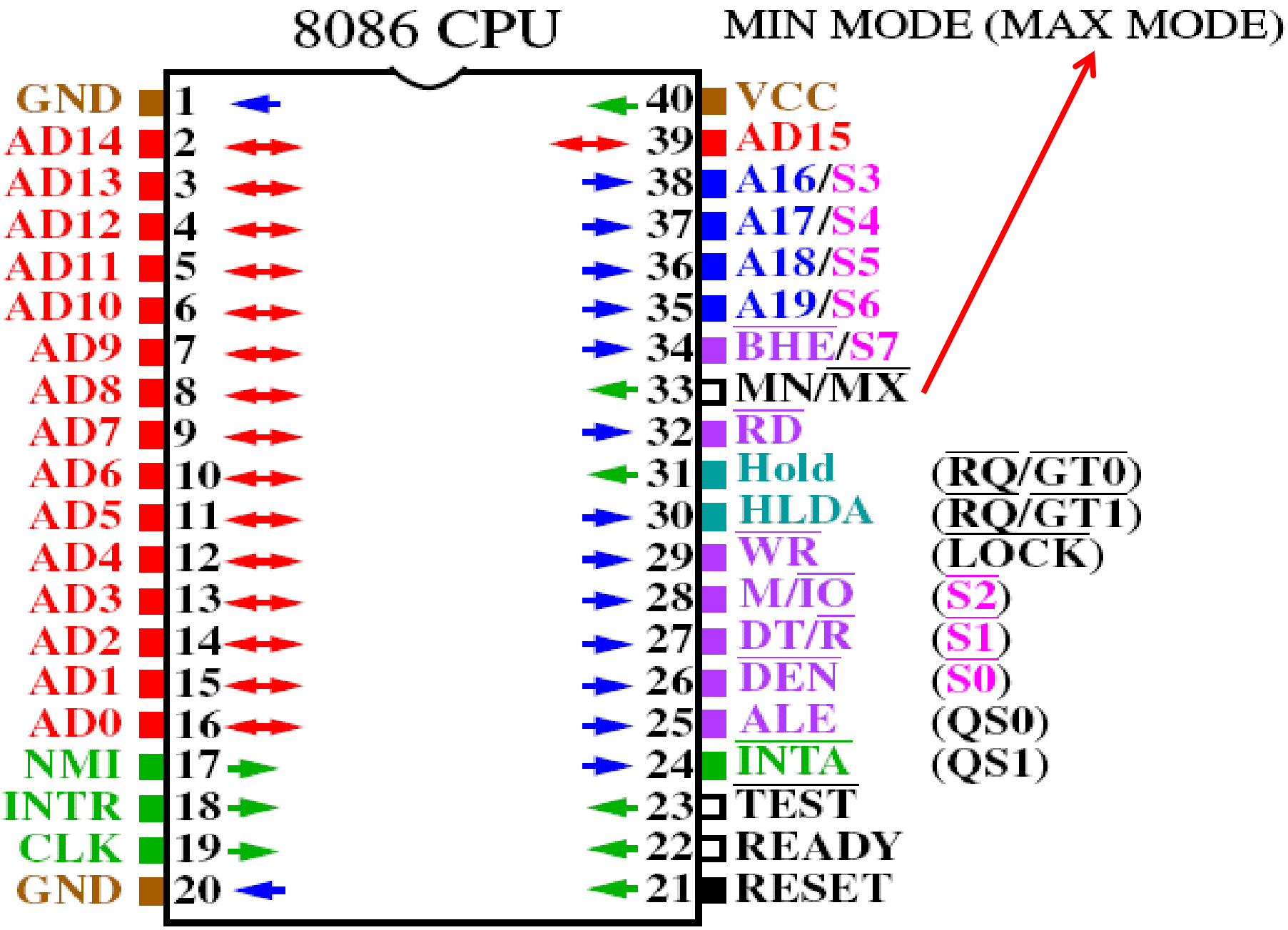
	8086	8088	80286	80386	80486	Pentium	Pentium Pro	Pentium II	Pentium III	Pentium 4	P4 EE
Year	1978	1979	1982	1985	1989	1992	1995	1997	1999	2001	2004
CLK (MHz)	5-10	5-8	6-16	16-33	25-50	60/ 66	150	400	800	1700	3200-3400
Transistors no.	29 k	2 k	130 k	275 k	1.2 M	3.1 M	5.5 M	7.5 M	28 M	42 M	55M
Physical Memory	1 Mo	1 Mo	16 Mo	4 Go	4 Go	4 Go	64 Go	64 Go	64 Go	64 Go	
Internal Data Bus	16	16	16	32	32	32	32	32	32	32	
External Data Bus	16	8	16	32	32	64	64	64	64	64	
Data Type	8, 16	8, 16	8, 16	8, 16, 32	8,16, 32	8,16, 32	8, 16, 32	8, 16, 32	8, 16, 32	8, 16, 32	
Cache Memory	--	--	--	--	8 ko L1	16 ko L1	16 ko L1 256/512ko L2	32 ko L1 256/512ko L2	32 ko L1 256/512ko L2	20 ko L1 512ko L2	+ 2Mo L3
MIPS~	0.8	0.8	2.7	6	20	100	440	440	700	3000	13000

General features of Intel processors on 16/32 bits used in PCs

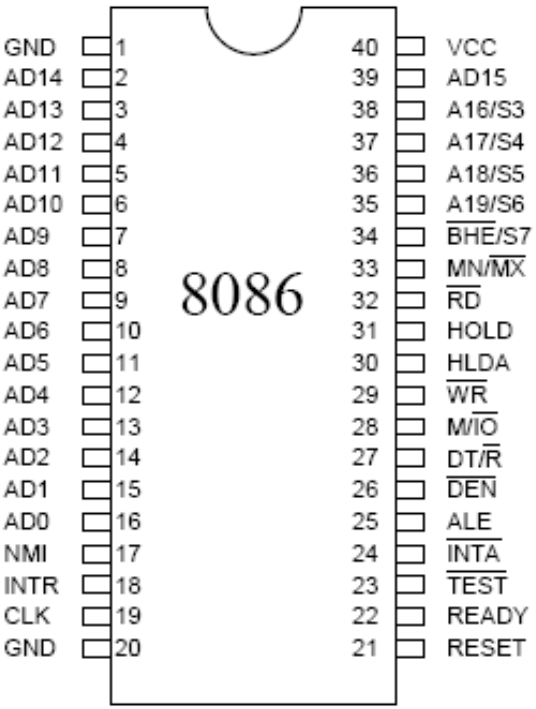
X86 Evolution

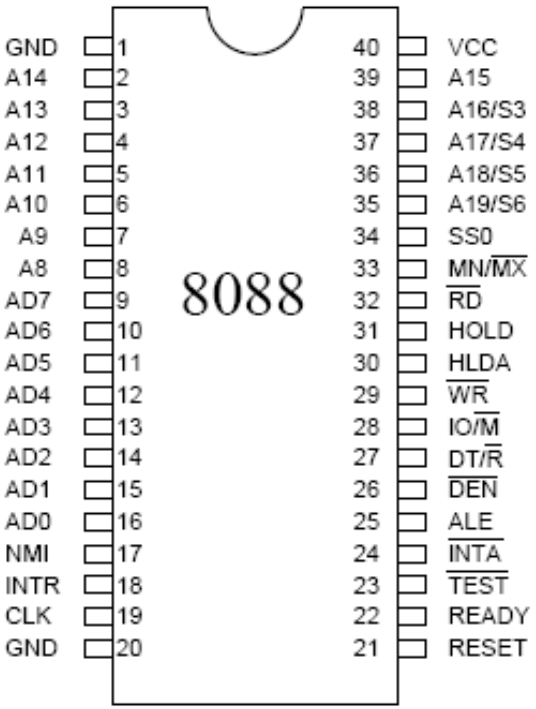



MIN
MAX
8086/8088
8086
Real
(1MB)
80286
Protected
(16MB)
80286
16 bits
16 bits
32 bits
16 bits
8086
Real Mode
(1MB)
80286
Protected
(16MB)
80386
Protected
(4GB)
8086
Virtual
Real Mode
(1MB)
80386


8086 CPU
MIN MODE (MAX MODE)
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 Hold (RQ/GT0)
30 HLDA (RQ/GT1)
29 WR (LOCK)
28 M/IO (S2)
27 DT/R (S1)
26 DEN (S0)
25 ALE (QS0)
24 INTA (QS1)
23 TEST
22 READY
21 RESET

8086/8088 Pinout Diagrams





8086			8088		
Pin	Mode		Pin	Mode	
	Minimum	Maximum		Minimum	Maximum
31	HOLD	RQ/GT0	31	HOLD	RQ/GT0
30	HLDA	RQ/GT1	30	HLDA	RQ/GT1
29	WR	LOCK	29	WR	LOCK
28	M/IO	S2	28	IO/M	S2
27	DT/R	S1	27	DT/R	S1
26	DEN	S0	26	DEN	S0
25	ALE	QS0	25	ALE	QS0
24	INTA	QS1	24	INTA	QS1
			34	SS0	High State

**Minimum/Maximum Mode Refers to the Bus Handshaking*

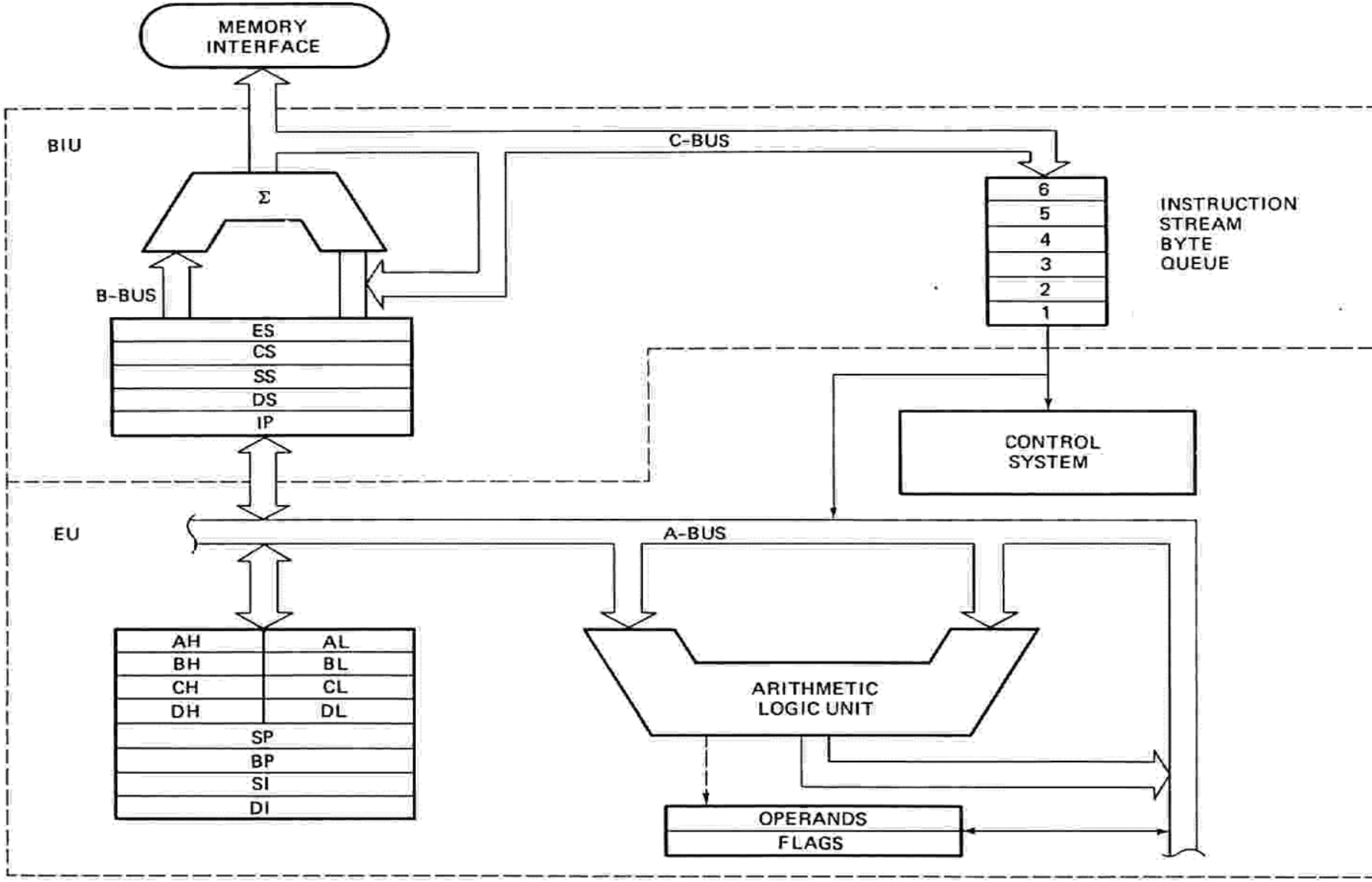


FIGURE 2-7 8086 internal block diagram. (*Intel Corp.*)

8086 Pinout Signals

- *AD15-AD0*

  Multiplexed address(ALE=1)/data bus(ALE=0).

- *A19/S6-A16/S3* (multiplexed)

  High order 4 bits of the 20-bit address OR status bits S6-S3.

- $M/\overline{IO}$

  Indicates if address is a Memory or IO address.

- $\overline{RD}$

  When 0, data bus is driven by memory or an I/O device.

- $\overline{WR}$

  Microprocessor is driving data bus to memory or an I/O device. When 0, data bus contains valid data.

- *ALE* (Address latch enable)

  When 1, address data bus contains a memory or I/O address.

- $DT/\overline{R}$ (Data Transmit/Receive)

  Data bus is transmitting/receiving data.

- *DEN* (Data bus Enable)

  Activates external data bus buffers.

- *S7, S6, S5, S4, S3, $\overline{S2}$, $\overline{S1}$, $\overline{S0}$*

  S7: Logic 1, S6: Logic 0.

  S5: Indicates condition of IF flag bits.

  S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{S2}$, $\overline{S1}$, $\overline{S0}$: Indicate function of current bus cycle (decoded by 8288).

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt Ack
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Passive

- ***INTR***

  When 1 and IF=1, microprocessor prepares to service interrupt. $\overline{\text{INTA}}$ becomes active after current instruction completes.

- ***$\overline{\text{INTA}}$***

  Interrupt Acknowledge generated by the microprocessor in response to INTR. Causes the interrupt vector to be put onto the data bus.

- ***NMI***

  Non-maskable interrupt. Similar to INTR except IF flag bit is not consulted and interrupt is vector 2.

- ***CLK***

  Clock input must have a duty cycle of 33% (high for 1/3 and low for 2/3s)

- ***VCC/GND***

  Power supply (5V) and GND (0V)

- ***MN/$\overline{\text{MX}}$***

  Select minimum (5V) or maximum mode (0V) of operation.

- ***$\overline{BHE}$***

  Bus High Enable. Enables the most significant data bus bits (D_{15}-D_8) during a read or write operation.

- ***READY***

  Used to insert wait states (controlled by memory and IO for reads/writes) into the microprocessor.

- ***RESET***

  Microprocessor resets if this pin is held high for 4 clock periods.

  Instruction execution begins at FFFF0H and IF flag is cleared.

- ***$\overline{TEST}$***

  An input that is tested by the WAIT instruction.

  Commonly connected to the 8087 coprocessor.

- ***HOLD***

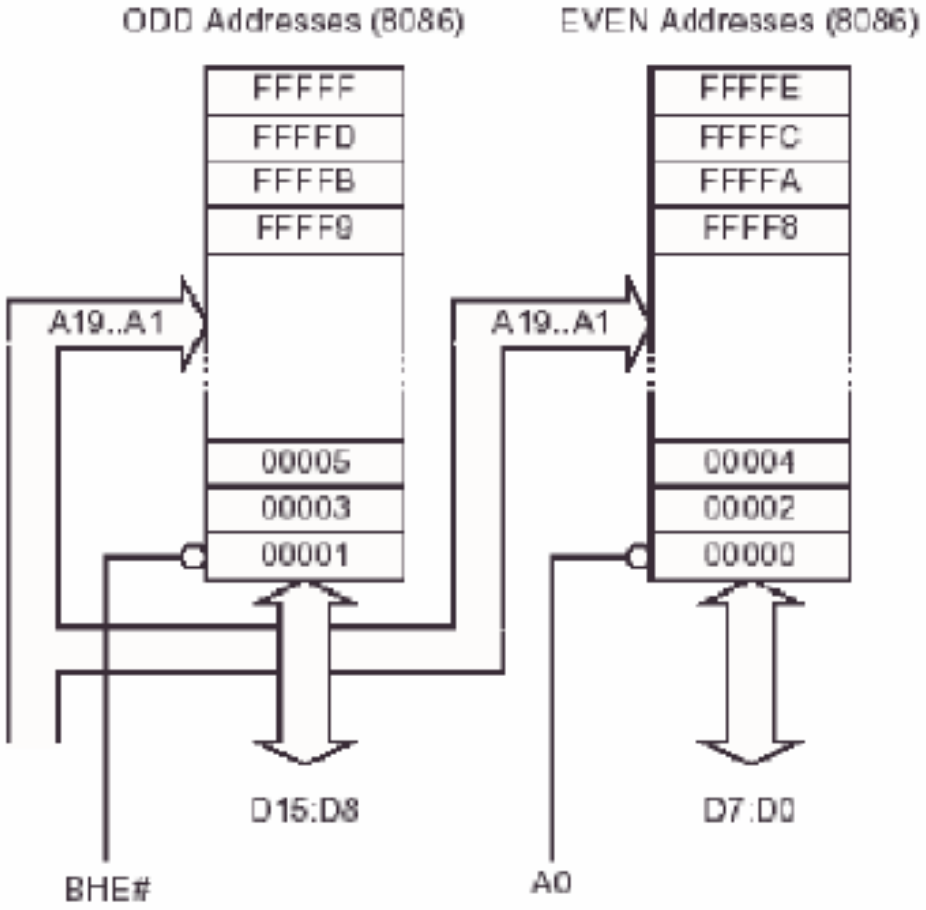
  Requests a direct memory access (DMA). When 1, microprocessor stops and places address, data and control bus in high-impedance state.

- ***HLDA*** (Hold Acknowledge)

  Indicates that the microprocessor has entered the hold state.

✓**BHE (Bank High Enable) line** (8086 only) :=0 for most significant byte of data and also carries S_7=1

BHE#	A0	Selection
0	0	Whole word (16-bits)
0	1	High byte to/from odd address
1	0	Low byte to/from even address
1	1	No selection



- $\overline{RQ}/GT1$ and $\overline{RQ}/GT0$

  Request/grant pins request/grant direct memory accesses (DMA) during maximum mode operation.

- $\overline{LOCK}$

  Lock output is used to lock peripherals off the system. Activated by using the LOCK: prefix on any instruction.

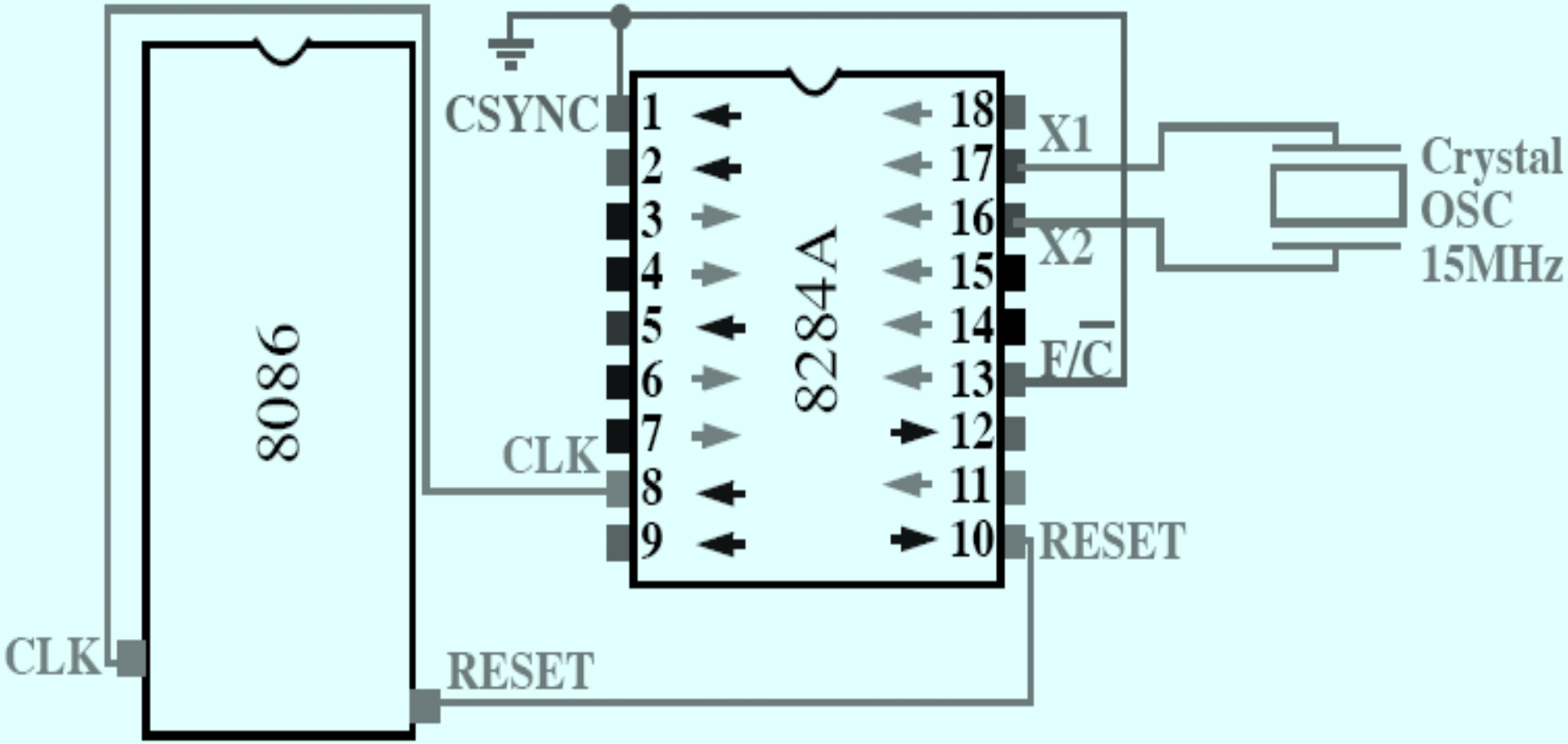
- *QS1 and QS0*

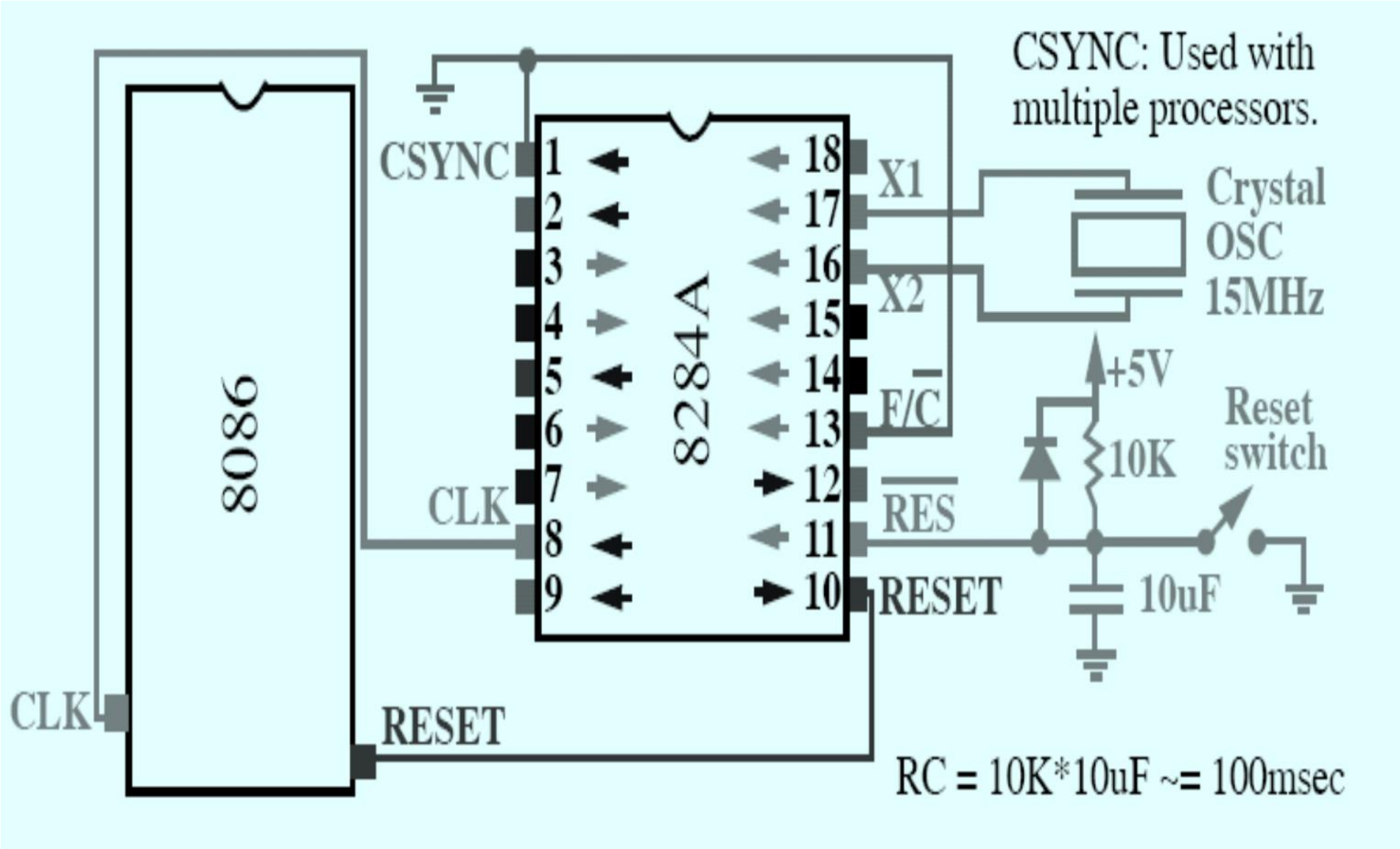
  The queue status bits show status of internal instruction queue. Provided for access by the numeric coprocessor (8087).

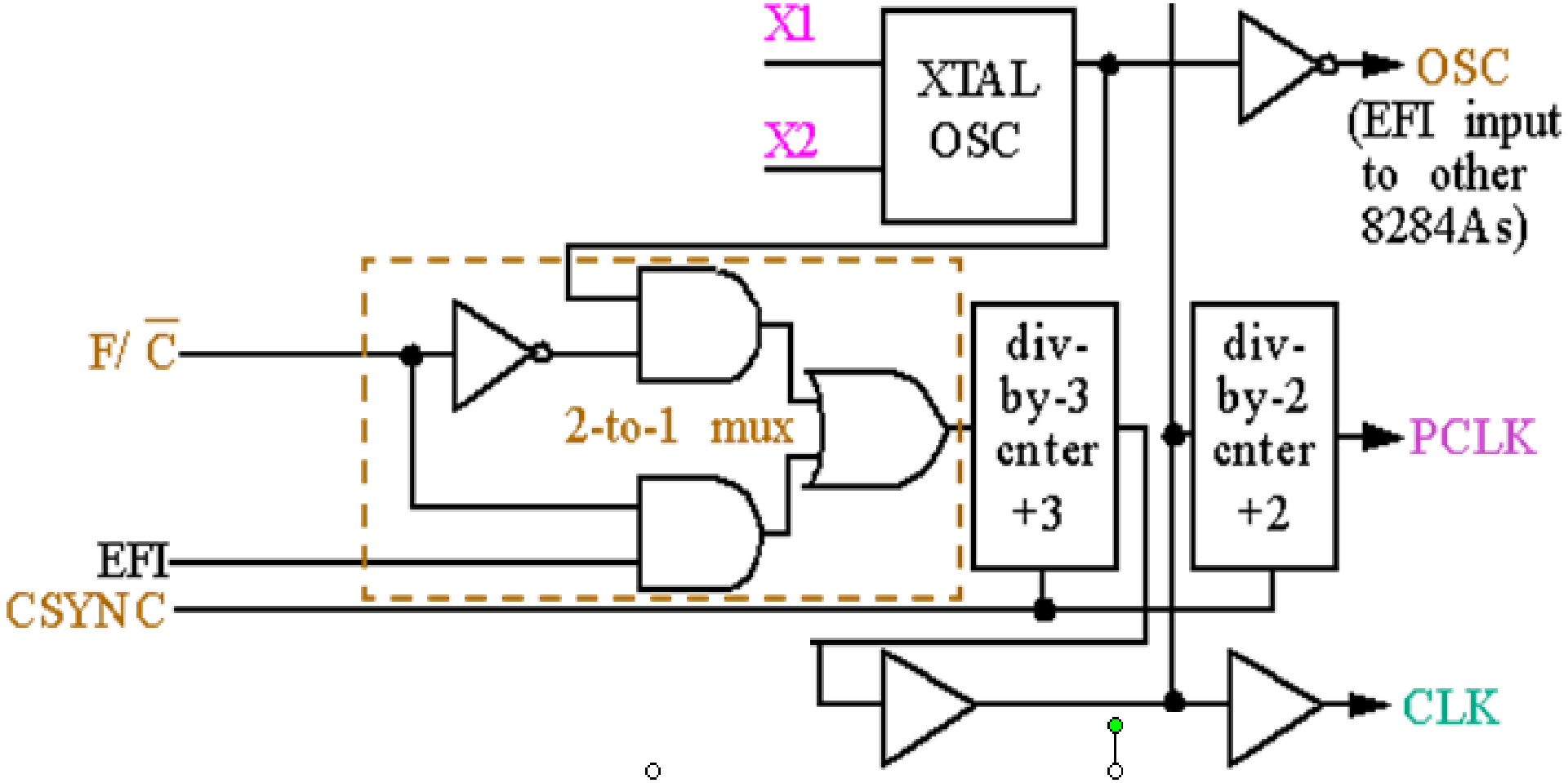
8284 – CLOCK GENERATION

- Clock generation
- RESET synchronization
- READY synchronization
- Peripheral clock signal

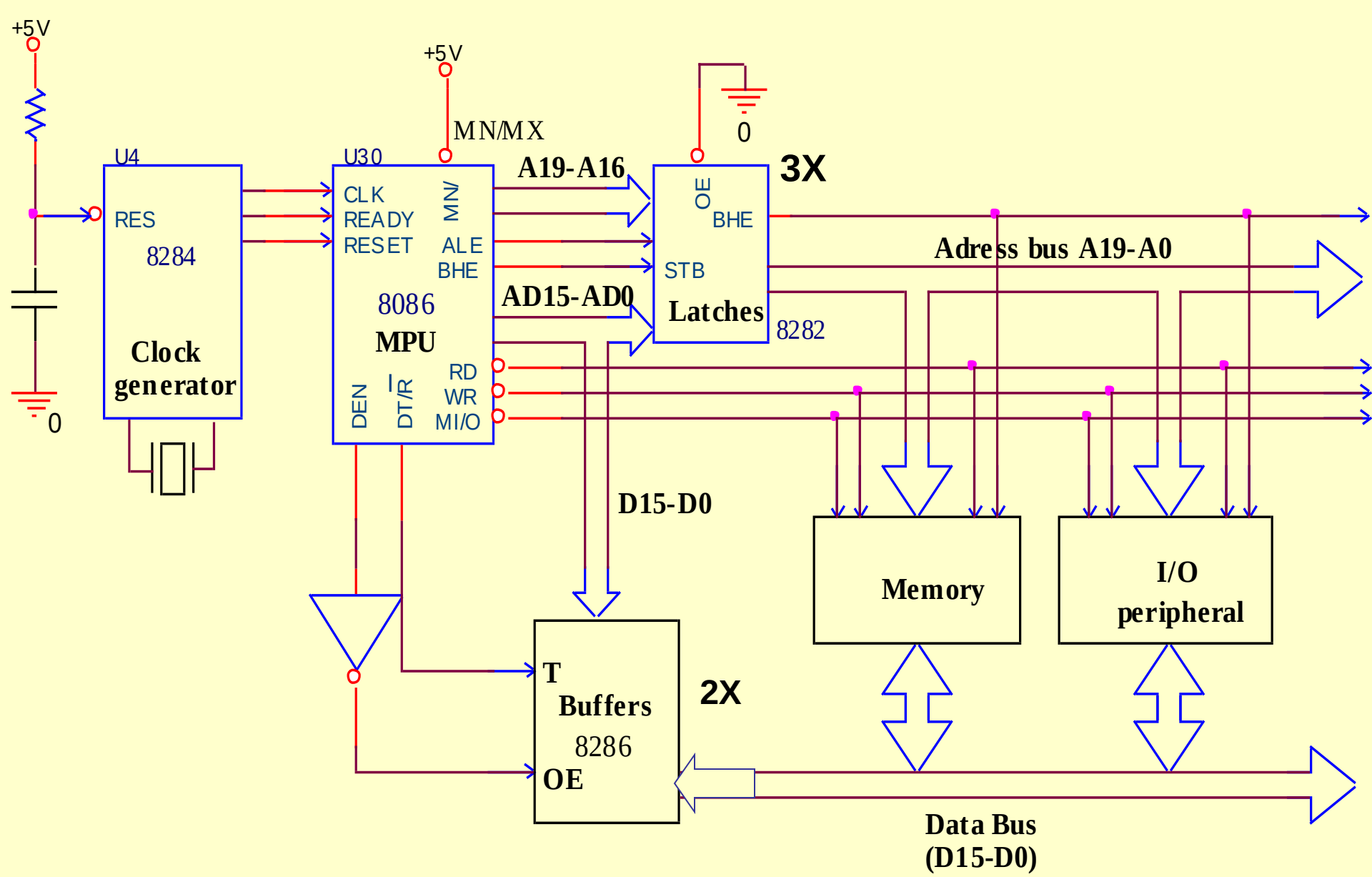
Connection of the 8284 and the 8086.



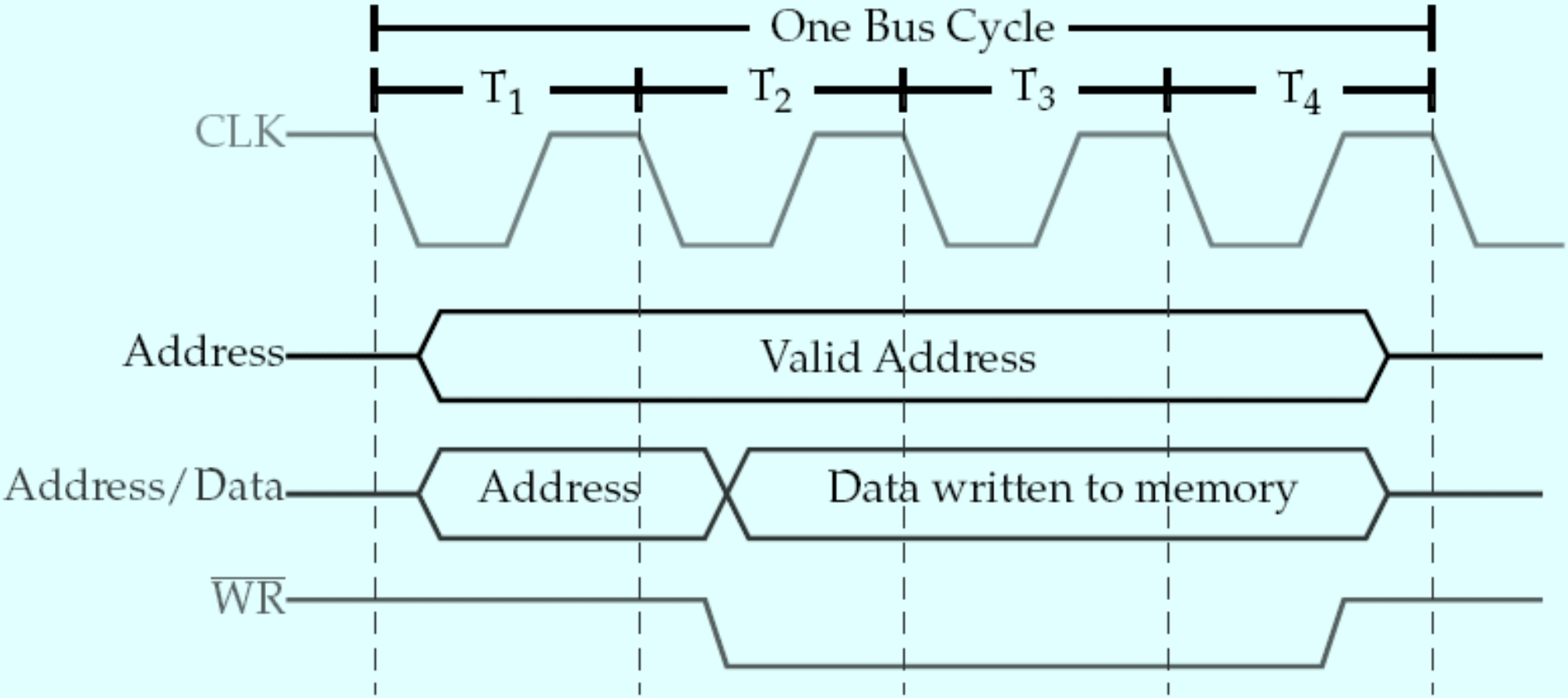

CSYNC: Used with multiple processors.
8086
8284A
CSYNC
CLK
RESET
X1
X2
F/C
RES
RESET
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
Crystal OSC 15MHz
+5V
10K
Reset switch
10uF
CLK
RESET
RC = 10K*10uF ~= 100msec



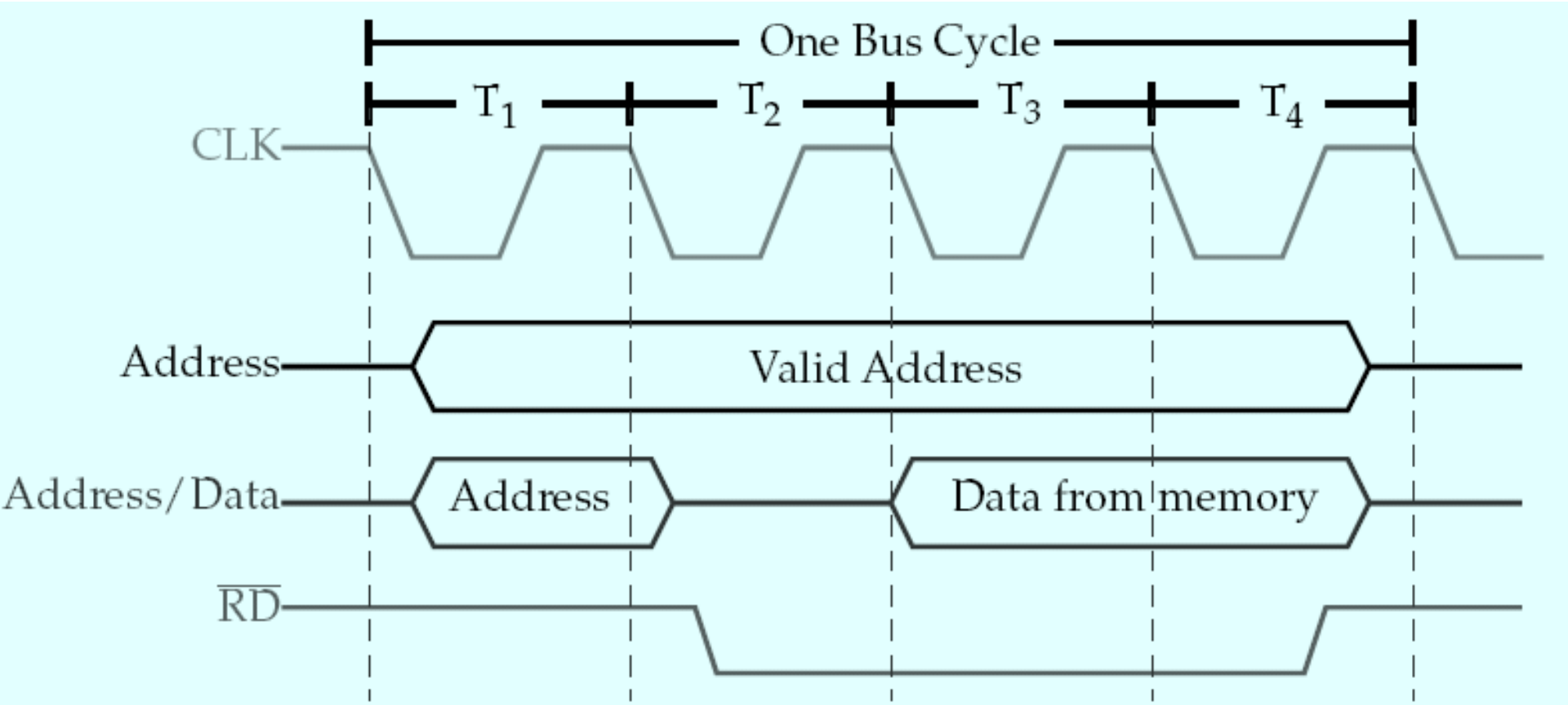
Block diagram of the 8284



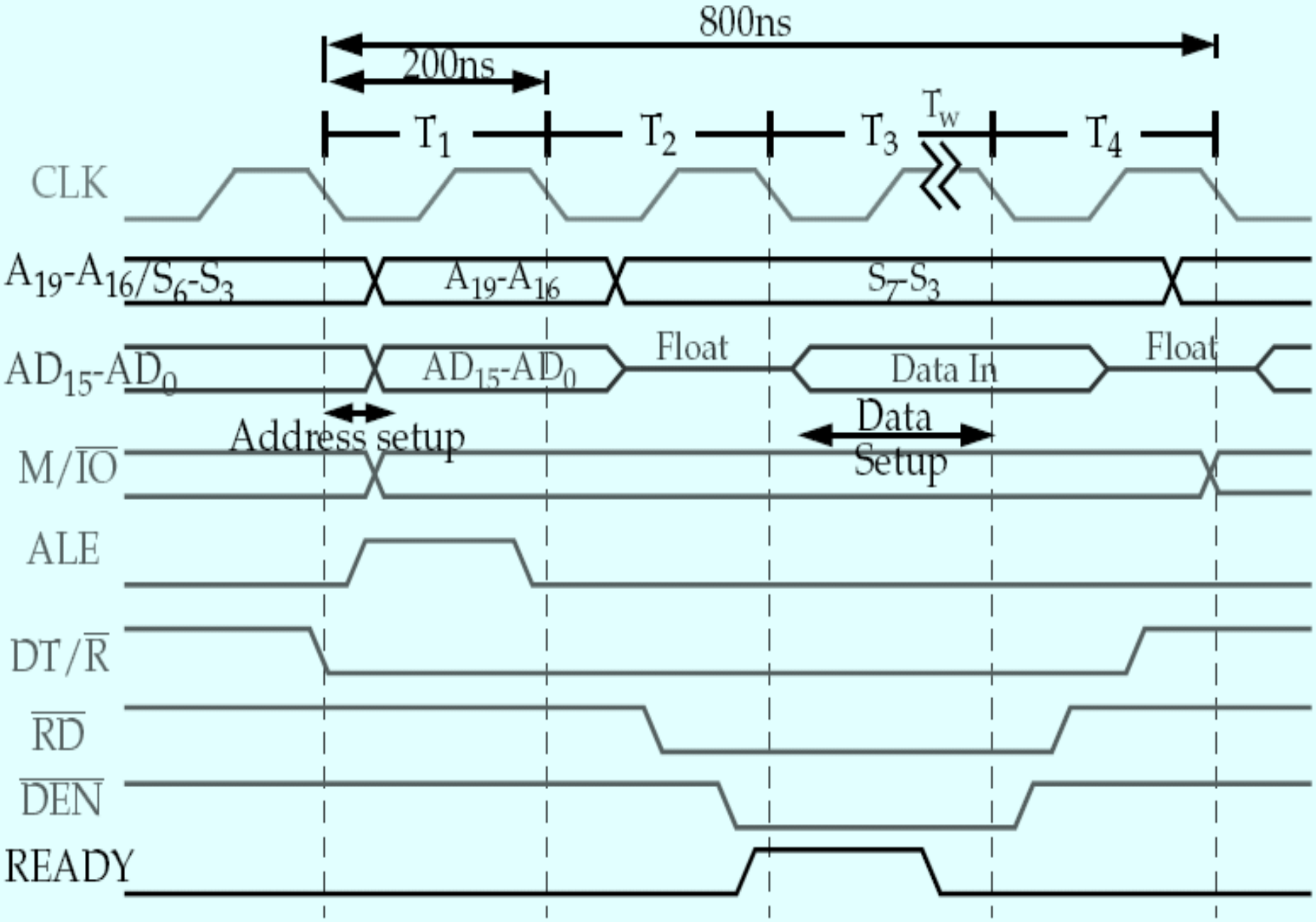
Microsystem using 8086 in minimum mode



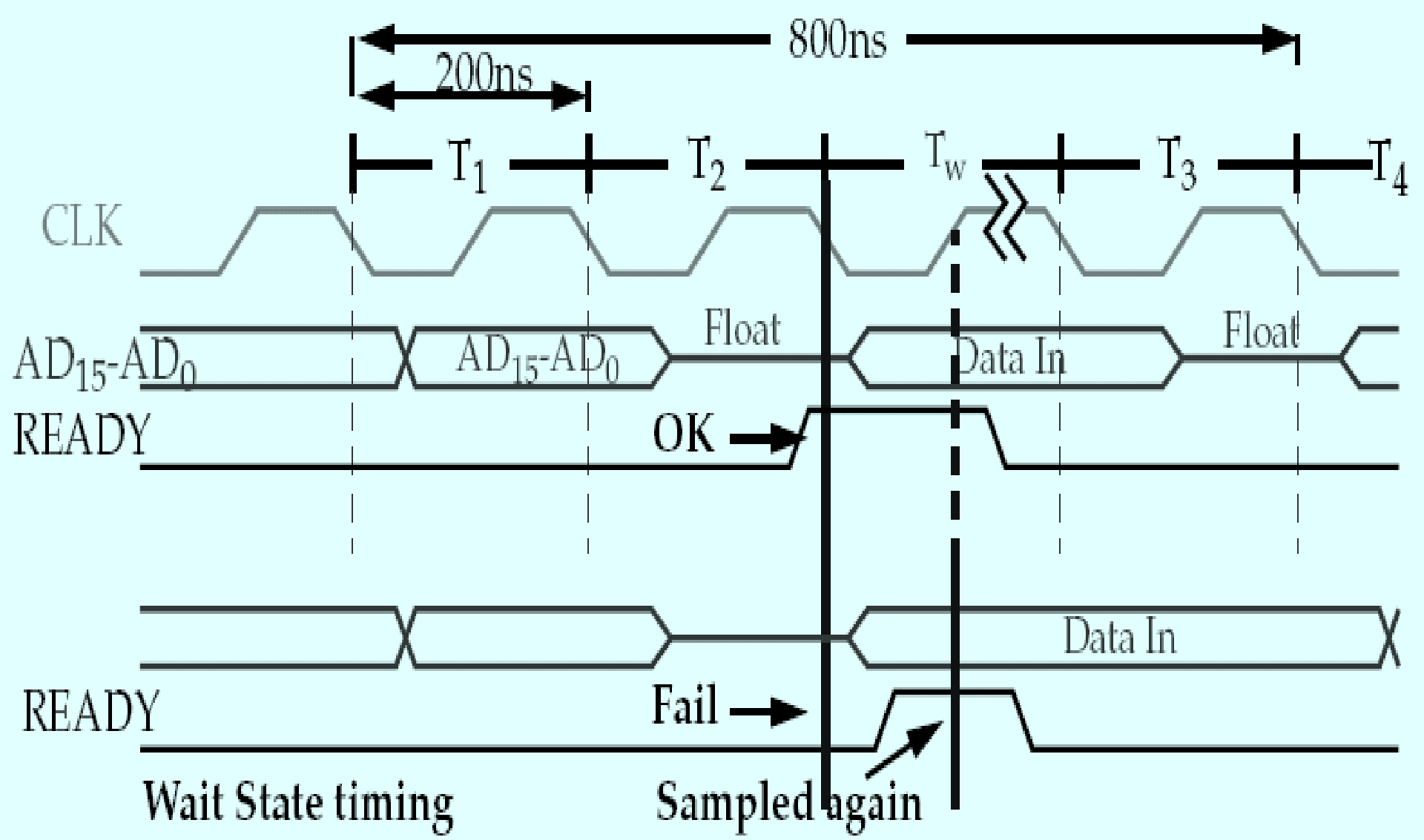
Simplified 8086 Write Bus Cycle



Simplified 8086 Read Bus Cycle



Bus Timing for a Read Operation


800ns
200ns
T1
T2
Tw
T3
T4
CLK
AD15-AD0
AD15-AD0
Float
Data In
Float
READY
OK
Data In
READY
Fail
Wait State timing
Sampled again

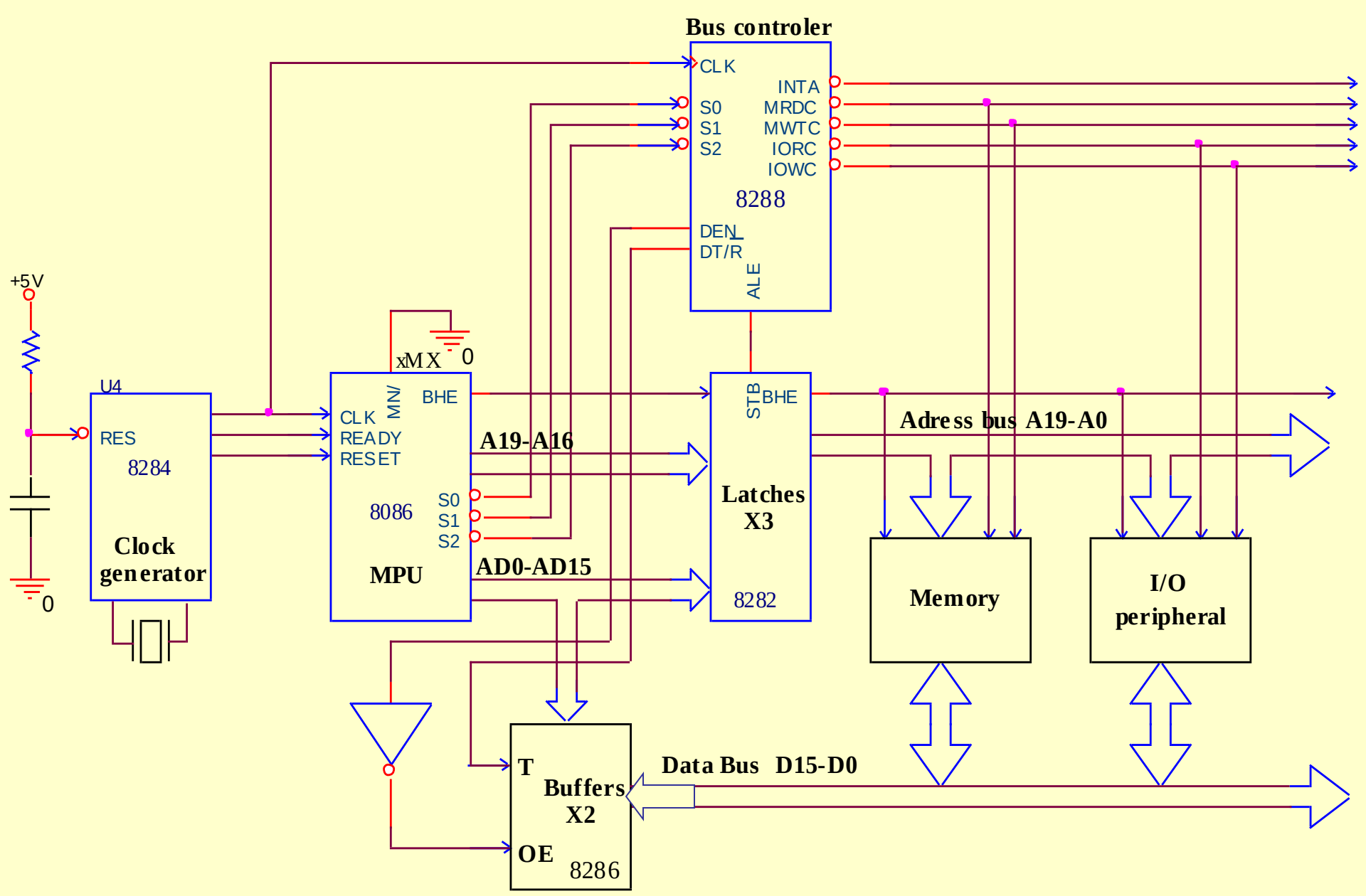
Bus Cycle and Time States

T1 - start of bus cycle. Actions include setting control signals (or S0-S2 status lines) to give the required values for ALE, DTR IO/M putting a valid address onto the address bus.

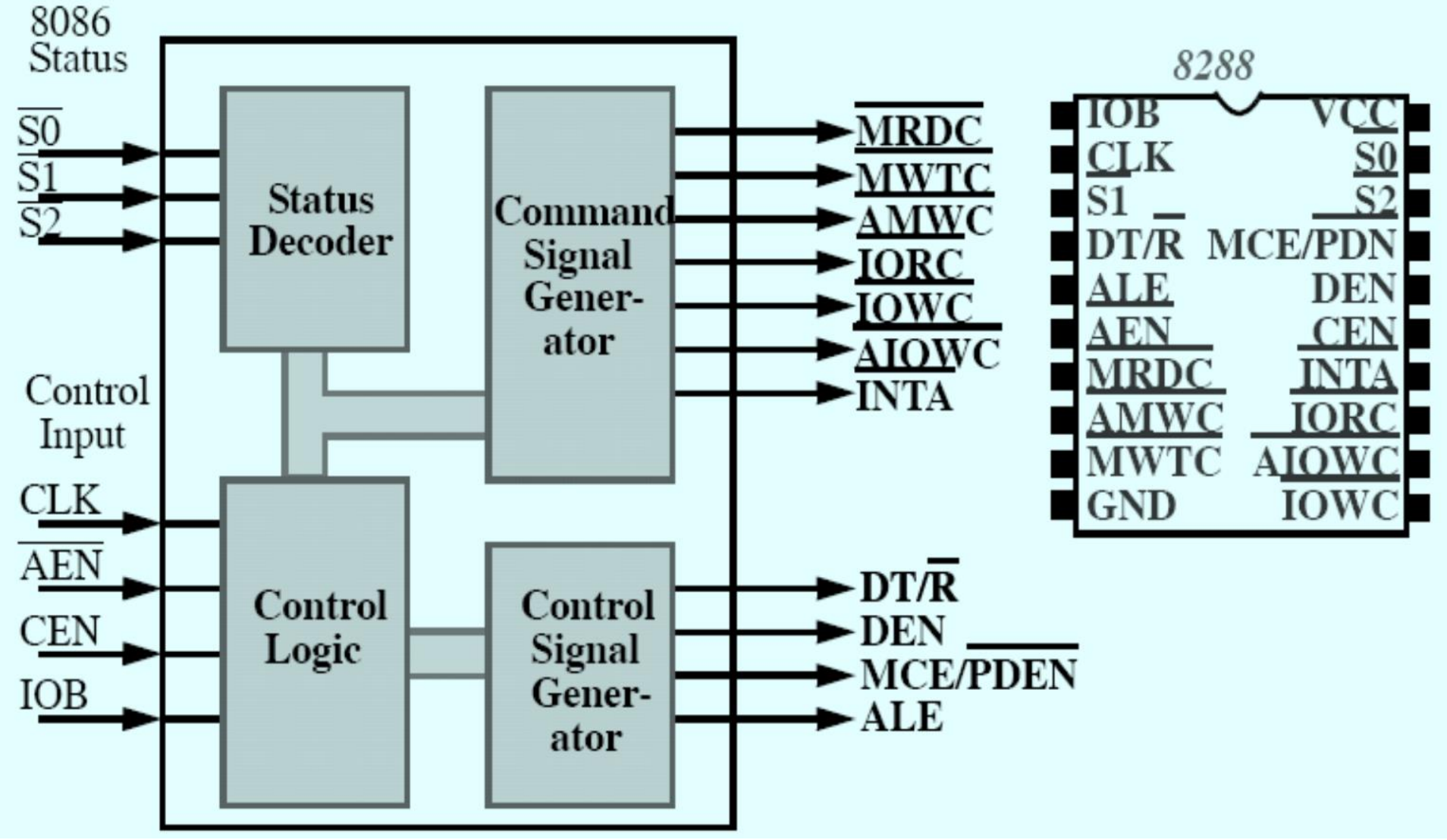
T2 - the RD or WR control signals are issued, DEN is asserted and in the case of a write, data is put onto the data bus. The DEN turns on the data bus buffers to connect the CPU to the external data bus. The READY input to the CPU is sampled at the end of T2 and if READY is low, a wait state T_W (one or more) is inserted before T3 begins.

T3 - this clock period is provided to allow memory to access the data. If the bus cycle is a read cycle, the data bus is sampled at the end of T3.

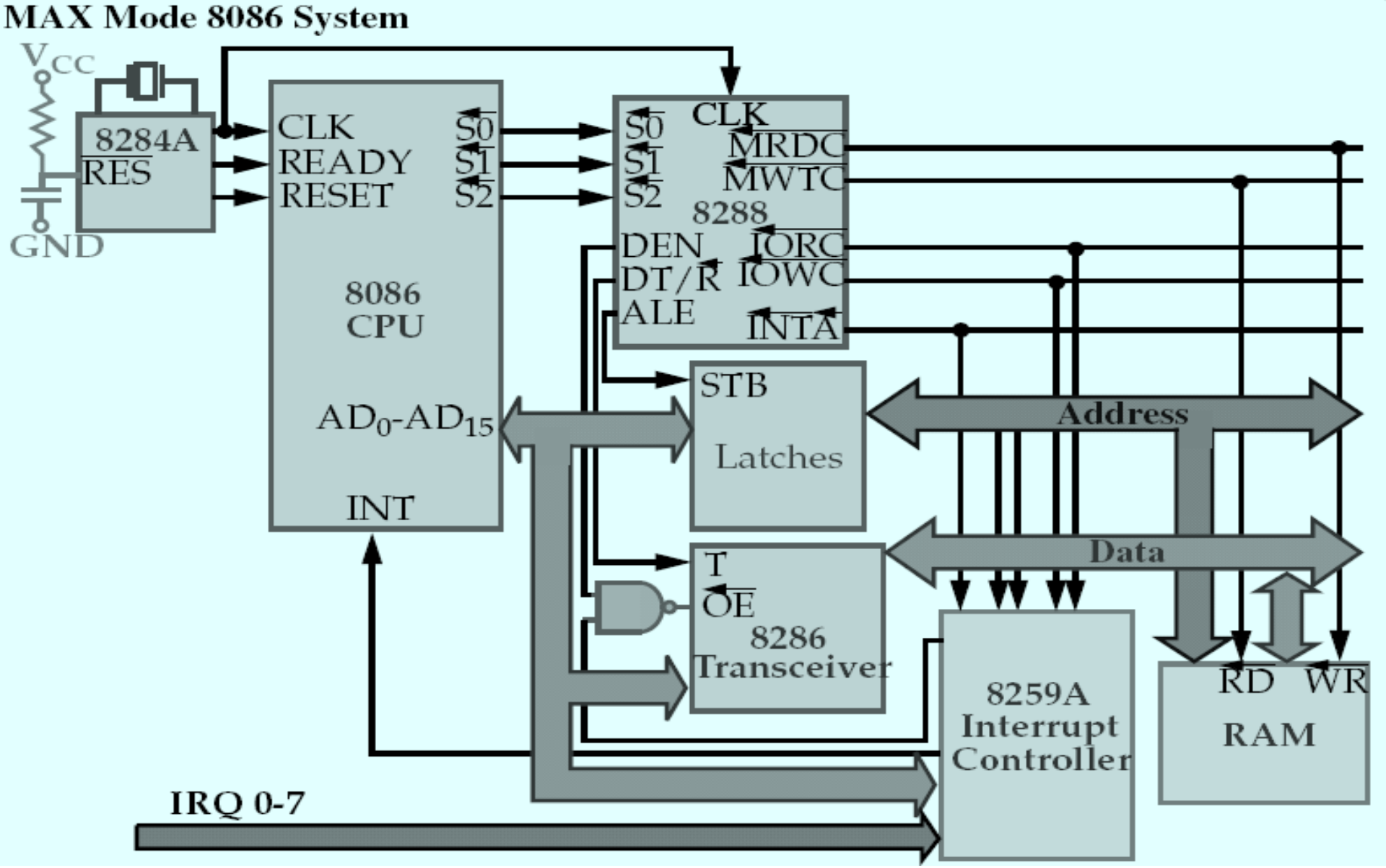
T4 - all bus signals are deactivated in preparation for the next clock cycle. The 8088 also finishes sampling the data (in a read cycle) in this period. For the write cycle, the trailing edge of the WR signal transfers data to the memory or I/O, which activates and write when WR returns to logic 1 level.

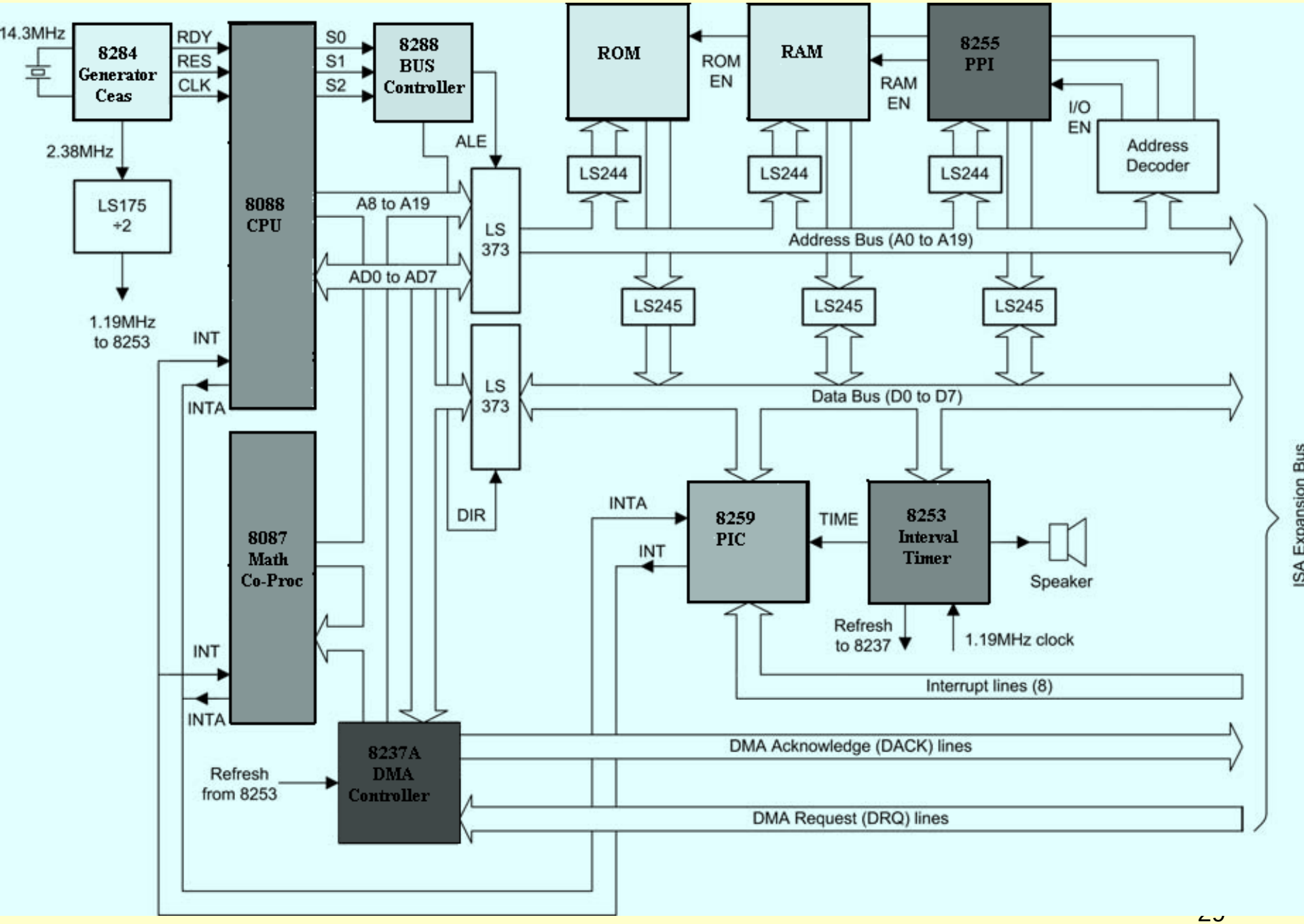


Microsystem using 8086 in maximum mode



Block diagram of the 8288 Bus Controller


MAX Mode 8086 System
VCC
GND
8284A
RES
CLK
READY
RESET
S0
S1
S2
8086
CPU
AD0-AD15
INT
CLK
S0
S1
S2
8288
DEN
DT/R
ALE
MRDC
MWTC
IORC
IOWC
INTA
STB
Latches
Address
Data
T
OE
8286
Transceiver
8259A
Interrupt
Controller
RD
WR
RAM
IRQ 0-7


14.3MHz
8284
Generator
Ceas
RDY
RES
CLK
2.38MHz
LS175
÷2
1.19MHz
to 8253
8088
CPU
INT
INTA
S0
S1
S2
8288
BUS
Controller
ALE
A8 to A19
AD0 to AD7
LS
373
LS
373
DIR
ROM
RAM
8255
PPI
ROM
EN
RAM
EN
I/O
EN
Address
Decoder
LS244
LS244
LS244
Address Bus (A0 to A19)
LS245
LS245
LS245
Data Bus (D0 to D7)
8087
Math
Co-Proc
INT
INTA
8259
PIC
INTA
INT
TIME
8253
Interval
Timer
Speaker
Refresh
to 8237
1.19MHz clock
Interrupt lines (8)
8237A
DMA
Controller
Refresh
from 8253
DMA Acknowledge (DACK) lines
DMA Request (DRQ) lines
ISA Expansion Bus

8086 interview questions

- **What are the flags in 8086?** - In 8086 Carry flag, Parity flag, Auxiliary carry flag, Zero flag, Overflow flag, Trace flag, Interrupt flag, Direction flag, and Sign flag.
- **What are the various interrupts in 8086?** - Maskable interrupts, Non-Maskable interrupts.
- **What is meant by Maskable interrupts?** - An interrupt that can be turned off by the programmer is known as Maskable interrupt.
- **What is Non-Maskable interrupts?** - An interrupt which can be never be turned off (ie.disabled) is known as Non-Maskable interrupt.
- **Which interrupts are generally used for critical events?** - Non-Maskable interrupts are used in critical events. Such as Power failure, Emergency, Shut off etc.,
- **Give example for Non-Maskable interrupts?** - Trap is known as Non-Maskable interrupts, which is used in emergency condition.
- **What is the Maximum clock frequency in 8086?** - 5 Mhz is the Maximum clock frequency in 8086.
- **What are the various segment registers in 8086?** - Code, Data, Stack, Extra Segment registers in 8086.
- **Which is the tool used to connect the user and the computer?** - Interpreter is the tool used to connect the user and the tool.
- **What is the position of the Stack Pointer after the PUSH instruction?** - The address line is 02 less than the earlier value.
- **What is the position of the Stack Pointer after the POP instruction?** - The address line is 02 greater than the earlier value.
- **Logic calculations are done in which type of registers?** - Accumulator is the register in which Arithmetic and Logic calculations are done.
- **What are the different functional units in 8086?** - Bus Interface Unit and Execution unit, are the two different functional units in 8086.
- **What is meant by cross-compiler?** - A program runs on one machine and executes on another is called as cross-compiler.
- **Which Segment is used to store interrupt and subroutine return address registers?** - Stack Segment in segment register is used to store interrupt and subroutine return address registers.
- **Which Flags can be set or reset by the programmer and also used to control the operation of the processor?** - Trace Flag, Interrupt Flag, Direction Flag.
- **What does EU do?** - Execution Unit receives program instruction codes and data from BIU, executes these instructions and store the result in general registers.
- **Which microprocessor accepts the program written for 8086 without any changes?** - 8088 is that processor.
- **What is the difference between 8086 and 8088?** - The BIU in 8088 is 8-bit data bus & 16- bit in 8086.Instruction queue is 4 byte long in 8088and 6 byte in 8086.