C13. PROGRAMMABLE PERIPHERAL INTERFACE (PPI)
8255A (PIO)

OUTLINE:

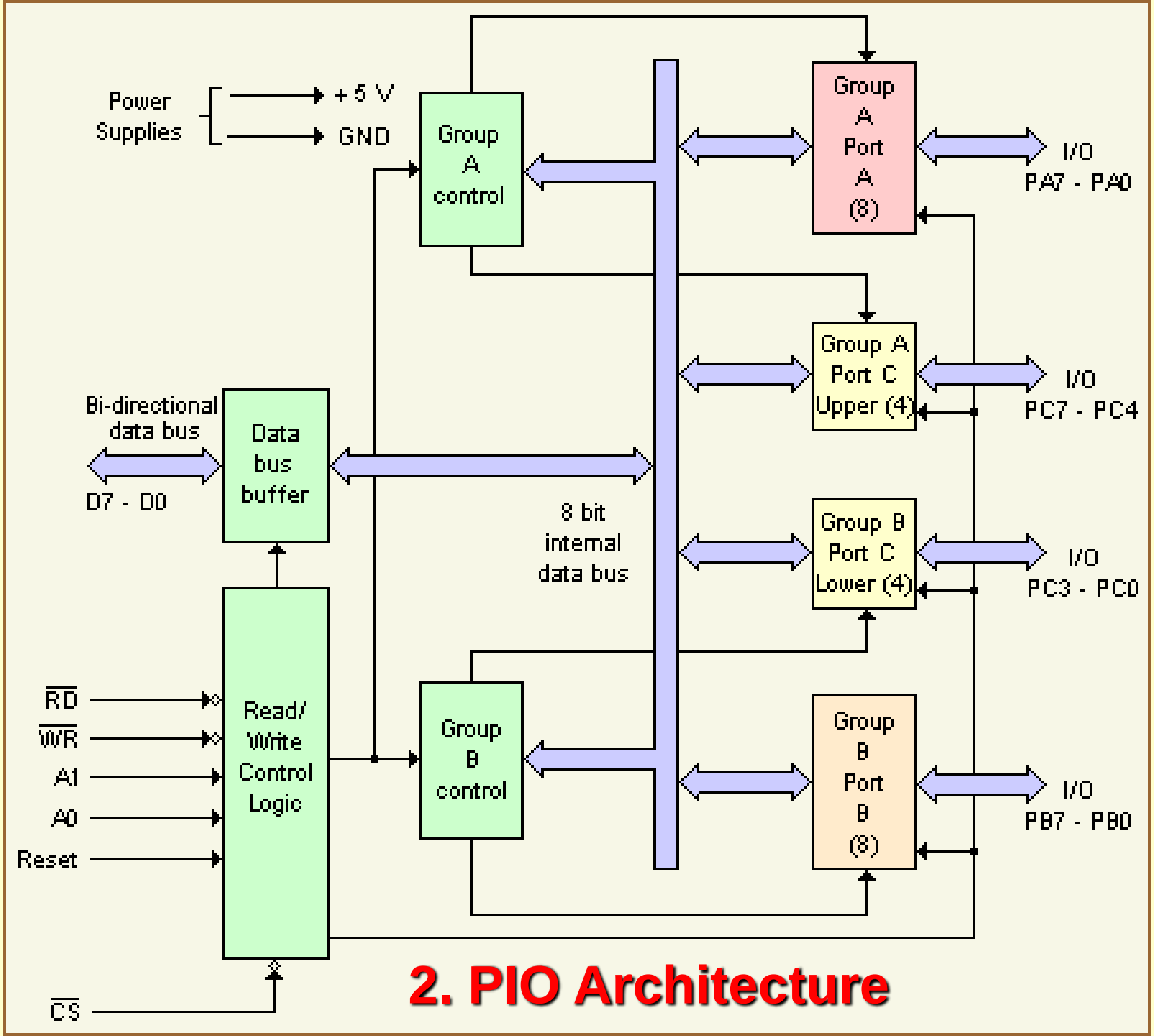
- ✓ PIO description
- ✓ PIO architecture
- ✓ PIO programming
- ✓ PIO in PC
- ✓ Applications

http://www.advancedmsinc.com/iocards/8255.htm
http://www.eisti.fr/~ga/phy/iitr/ii05/tr.pdf

1. PIO Description

- The 8255A implements a programmable peripheral interface for I/O operation
- The 8255A has 24 I/O signals that may be programmed in two groups
- PIO operates in the following three modes:

- ***Mode 0:*** *Basic Input/Output* —Port A, port B, and port C (H&L) may be independently configured as inputs or outputs to read or hold static data. Outputs are latched; inputs are not latched.
- ***Mode 1:*** *Strobed Input/Output*—Port A and port B can be independently configured as strobed input or output ports. Signals from port C are dedicated as control signals for data handshaking.
- ***Mode 2:*** *Bidirectional Bus* —Port A can be configured as a bidirectional bus with the majority bits of port C providing the control signals. In this configuration, port B can still implement mode 0 or mode 1.



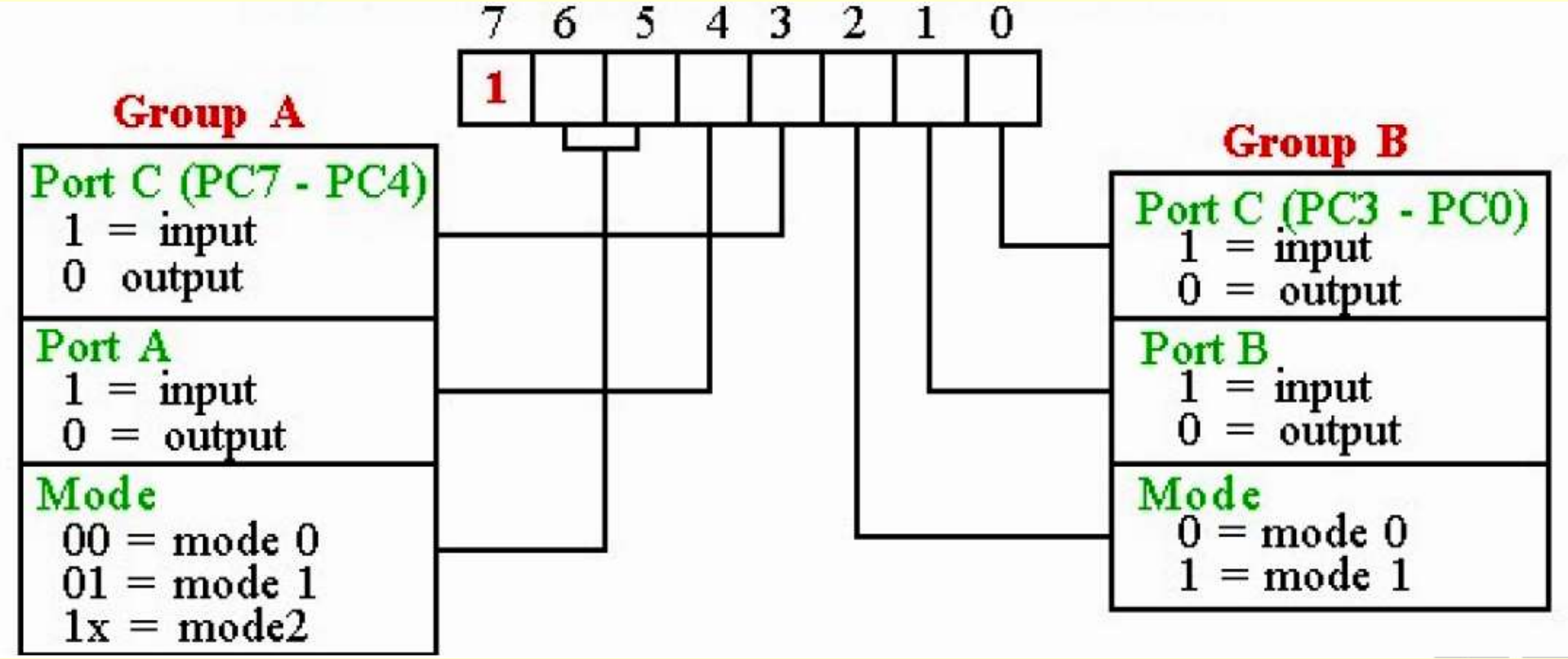
2. PIO Architecture

Register Address Map

A1	A0	Register/Port
0	0	Port A data (all modes)
0	1	Port B data (all modes)
1	0	Port C data (mode 0) and status (modes 1 and 2)
1	1	Control register mode definition / port C bit set/reset

- PIO port addresses reserved in PC: 60h-63h
- To PC-AT, PIO is replaced by a microcontroller , adr. 60h-64h

3. PIO Programming

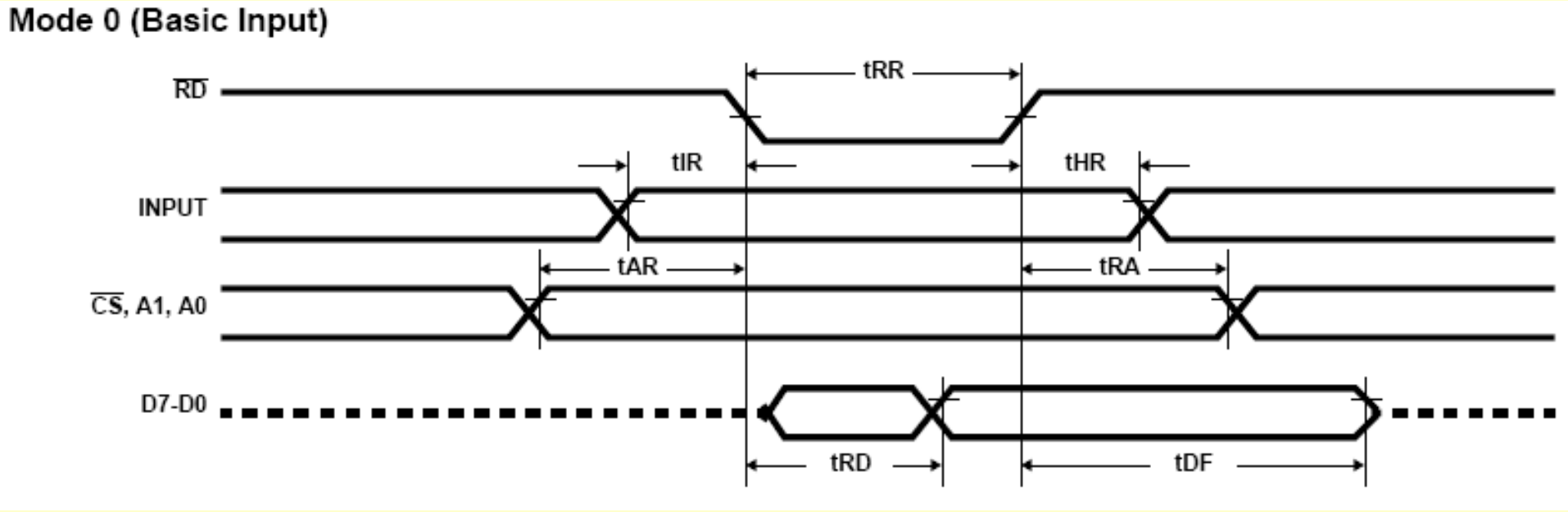


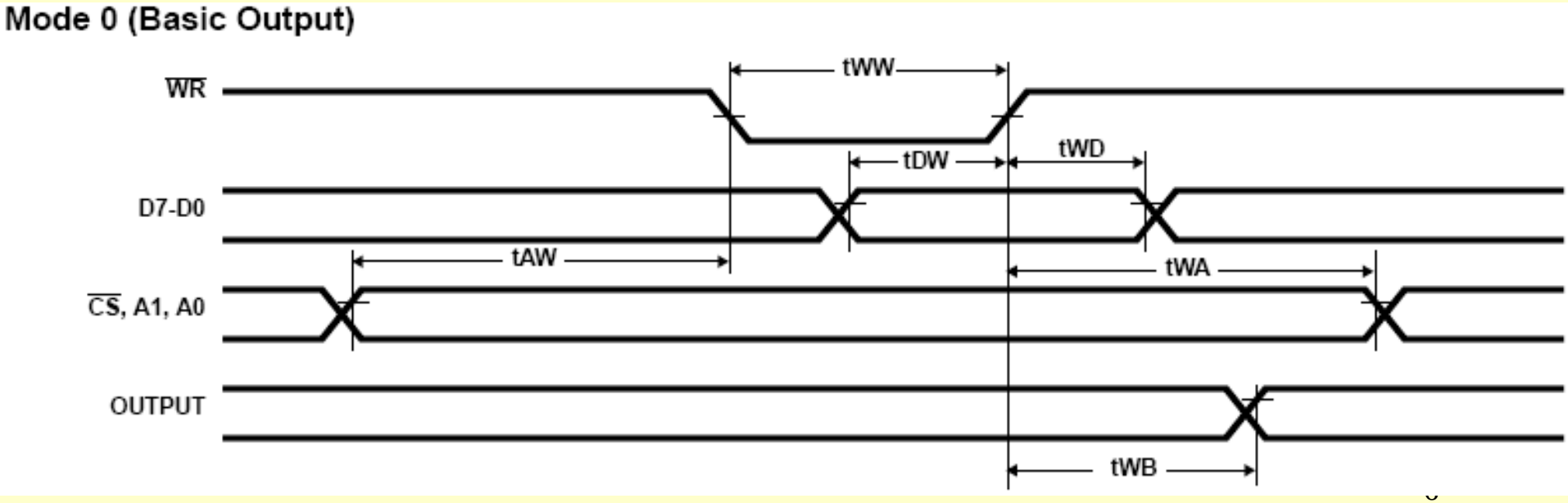
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

1 = I / O Mode

0 = BSR Mode

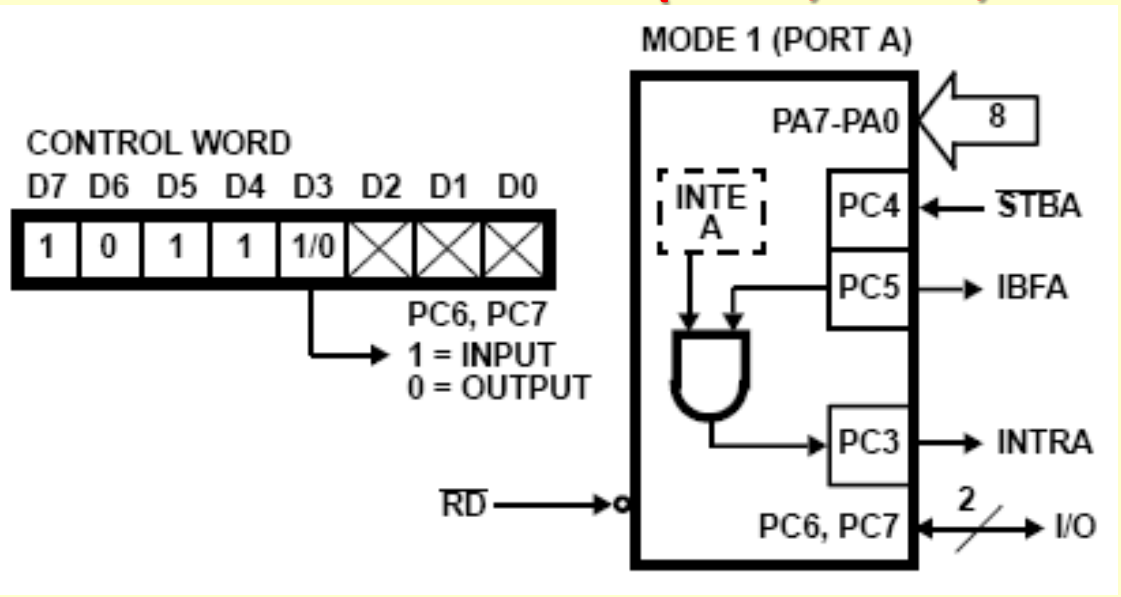
Mode 0: Basic Input/Output (D7=1, D6=D5=D2=0)



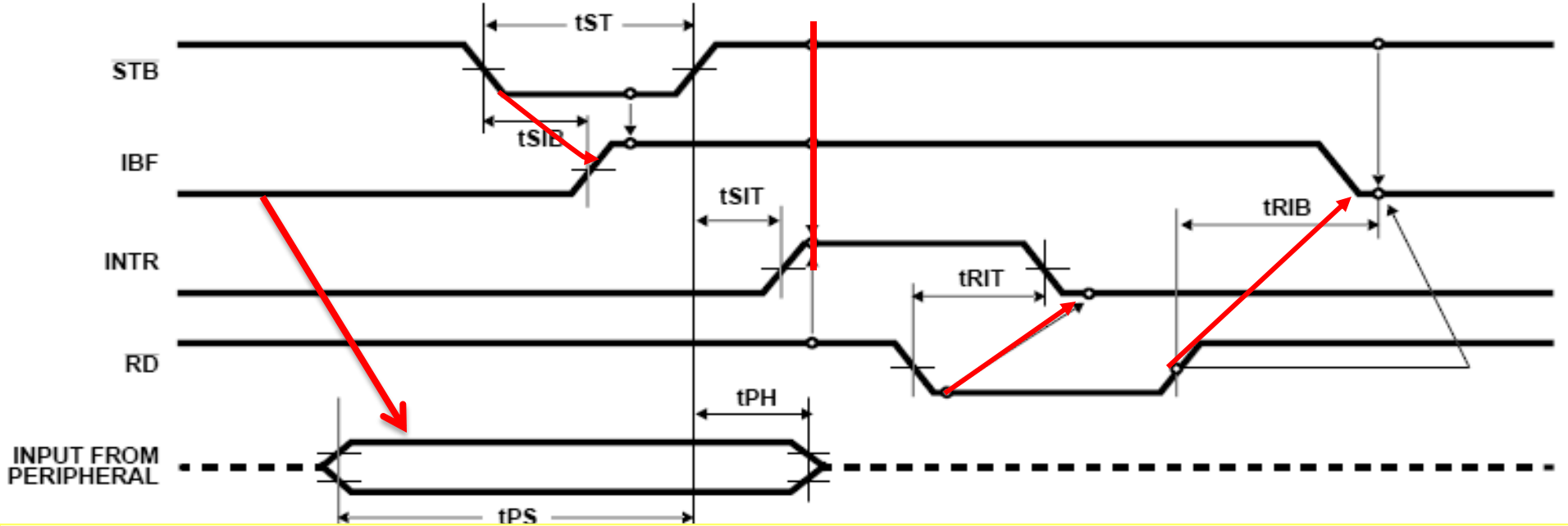


Mode 0. Timing waveforms for Input and Output operation

Mode 1: Strobed Input/Output
(D7=1, D6=0, D5=D2=1)



A,C ports configuration for Input and Output operations



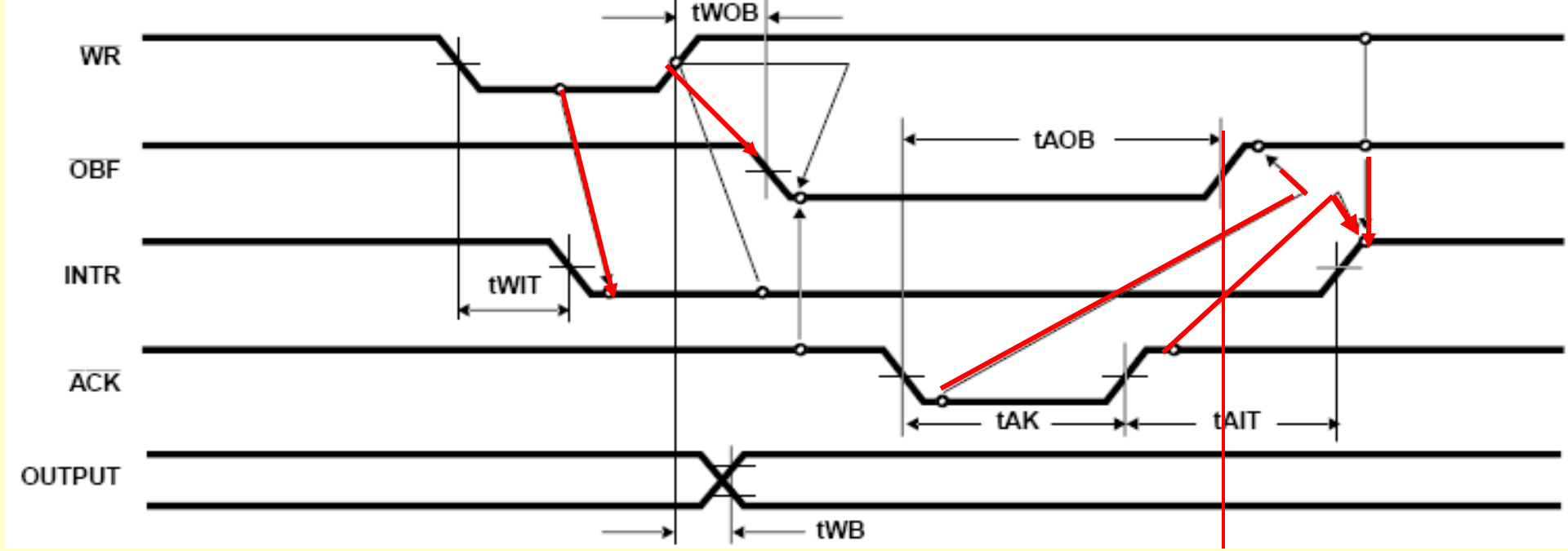
Input Control Signal Definition

STB (Strobe Input)
A “low” on this input loads data into the input latch

IBF (Input Buffer Full F/F)
A “high” on this output indicates that the data has been loaded into the input latch
IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)
A “high” on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: STB = IBF =1 and INTE is a “one”. It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A Controlled by bit set/reset of PC4.
INTE B Controlled by bit set/reset of PC2.



Output Control Signal Definition

-OBF - Output Buffer Full F/F. The OBF output will go “low” to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since OBF can go true before data is available. ***Data is guaranteed valid at the rising edge of OBF.*** The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

-ACK - Acknowledge Input. A “low” on this input informs the 8255A that the data from Port A /B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data.

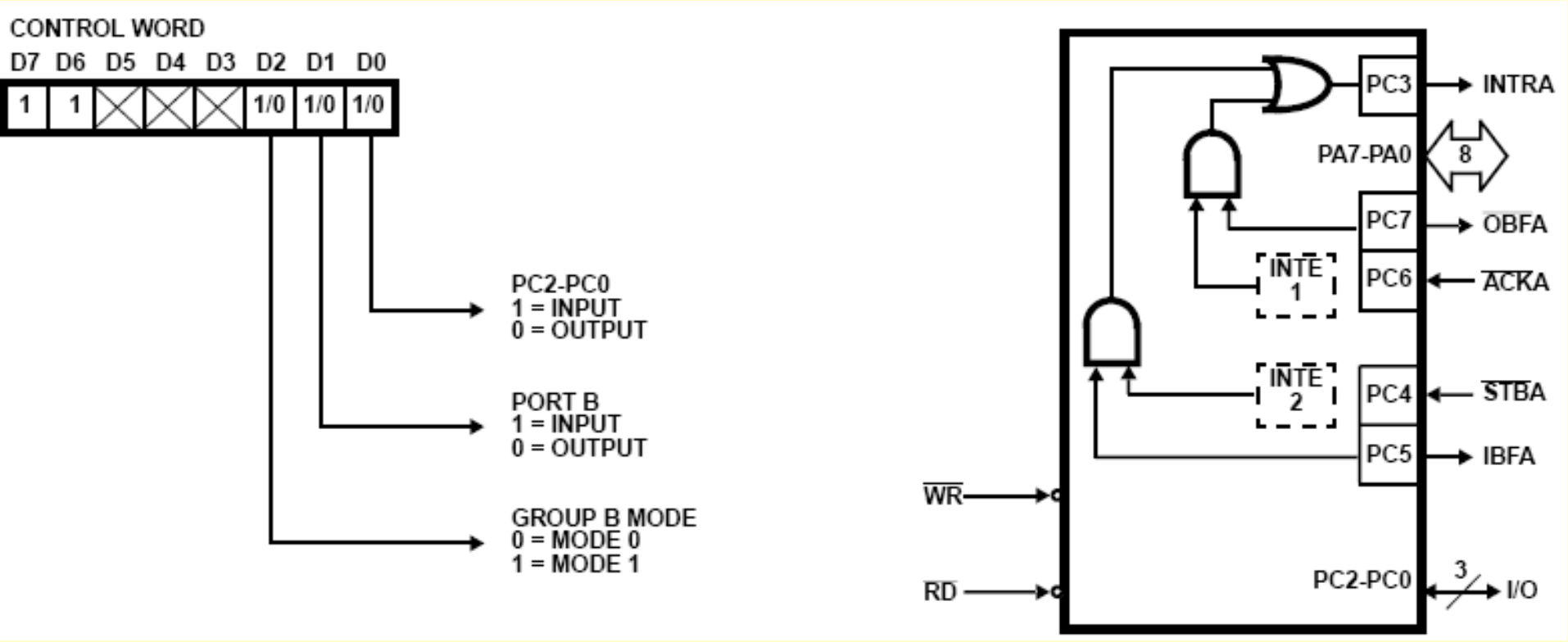
INTR - (Interrupt Request). A “high” on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK=OBF=1 and INTE=1. It is reset by the falling edge of WR.

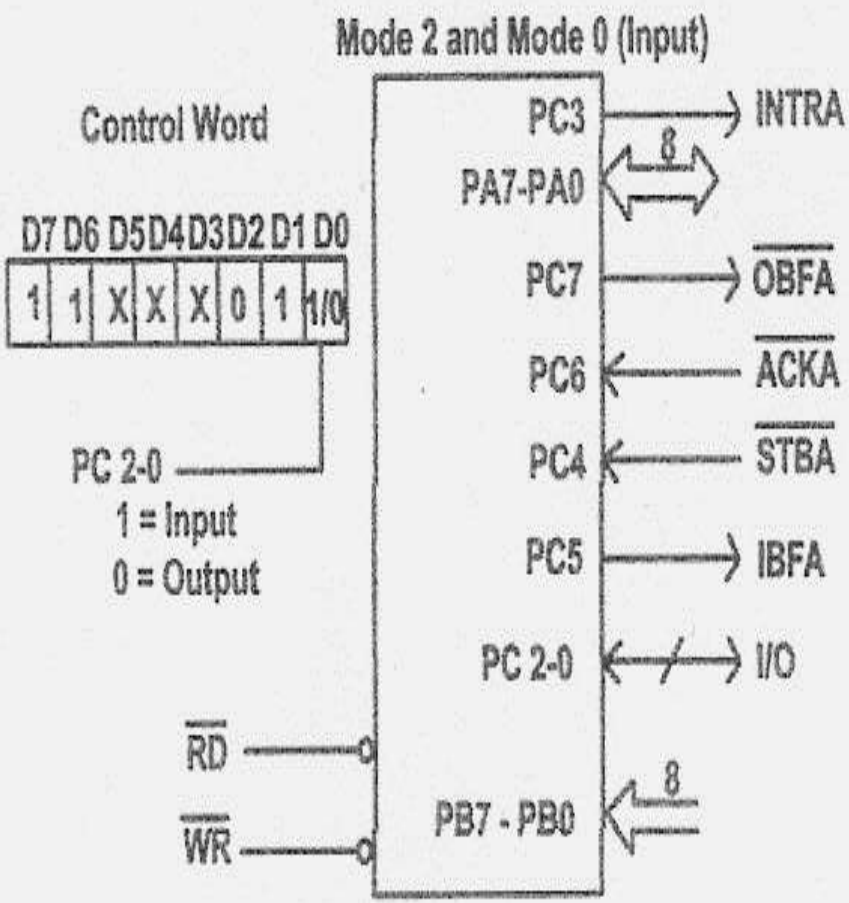
INTE A Controlled by Bit Set/Reset of PC6.
INTE B Controlled by Bit Set/Reset of PC2.

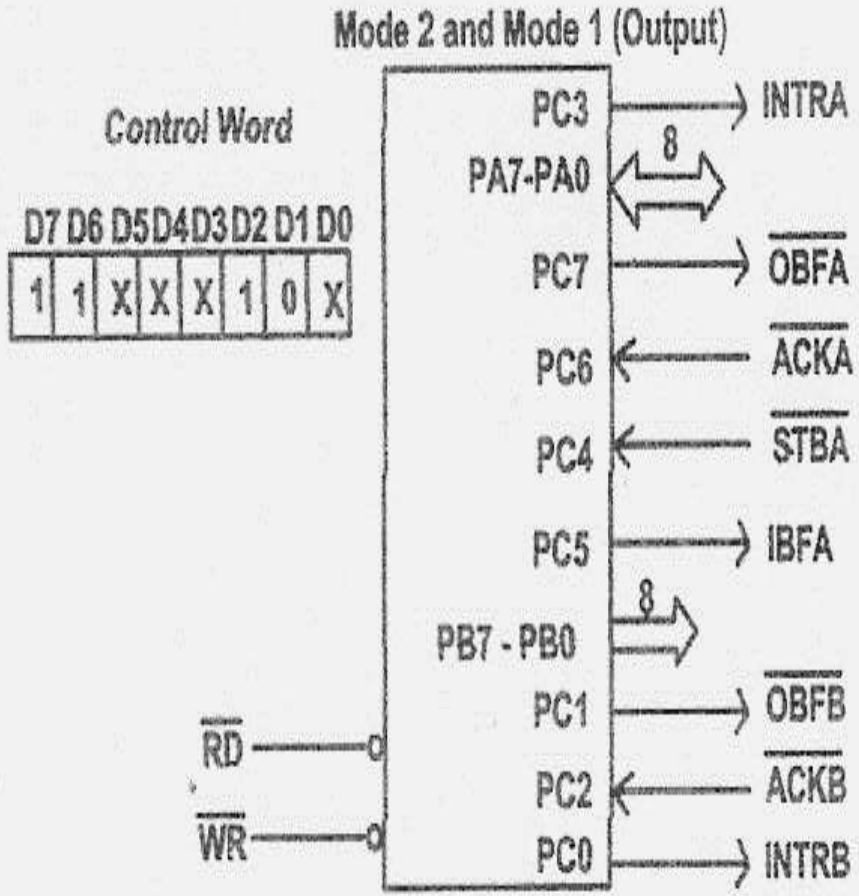
Port C with Port A & Port B Both Configured in Mode 1

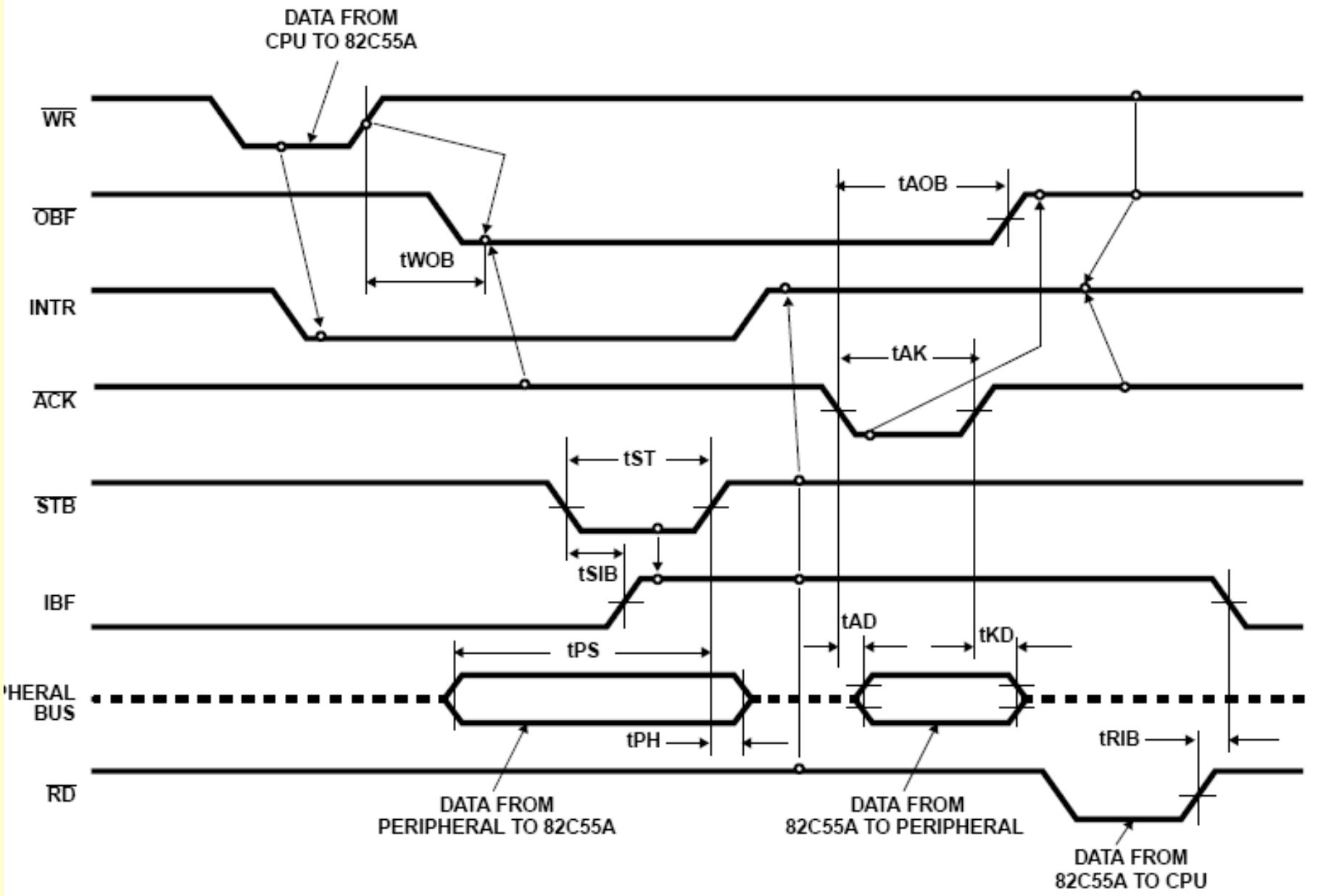
Bit	Mode 1 Input	Mode 1 Output	Description
PC0	intrb	intrb	Always output.
PC1	ibfb	-obfb	Always output.
PC2	-stbb	-ackb	Always input.
PC3	intra	intra	Always output.
PC4	-stba	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC5	ibfa	I/O	I/O direction configured by bit 3 of the control register in “mode 1 output.”
PC6	I/O	-acka	I/O direction configured by bit 3 of the control register in “mode 1 input.”
PC7	I/O	-obfa	I/O direction configured by bit 3 of the control register in “mode 1 input.”

Mode 2: Strobed Bidirectional Bus
(D7=1, D6=1, D5=D2=XX)



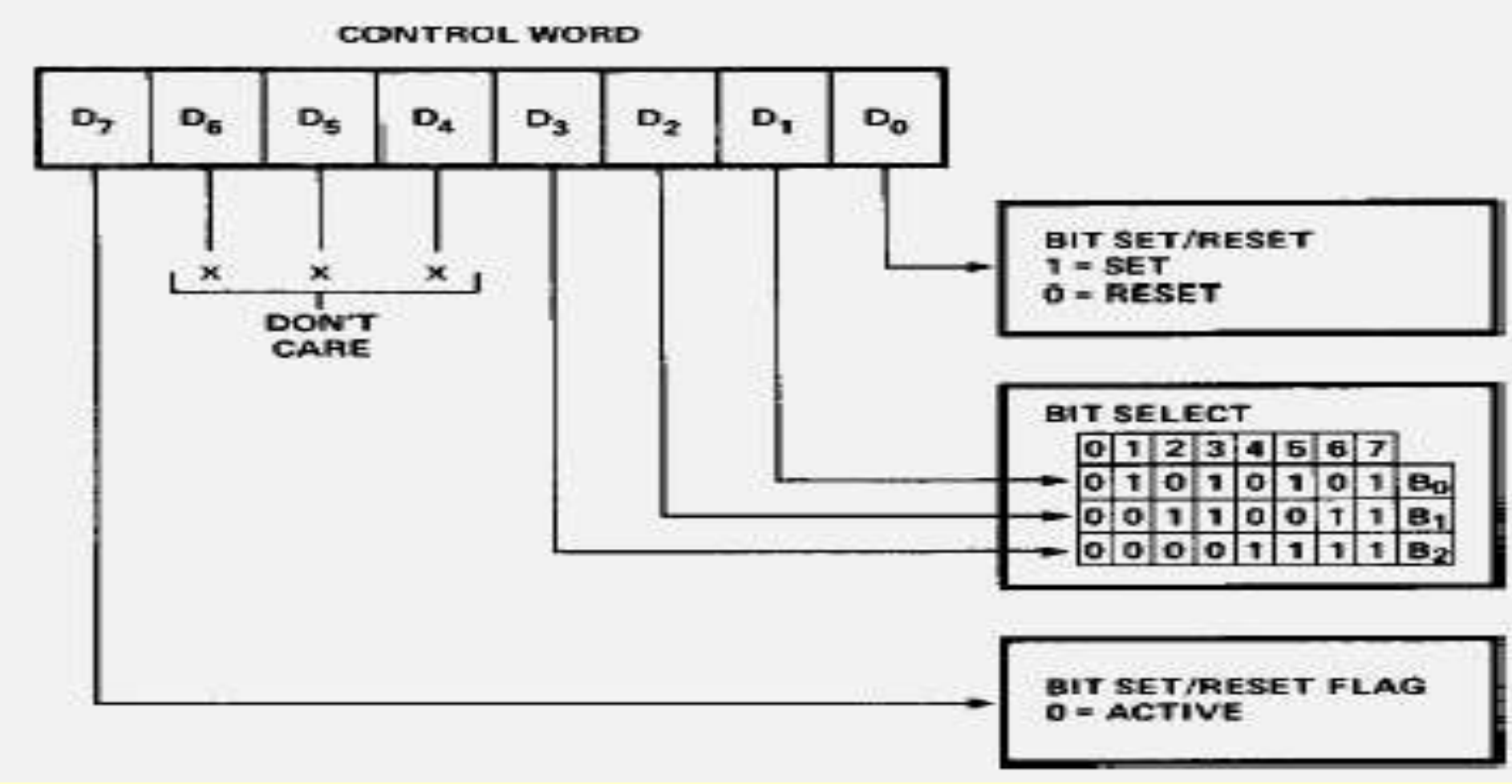

Mode 2 and Mode 0 (Input)
Control Word
D7 D6 D5 D4 D3 D2 D1 D0
1 1 X X X 0 1 1/0
PC 2-0
1 = Input
0 = Output
PC3
INTRA
8
PA7-PA0
PC7
OBFA
PC6
ACKA
PC4
STBA
PC5
IBFA
PC 2-0
I/O
RD
WR
8
PB7 - PB0


Mode 2 and Mode 1 (Output)
Control Word
D7 D6 D5 D4 D3 D2 D1 D0
1 1 X X X 1 0 X
PC3
INTRA
8
PA7-PA0
PC7
OBFA
PC6
ACKA
PC4
STBA
PC5
IBFA
8
PB7 - PB0
PC1
OBFB
PC2
ACKB
PC0
INTRB
RD
WR



Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

Mode 2. Timing waveforms for I/O operations

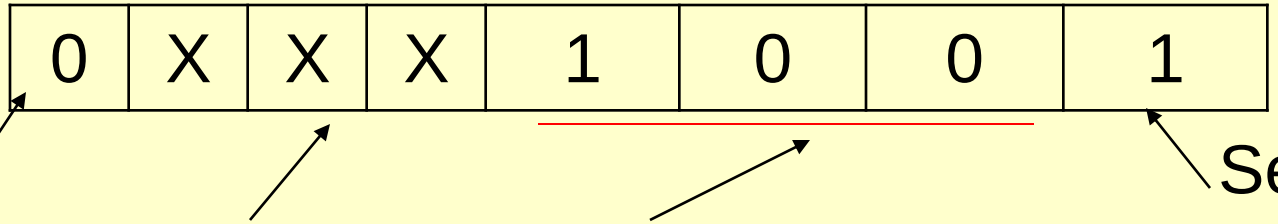


C port bits set/reset

1 = I / O Mode

0 = BSR Mode

Ex. 1: Set to 1 bit 4 of Port C



Required instructions

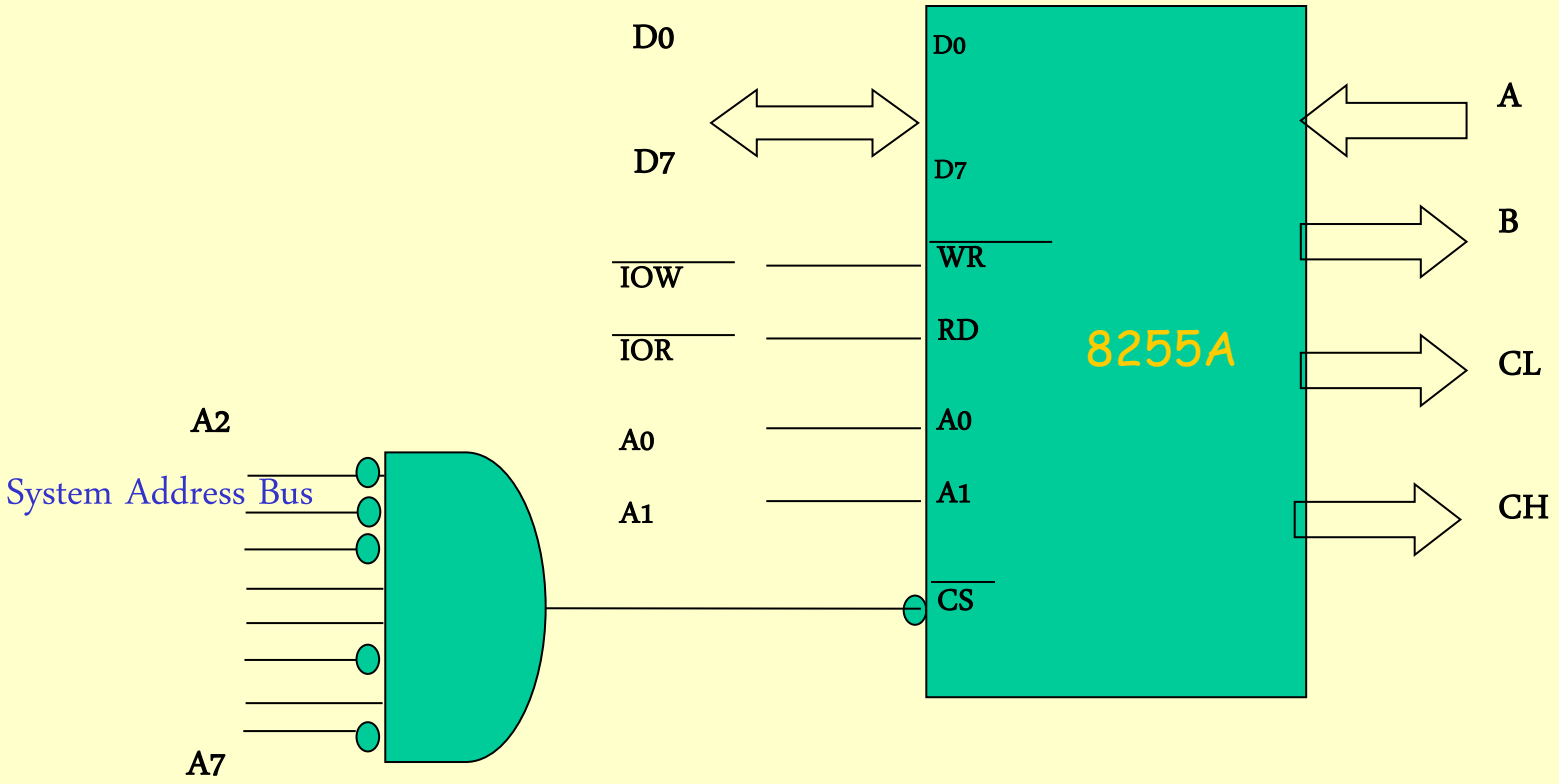
MOV AL, 09H

OUT 7FH, AL

8255 Mode Definition Summary

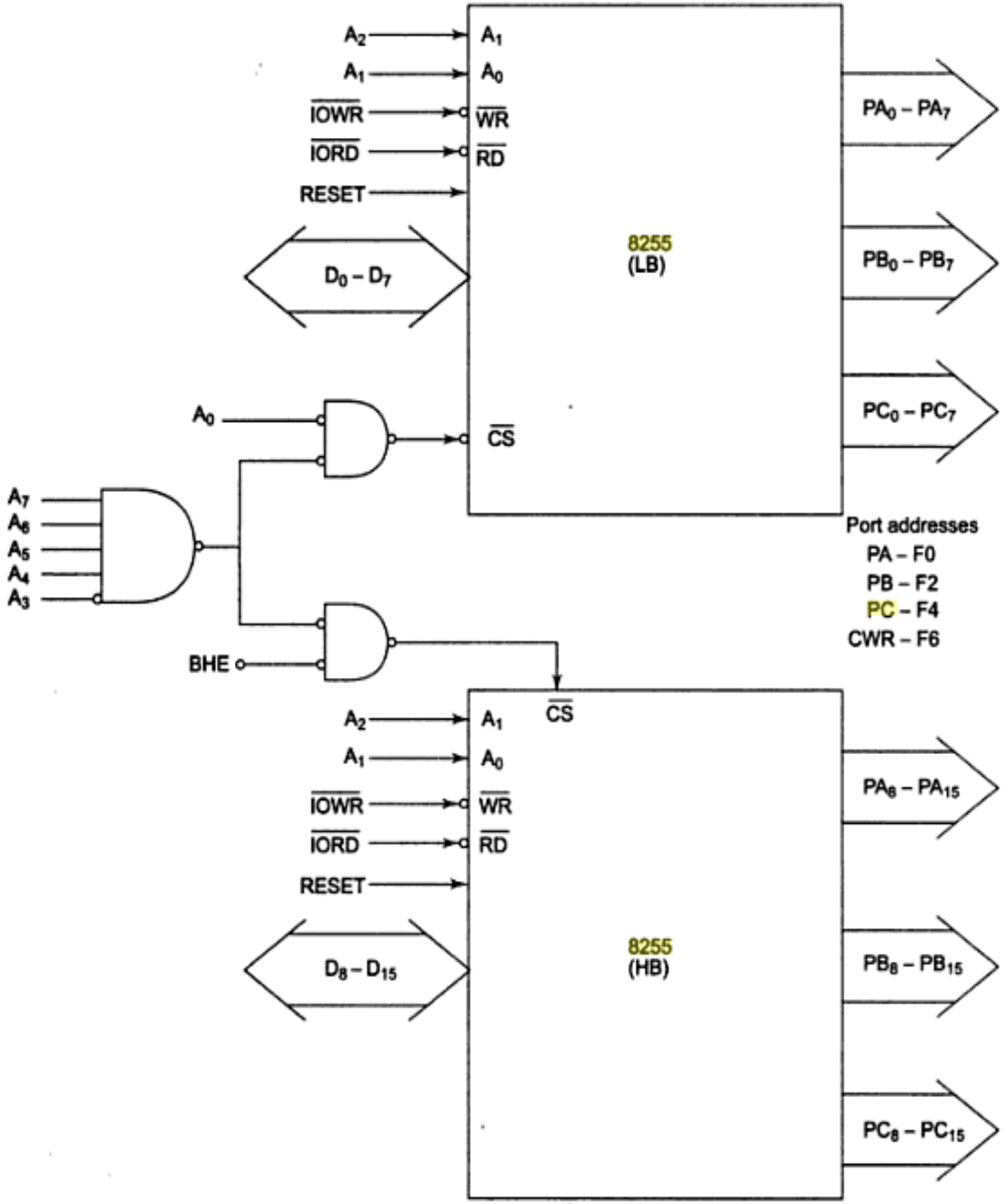
	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	⟷
PA_1	IN	OUT	IN	OUT	⟷
PA_2	IN	OUT	IN	OUT	⟷
PA_3	IN	OUT	IN	OUT	⟷
PA_4	IN	OUT	IN	OUT	⟷
PA_5	IN	OUT	IN	OUT	⟷
PA_6	IN	OUT	IN	OUT	⟷
PA_7	IN	OUT	IN	OUT	⟷
PB_0	IN	OUT	IN	OUT	—
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

PIO Applications. 16 bits ports design using PIO.

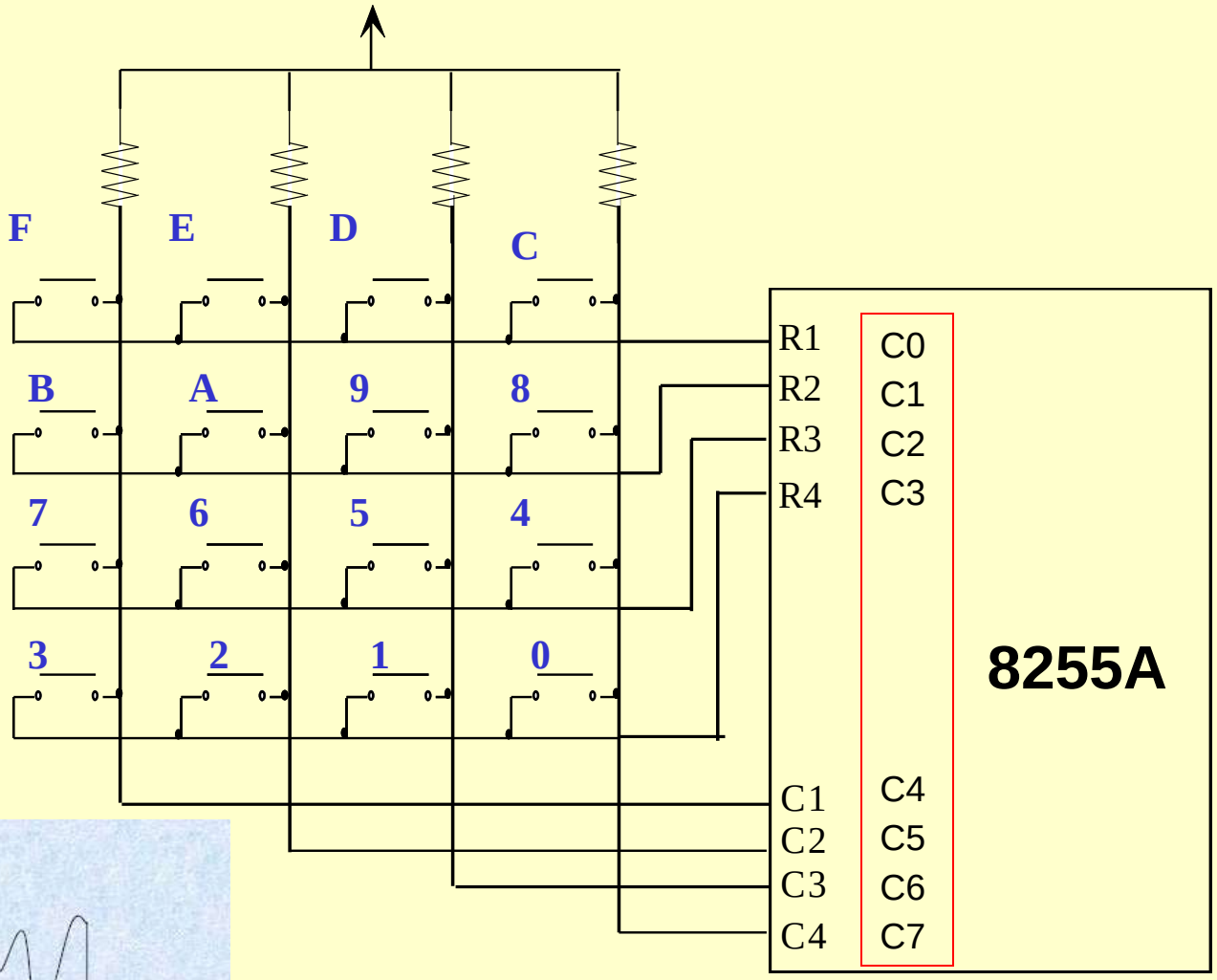


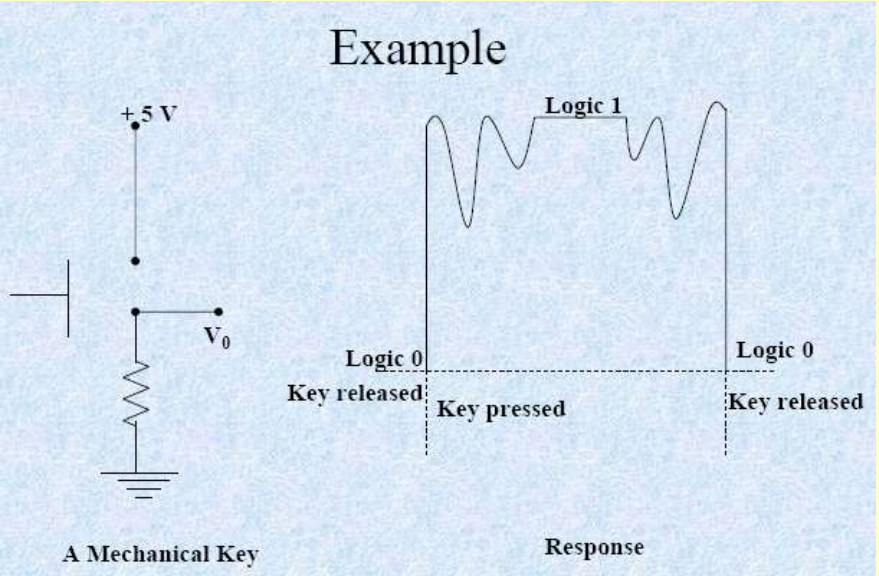
Problem.
Interface 16-bit 8255 ports with 8086.
The address of port A is F0h.

Solution. To implement a 16bit port, 2x8255s are required. One will act as the lower 8bit port (D0-D7) , while the other will act as the upper 8 bit port D8-D15.
The overall scheme is as shown in the next fig.
While initialising AL and AH (AX) both should be loaded with suitable (common) control words. In this system port A, port B and port C all may work as 16-bit ports.

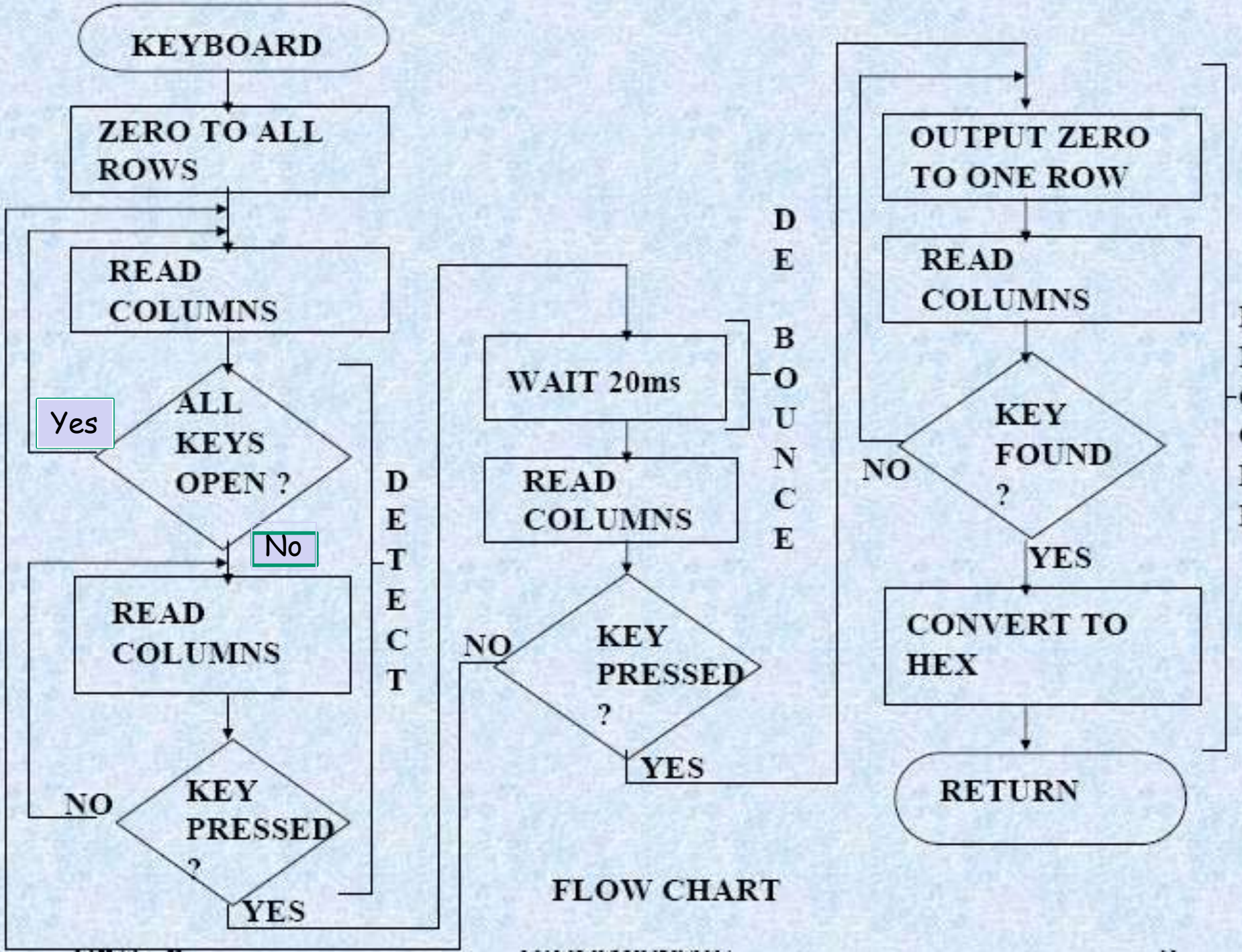


Interfacing 16-bit 8255 Ports with 8086



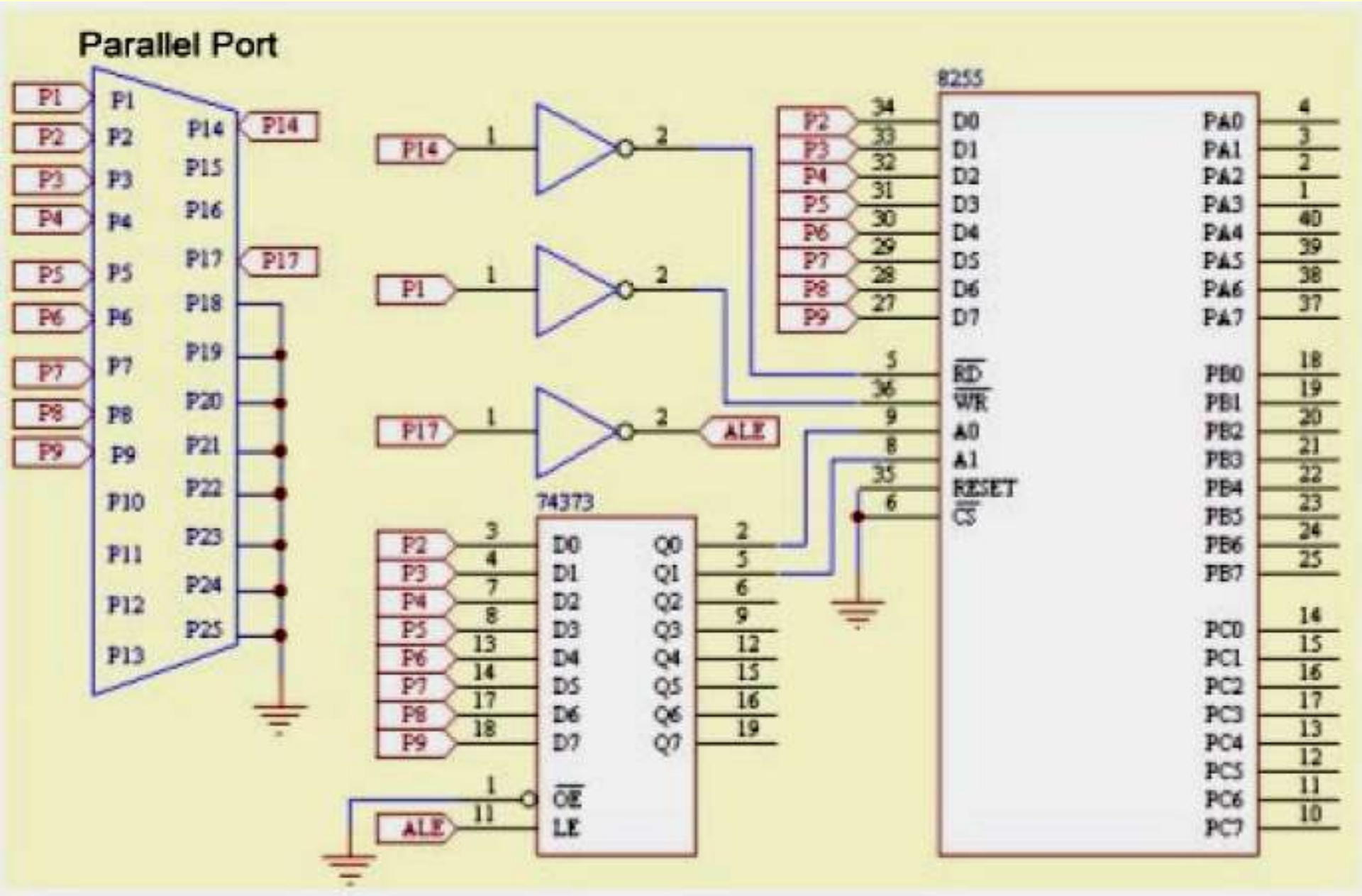


HW1. **Write an application which provide in AL the pressed key code.**

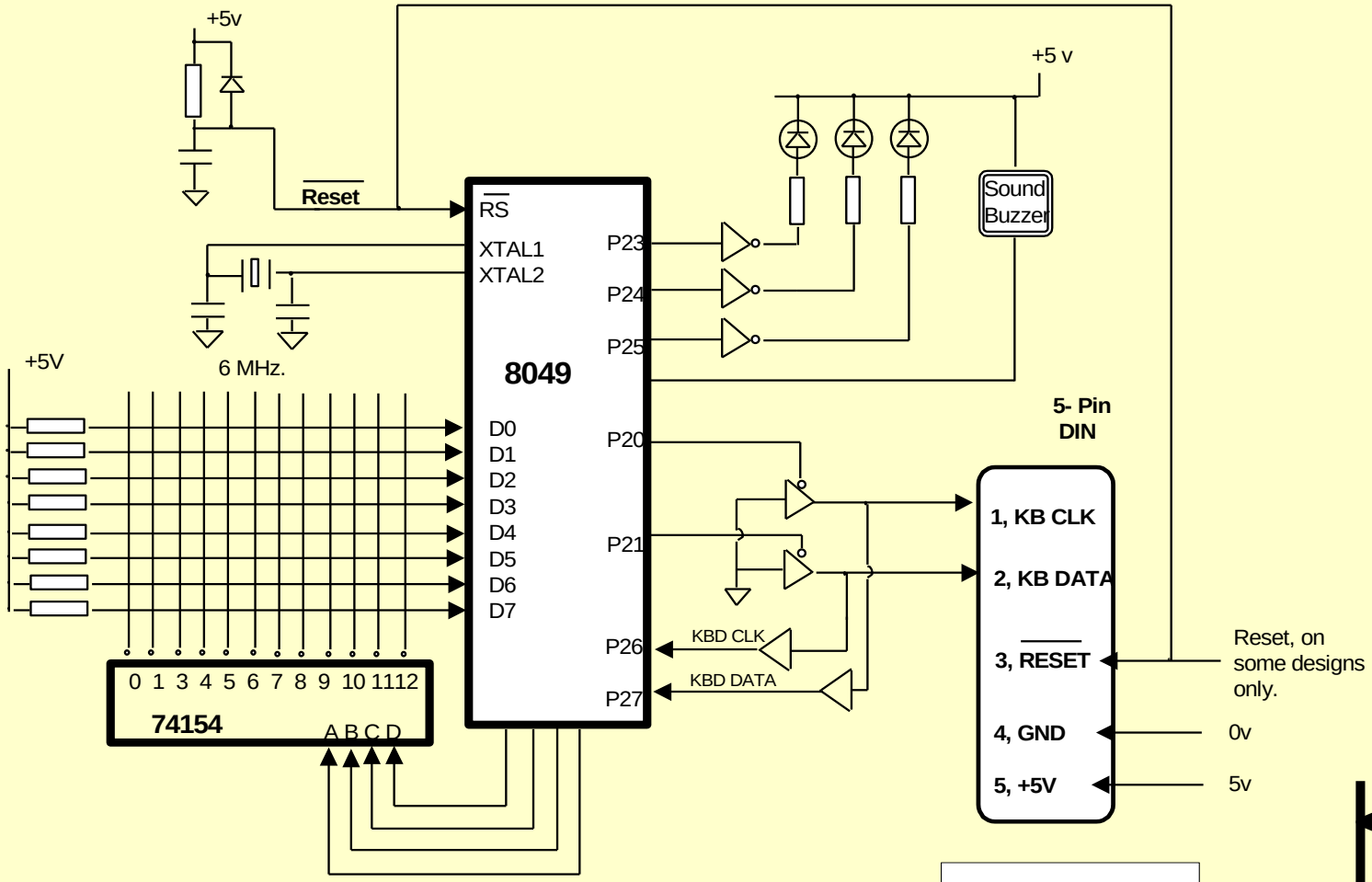

KEYBOARD
ZERO TO ALL ROWS
READ COLUMNS
ALL KEYS OPEN ?
Yes
No
READ COLUMNS
KEY PRESSED ?
NO
YES
DETECT
WAIT 20ms
READ COLUMNS
KEY PRESSED ?
NO
YES
DEBOUNCE
OUTPUT ZERO TO ONE ROW
READ COLUMNS
KEY FOUND ?
NO
YES
CONVERT TO HEX
RETURN
ENCODE

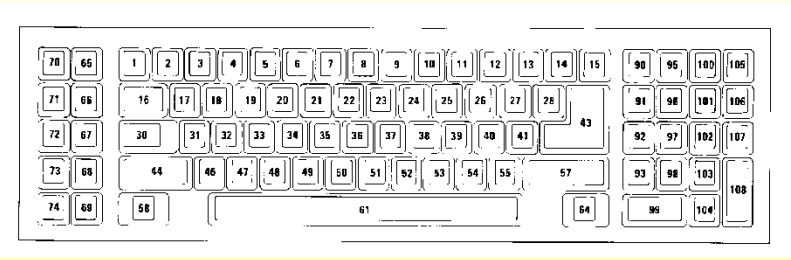
FLOW CHART

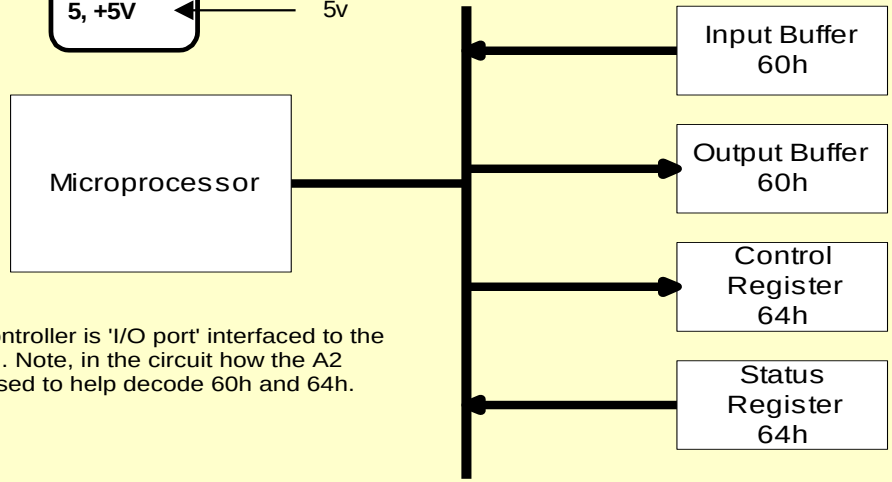
HW2. Analyze this electrical scheme and find its function.



The Keyboard Circuit

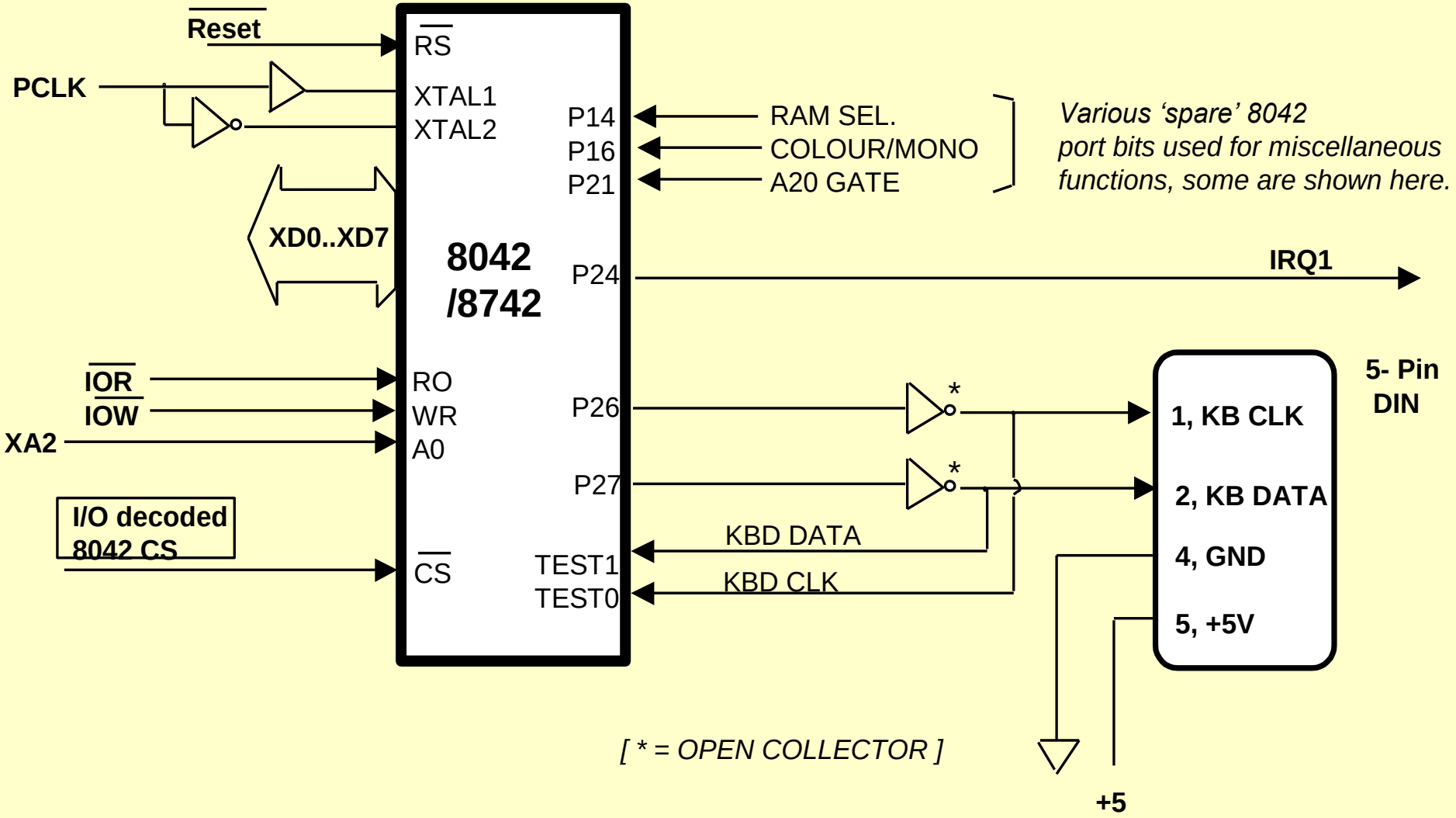






The keyboard controller is 'I/O port' interfaced to the PC/AT as shown. Note, in the circuit how the A2 address line is used to help decode 60h and 64h.

The Key Board Controller



DISTR, DOSTR = Data Input and Data Output Strobes.