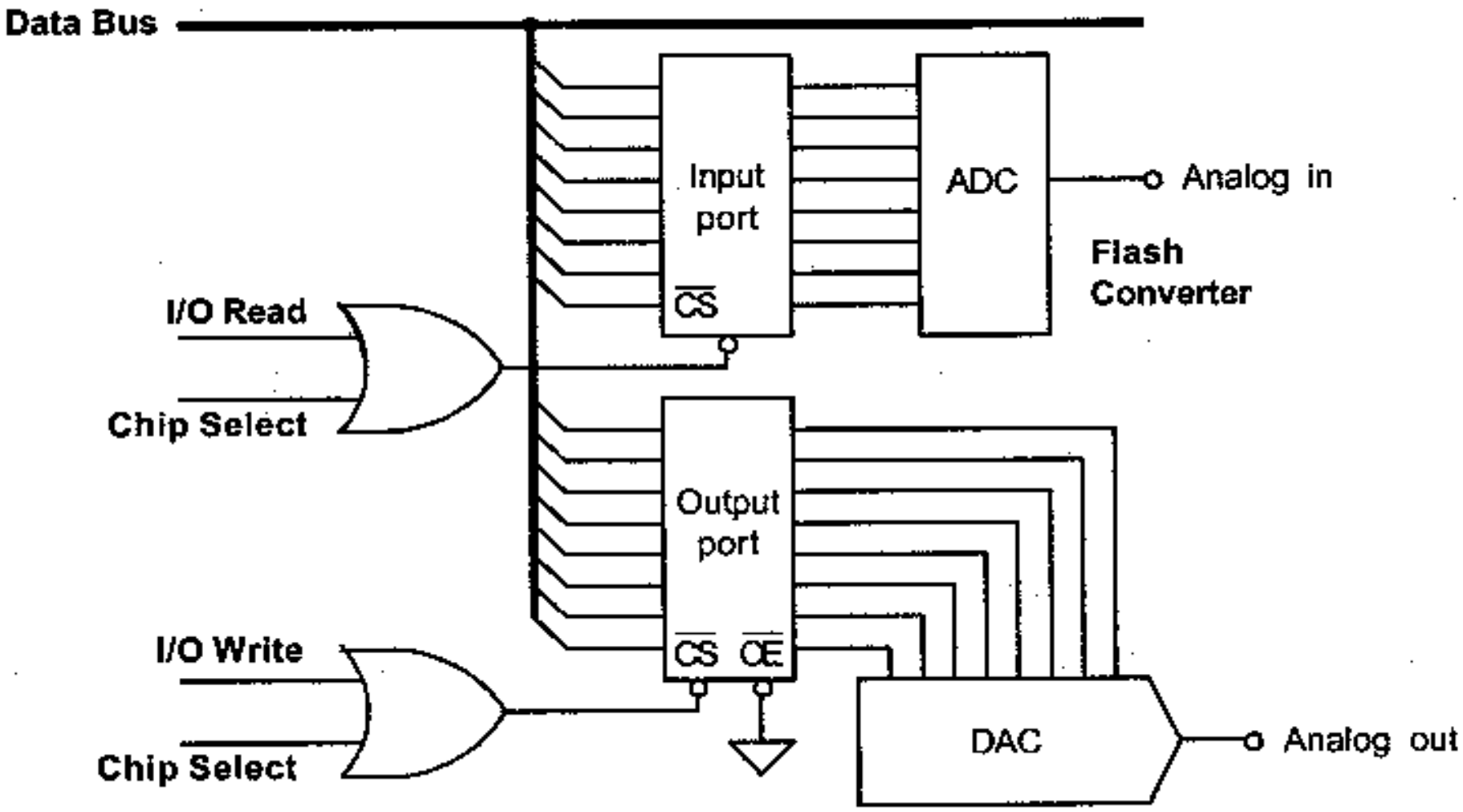
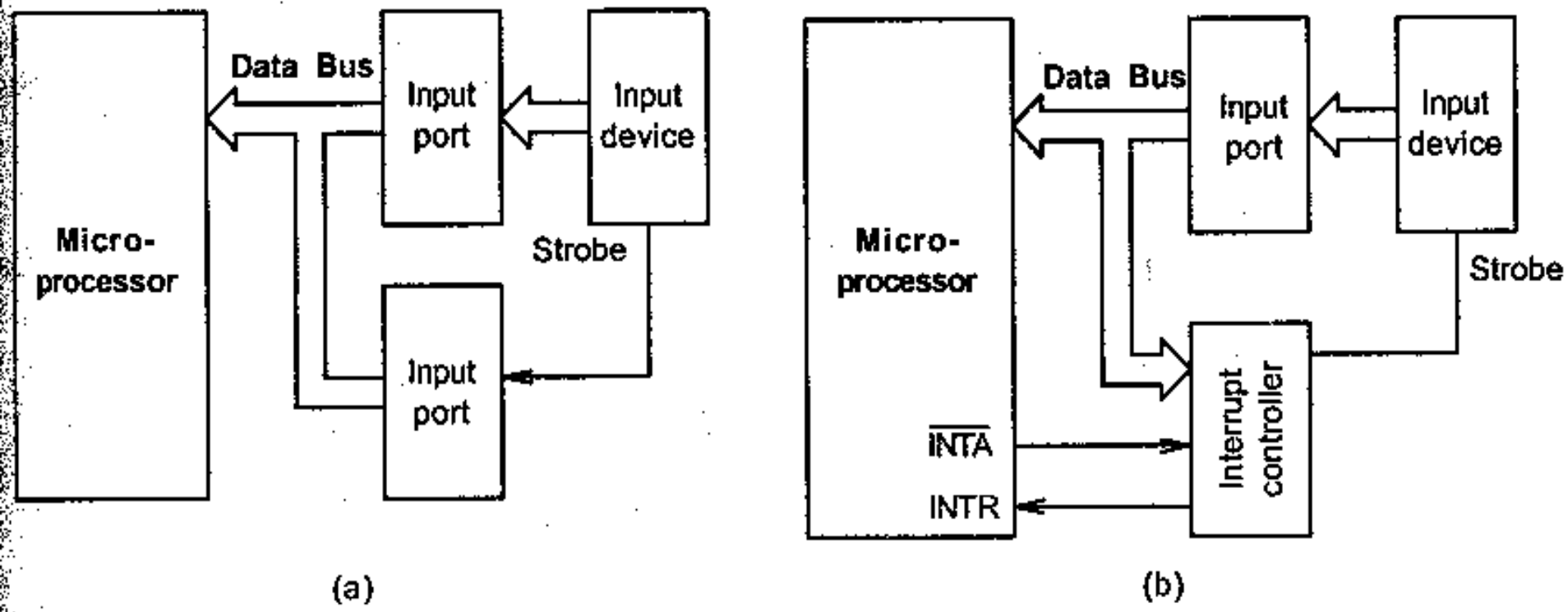
Aplicatii

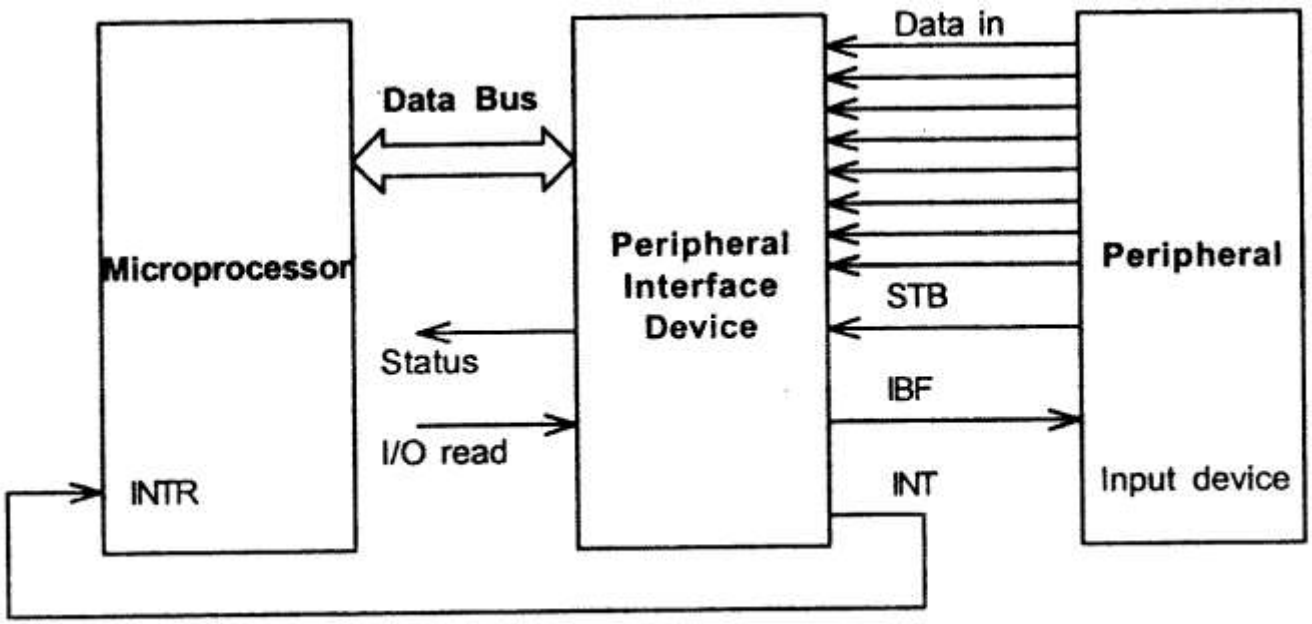
Conectarea CNA/CAN la sisteme cu Microprocesor



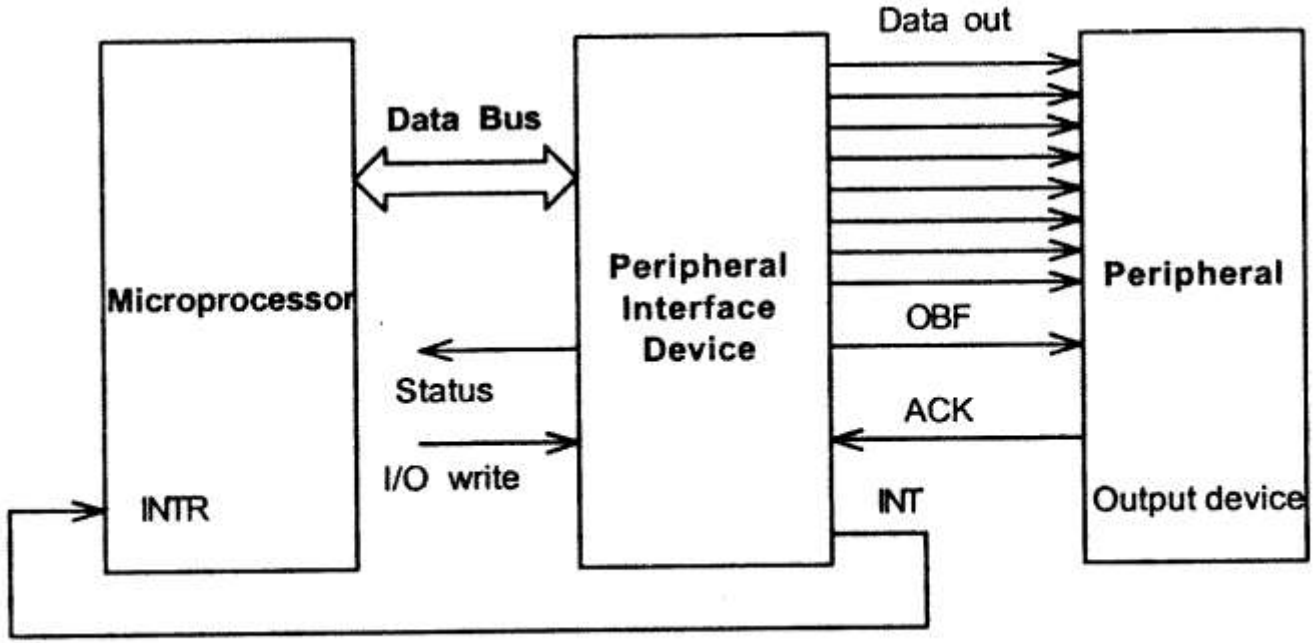
Data transfer by simple I/O.



Strobe I/O—(a) polling, (b) interrupt.



(a)



(b)

Handshake I/O—(a) input operation, (b) output operation.

ADConverter - AD 574A

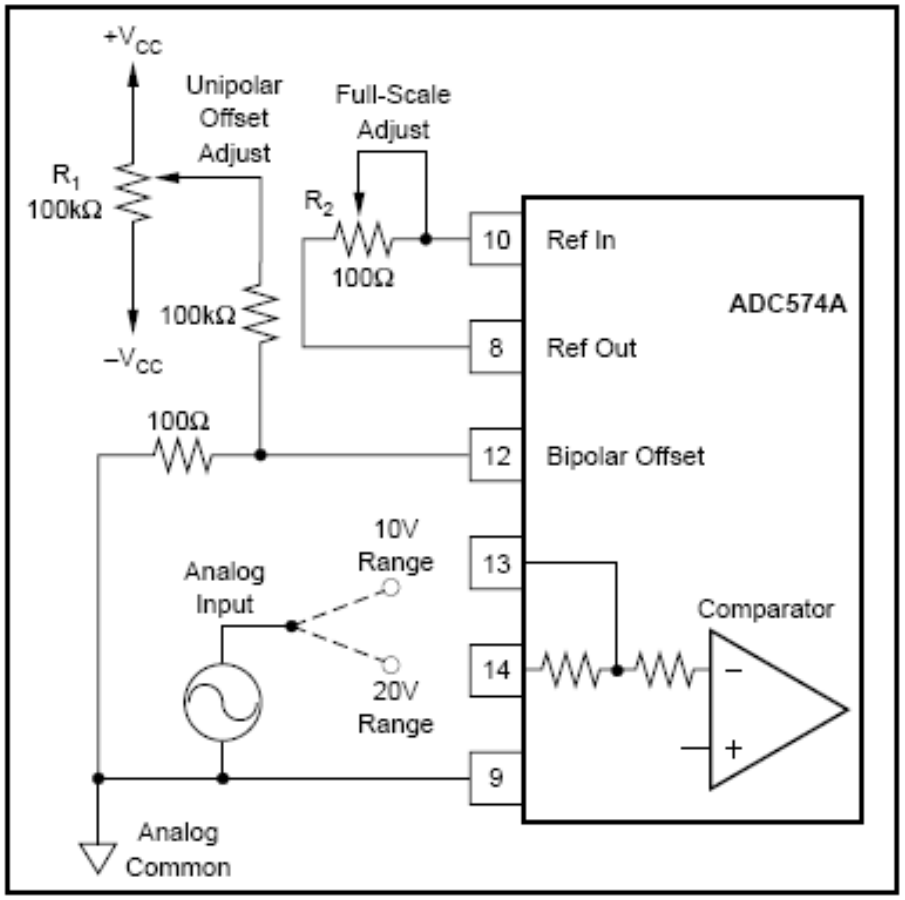


FIGURE 2. Unipolar Configuration.

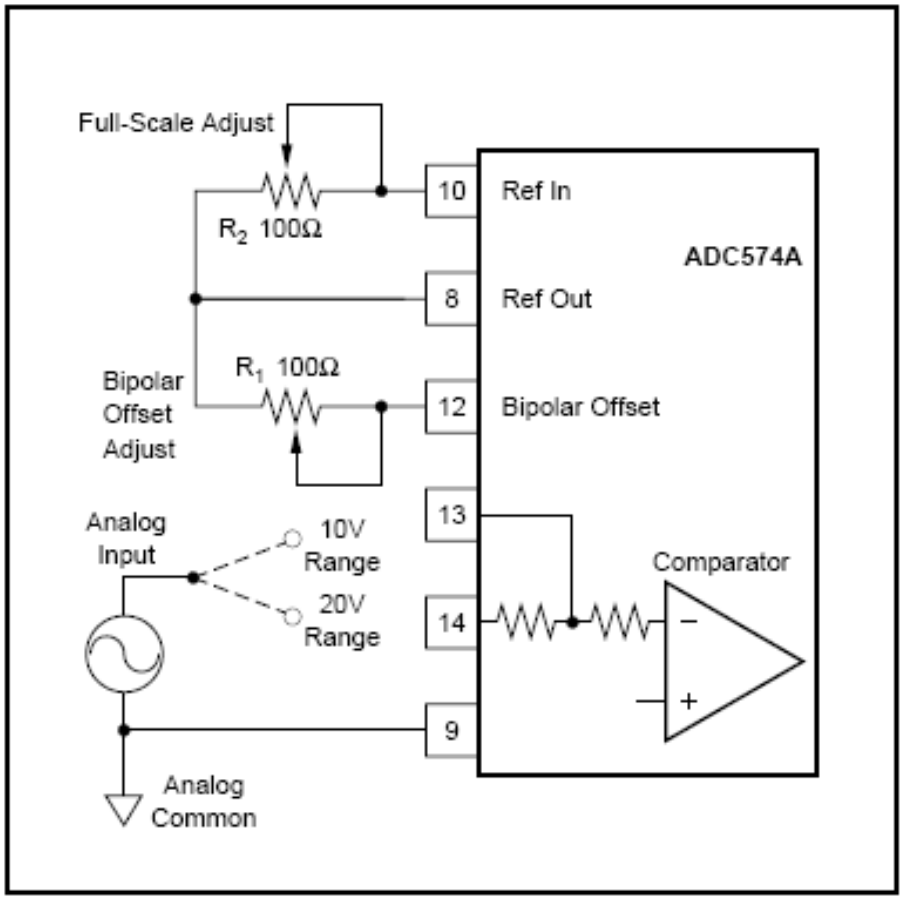
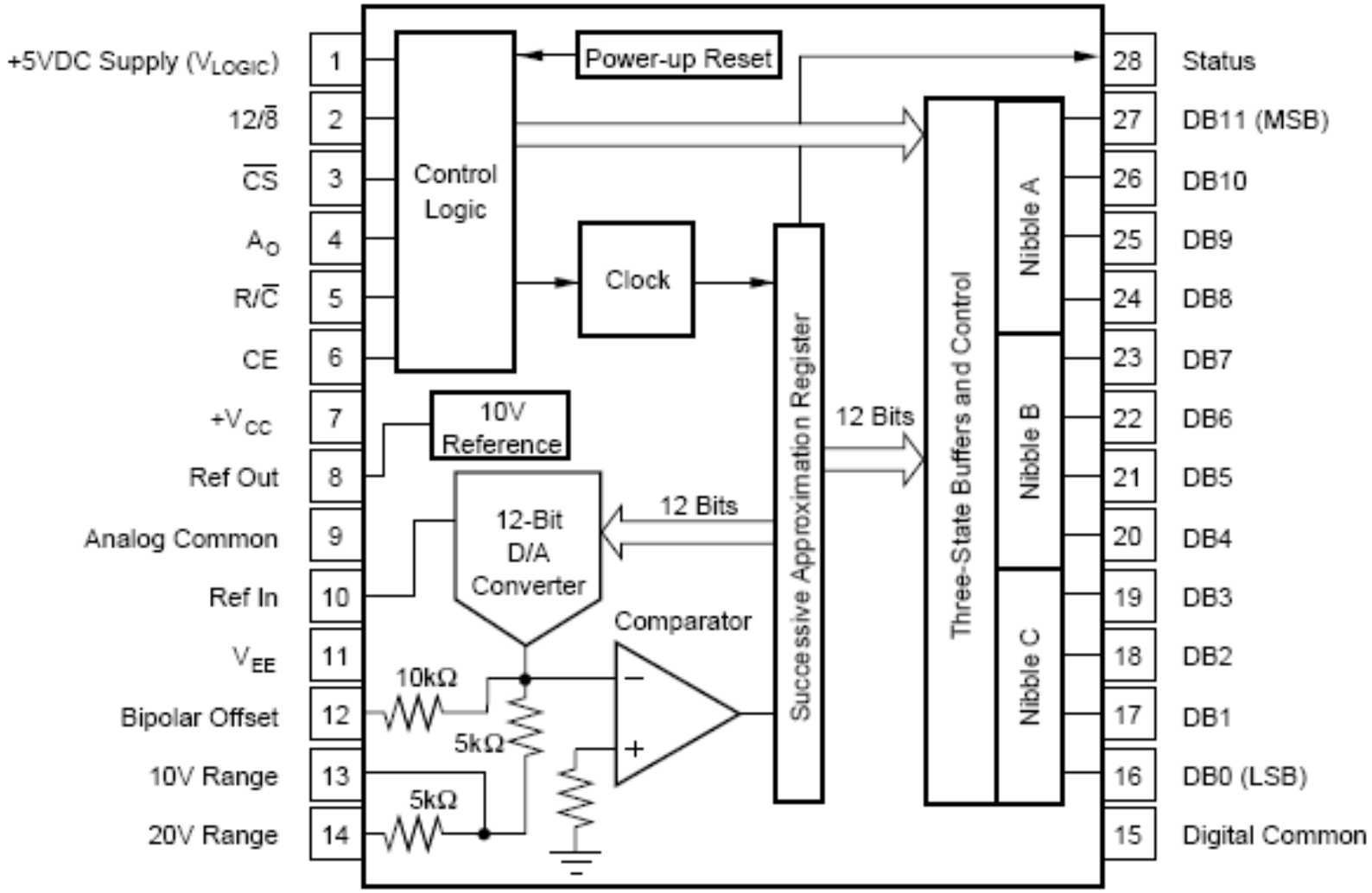


FIGURE 3. Bipolar Configuration.

PIN CONFIGURATION



CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

2

1

TABLE III. Control Input Truth Table.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

PIN DESIGNATION	DEFINITION	FUNCTION
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion.
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion.
R/$\overline{C}$(Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8- or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation.
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte).
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSBs or LSBs as determined by the A_0 line.

TABLE II. ADC574A Control Line Functions.

CONVERSION TIME (4)							
8-Bit Cycle	10	13	17	*	*	*	µs
12-Bit Cycle	15	20	25	*	•	•	µs

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HS}	STS Delay After Data Valid	300	400	1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

TABLE IV. Stand-Alone Mode Timing.

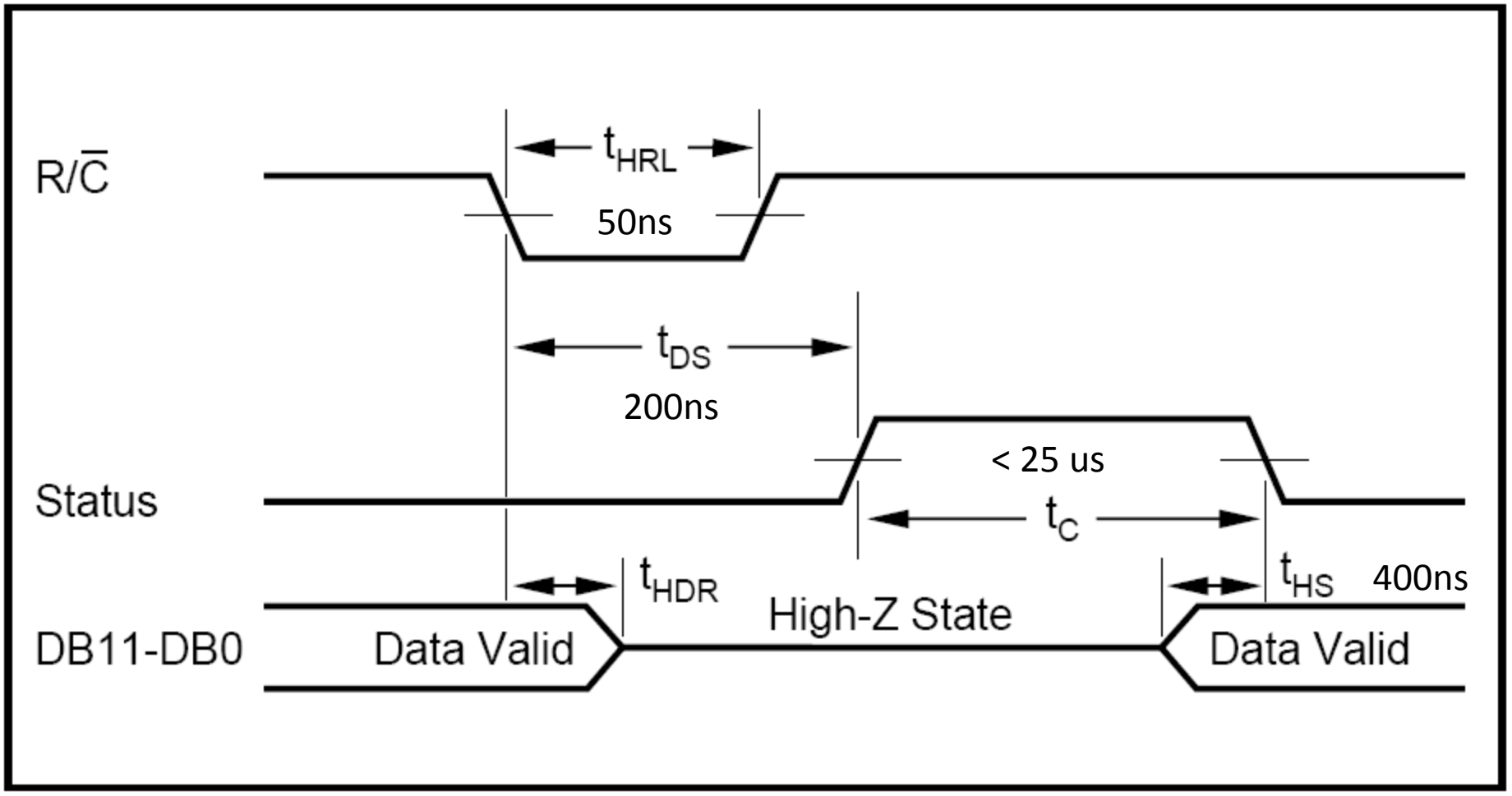


FIGURE 4. R/$\overline{C}$ Pulse Low—Outputs Enabled After Conversion.

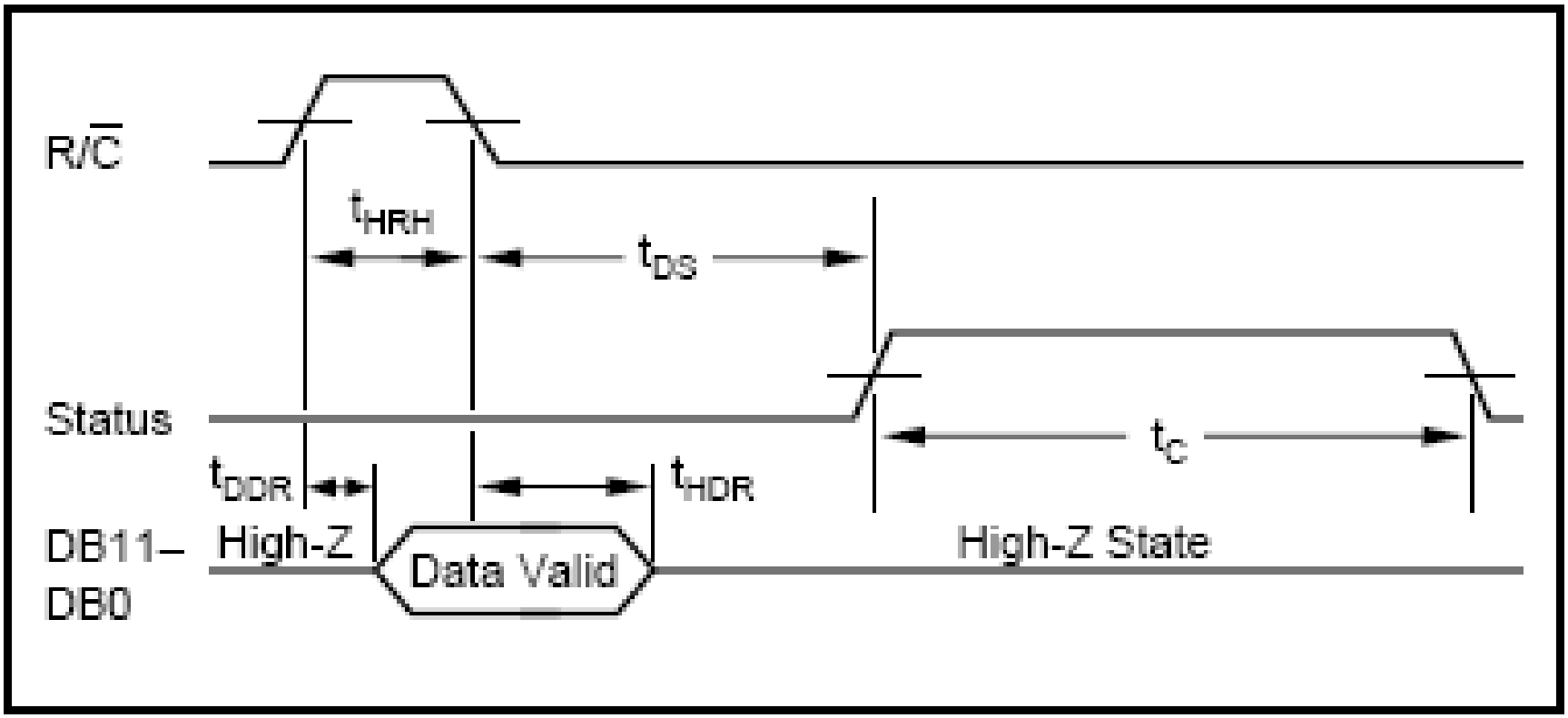
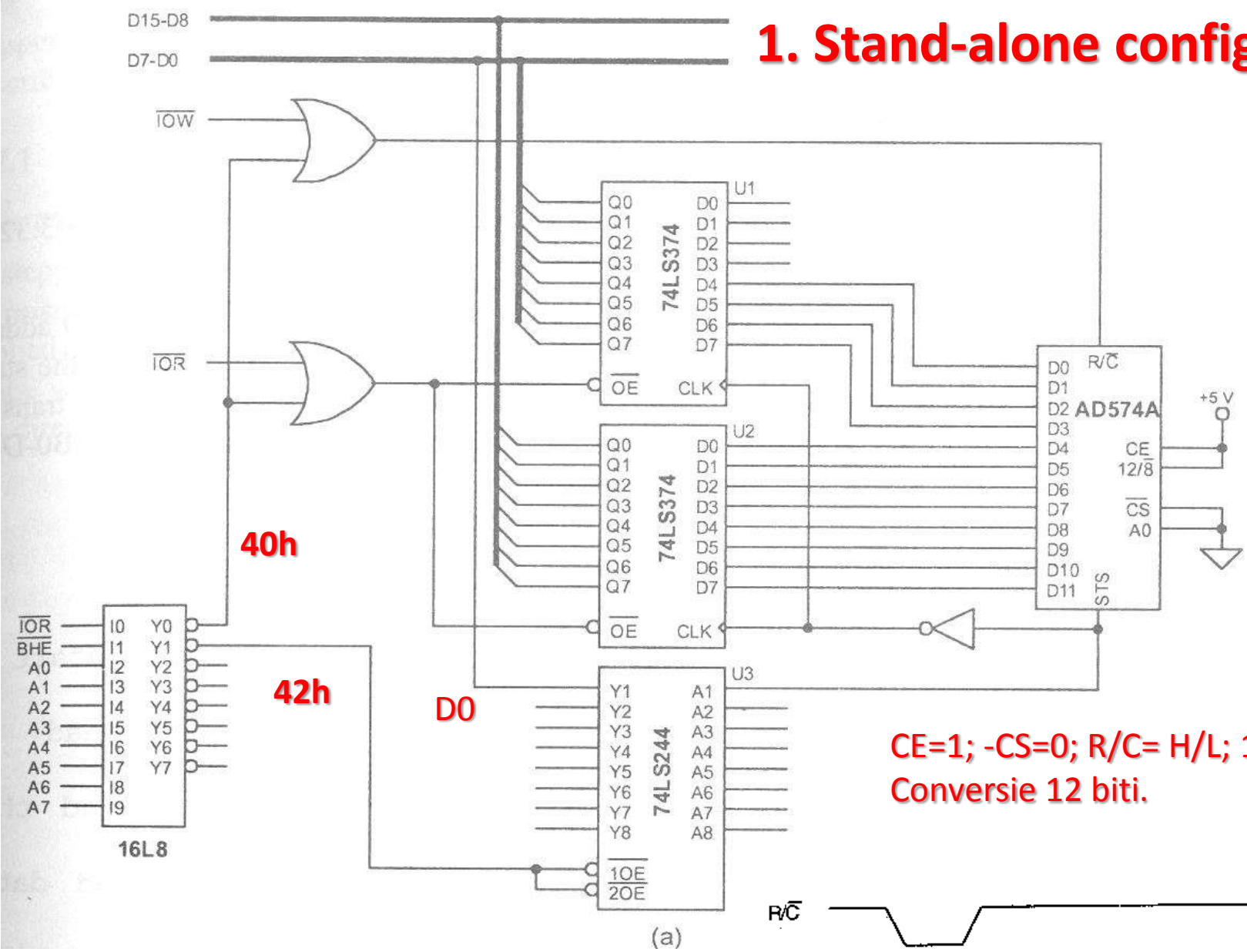
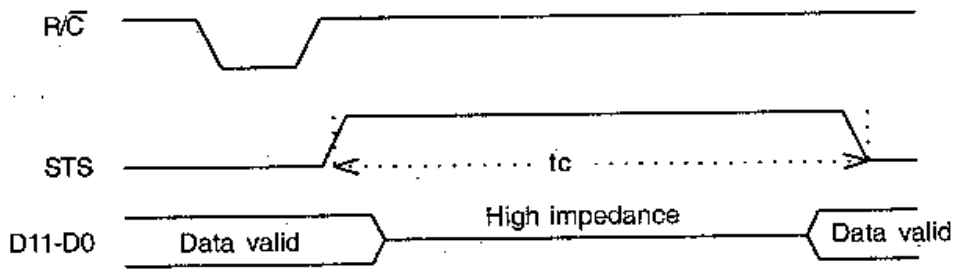


FIGURE 5. R/$\overline{C}$ Pulse High—Outputs Enabled Only While R/$\overline{C}$ Is High.

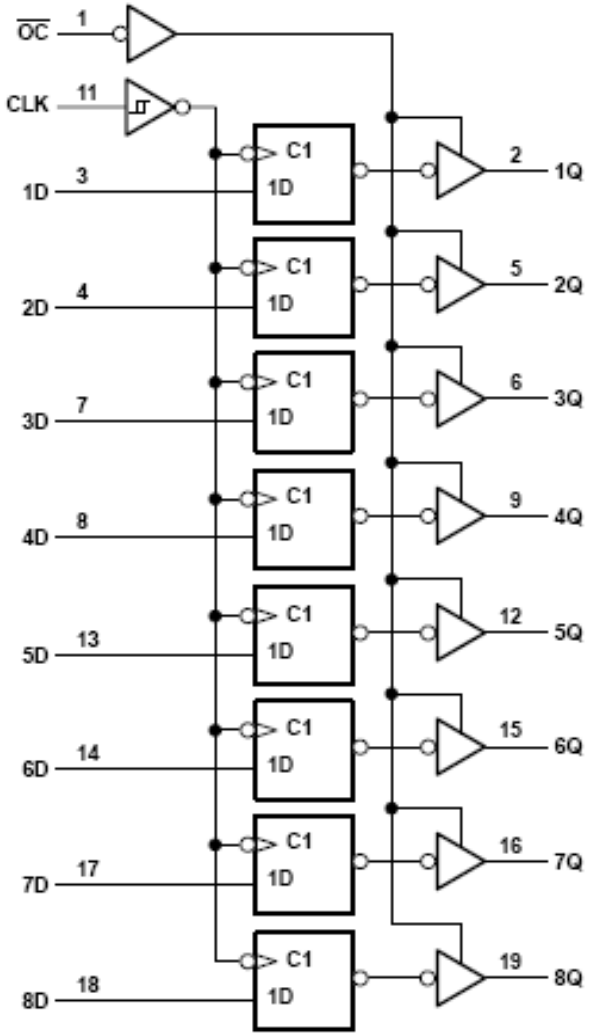
1. Stand-alone configuration



CE=1; -CS=0; R/C= H/L; 12/8=x; A0=0
Conversie 12 biti.

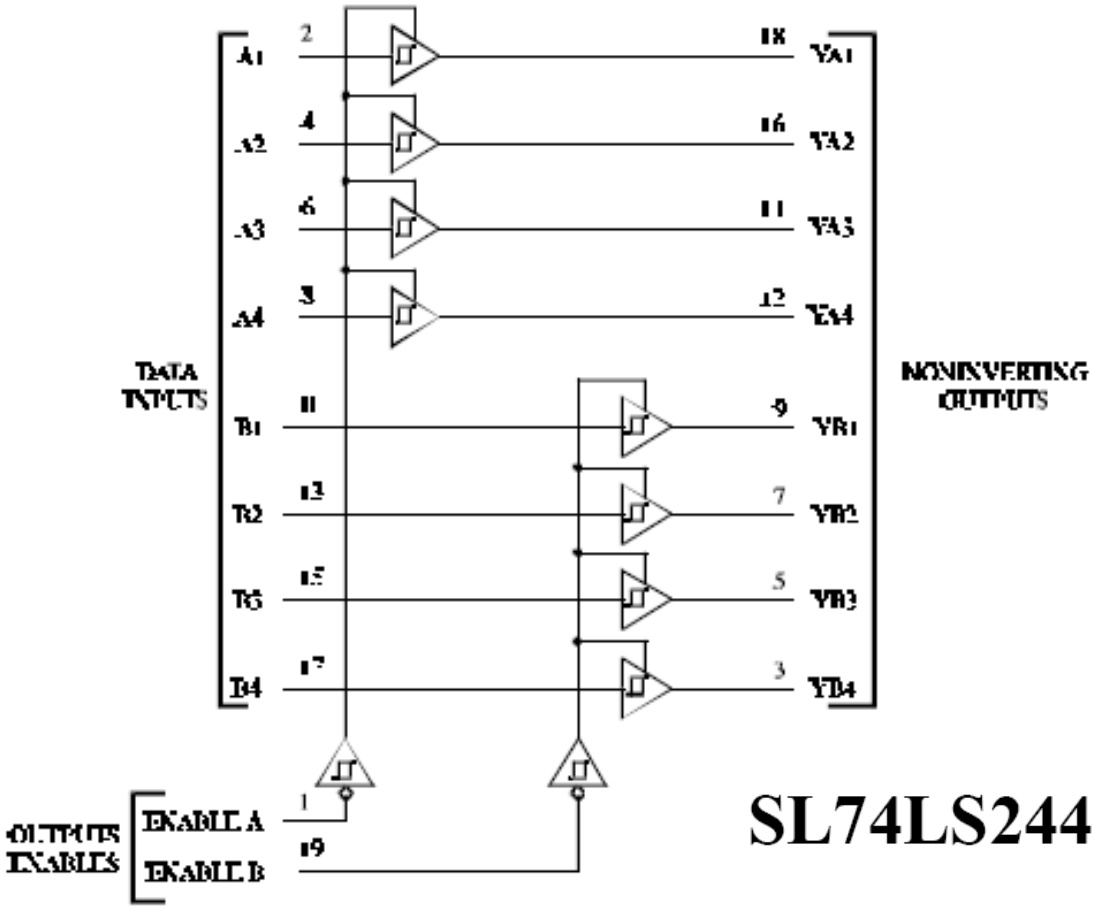


'LS374, 'S374
Positive-Edge-Triggered Flip-Flops



'LS374, 'S374
(each latch)

INPUTS			OUTPUT
$\overline{OC}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

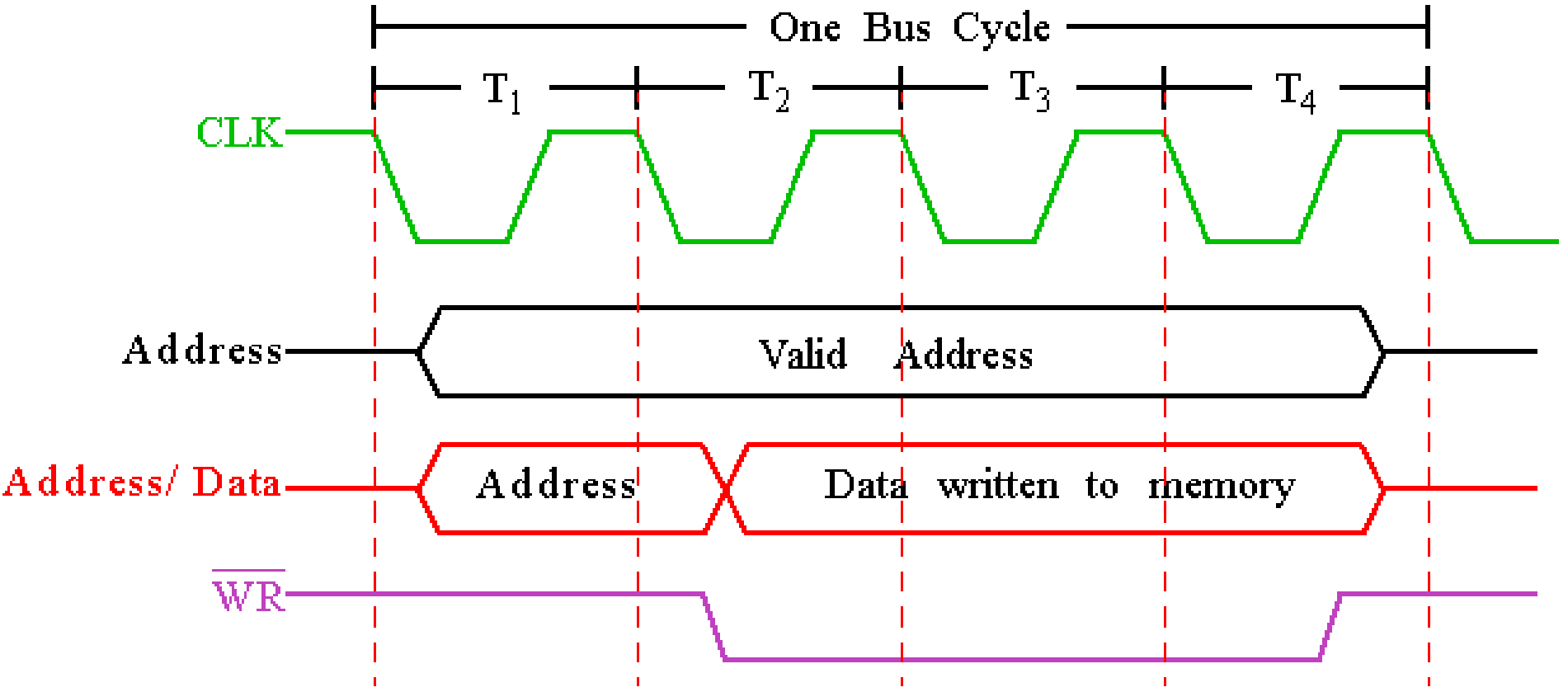


SL74LS244

FUNCTION TABLE

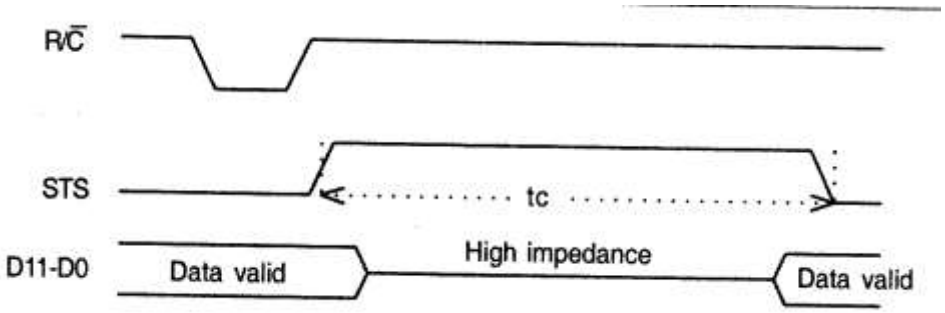
Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	L
L	H	H
H	X	Z

X=don' t care
Z = high impedance



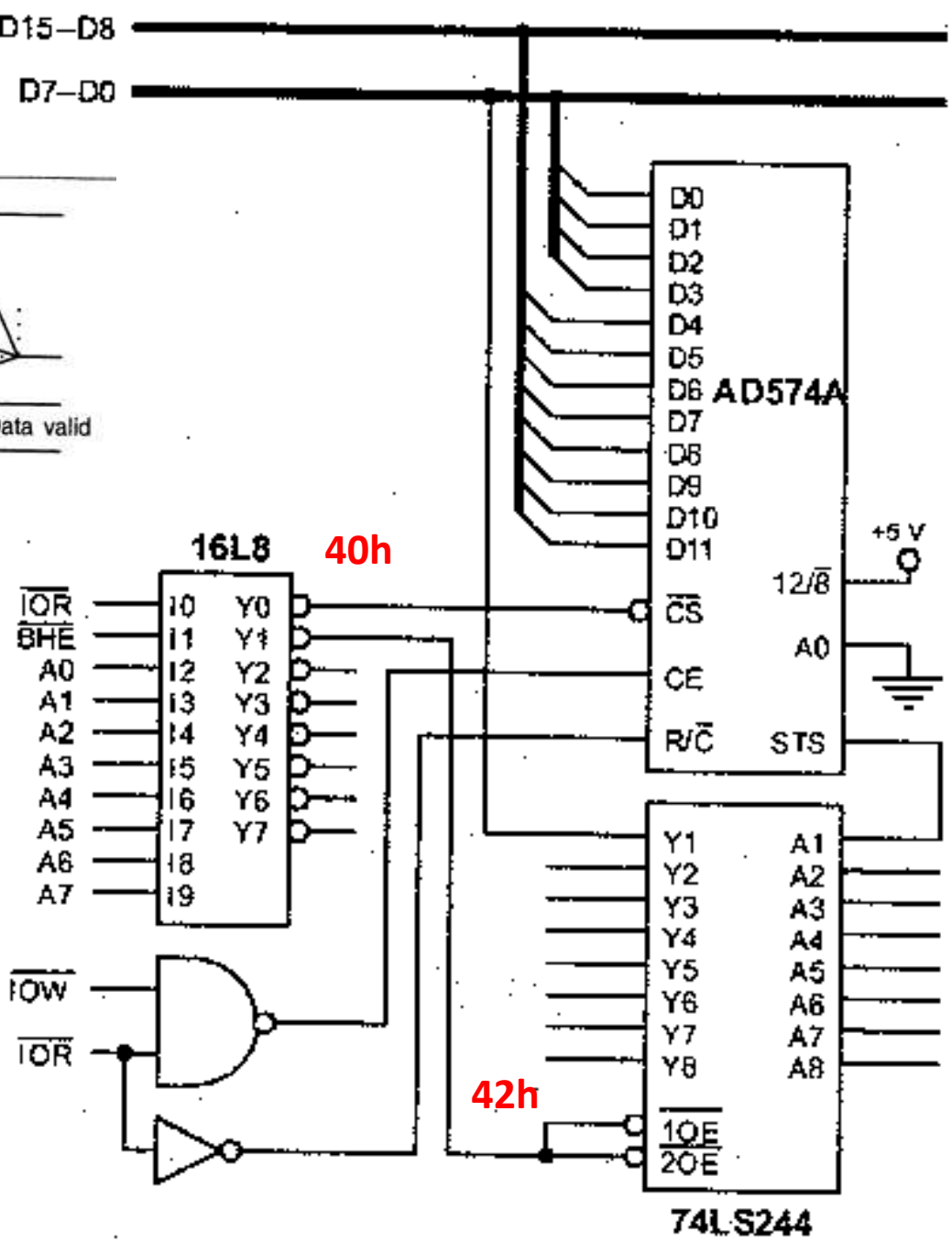
Simplified 8086 Write Bus Cycle

2. Direct connection



Start conv. CS=0; A0=0;R/C=0; CE=L-H

Citire conv. CS=0;A0=0;CE=1;R/C=1



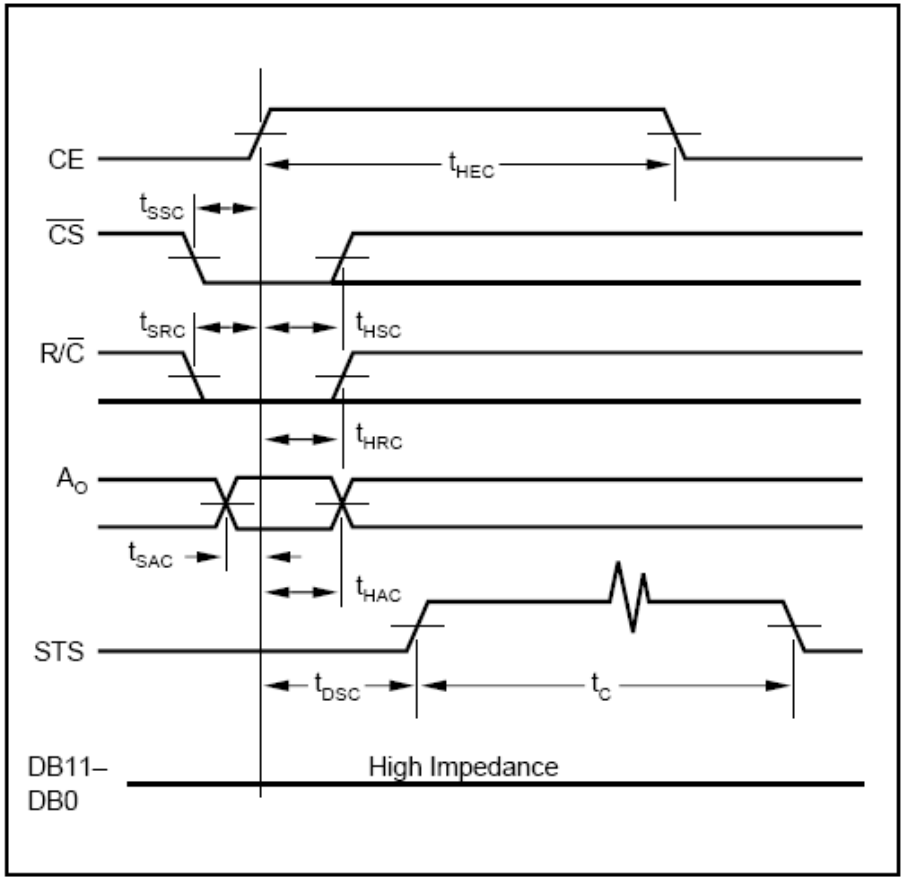


FIGURE 6. Conversion Cycle Timing.

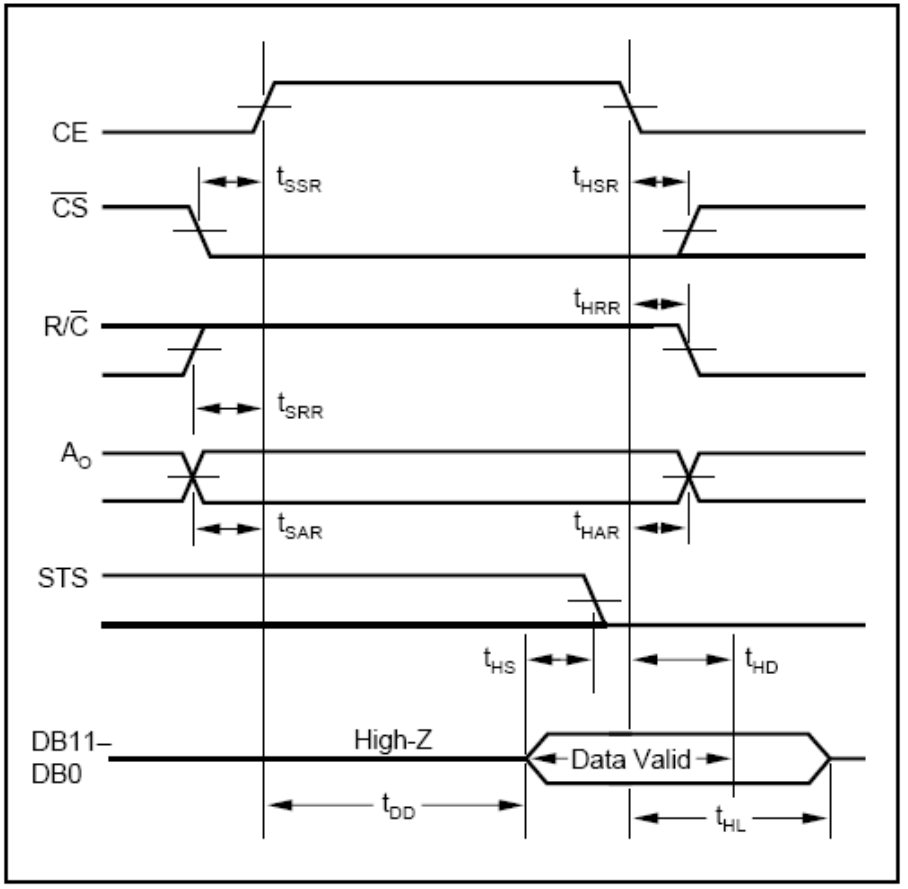
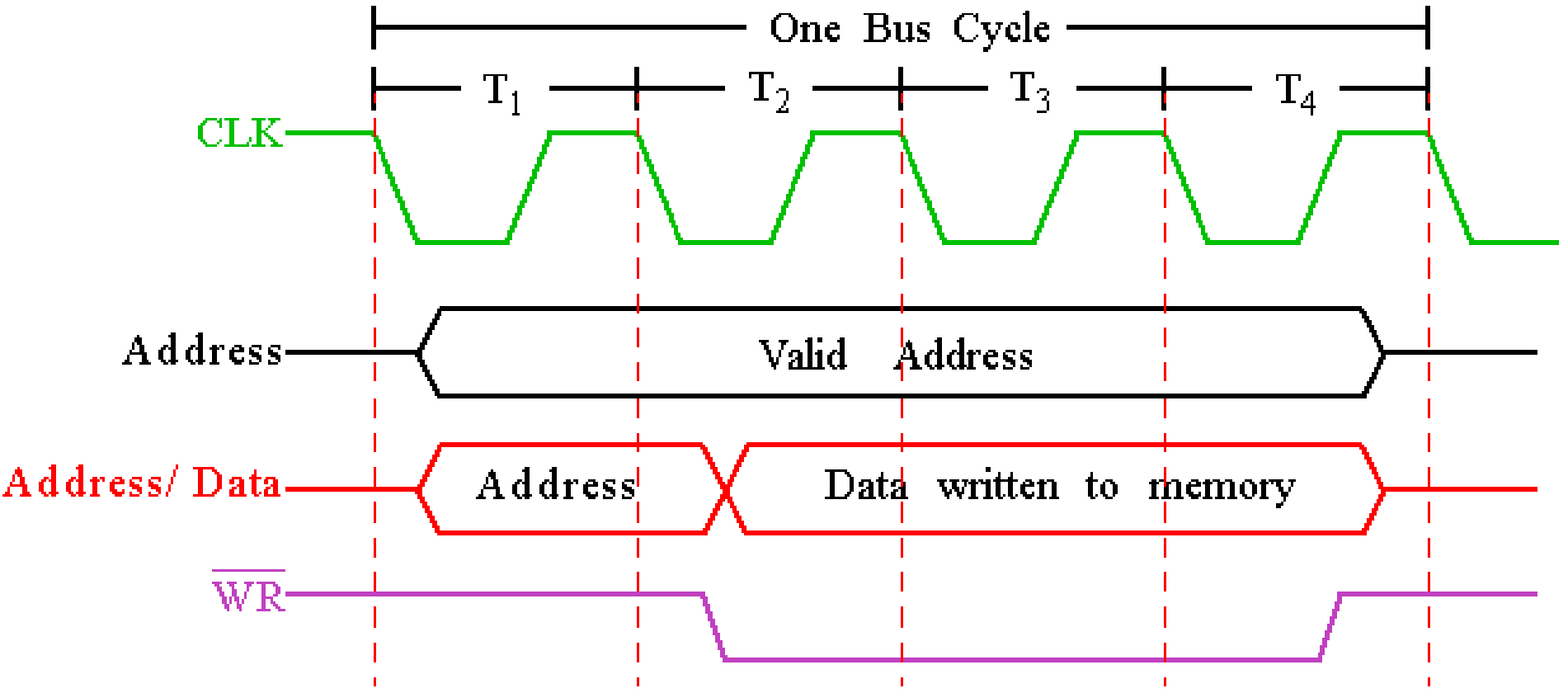
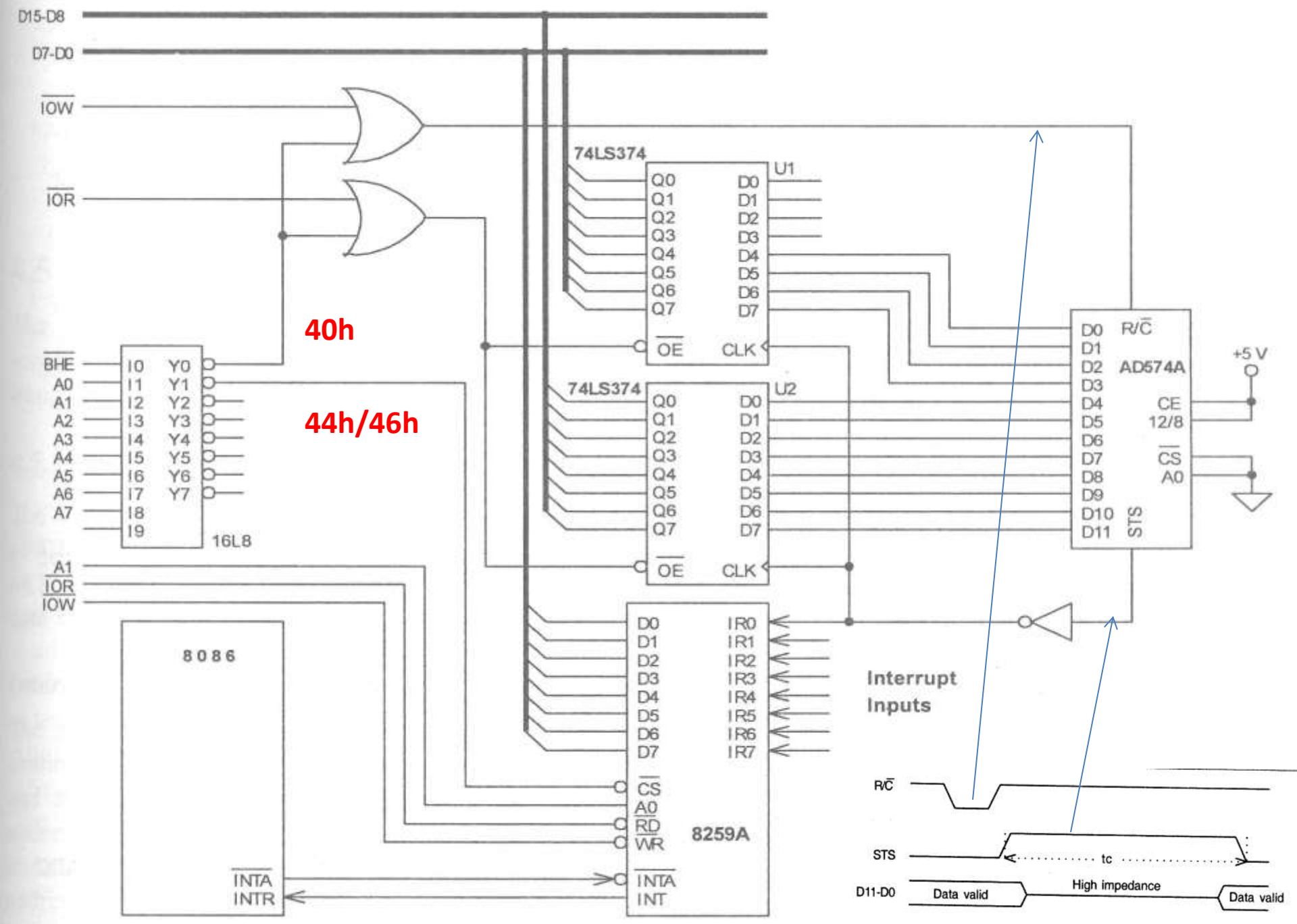


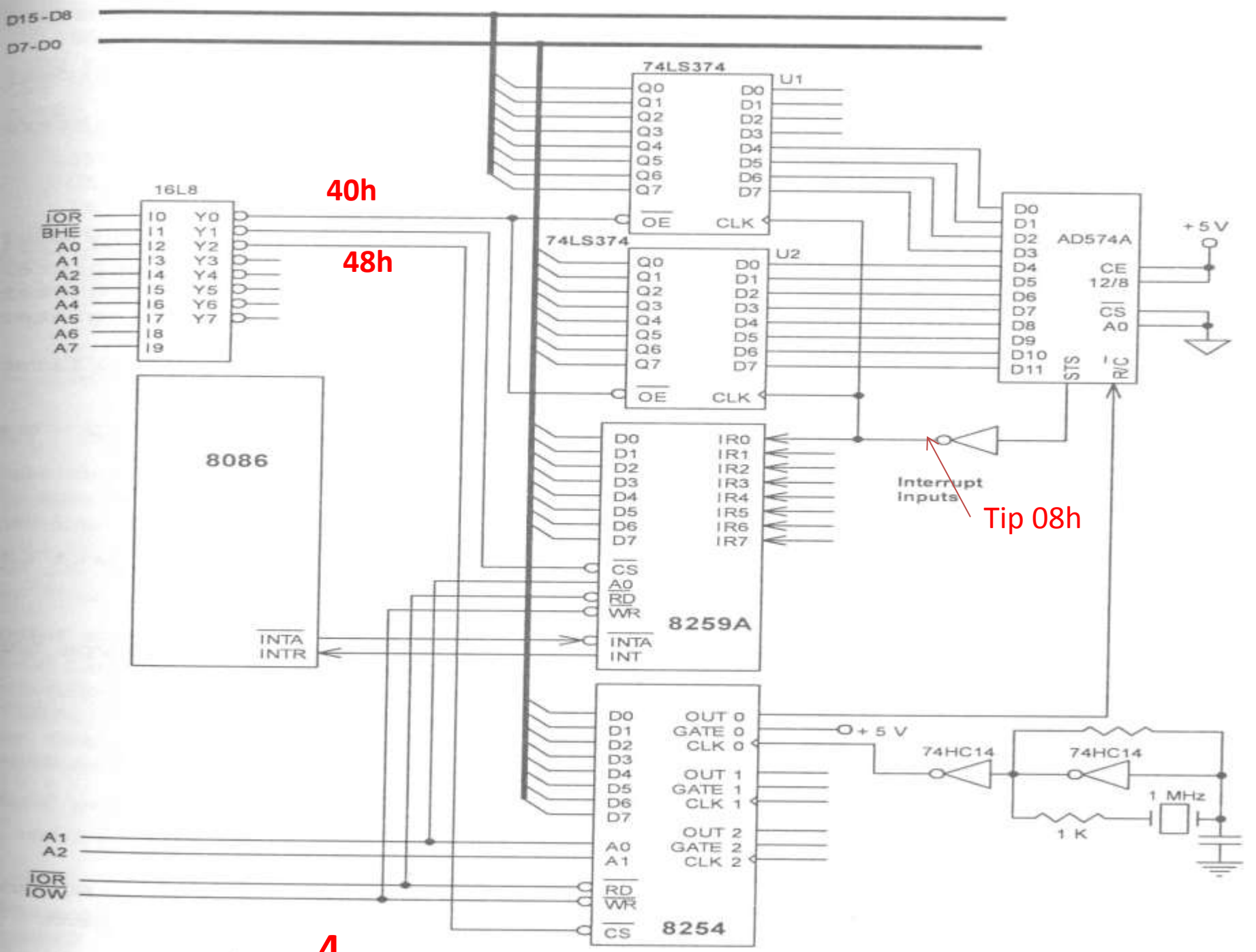
FIGURE 7. Read Cycle Timing.



Simplified 8086 Write Bus Cycle



3. Interrupt driven data acquisition.



4. Timer controlled interrupt driven data acquisition.

5. Modificati schema astfel ca achizitia esantioanelor sa se faca prin DMA.
Scrieti secventele de program care stau la baza functionarii schemei (programare DMAC, generare start conversie, ...)